

## TPA6132A2 25-mW DirectPath™ Stereo Headphone Amplifier With Pop Suppression

### 1 Features

- Patented DirectPath™ Technology Eliminates Need for DC-Blocking Capacitors
  - Outputs Biased at 0 V
  - Excellent Low Frequency Fidelity
- Active Click and Pop Suppression
- 2.1 mA Typical Supply Current
- Fully Differential or Single-Ended Inputs
  - Built-In Resistors Reduces Component Count
  - Improves System Noise Performance
- Constant Maximum Output Power from 2.3 V to 5.5 V Supply
  - Simplifies Design to Prevent Acoustic Shock
- Improved RF Noise Immunity
- Microsoft™ Windows Vista™ Compliant
- High Power Supply Noise Rejection
  - 100 dB PSRR at 217 Hz
  - 90 dB PSRR at 10 kHz
- Wide Power Supply Range: 2.3 V to 5.5 V
- Gain Settings: –6 dB, 0 dB, 3 dB, and 6 dB
- Short-Circuit and Thermal-Overload Protection
- ±8 kV HBM ESD Protected Outputs
- Small Package Available
  - 16-Pin, 3 mm × 3 mm Thin QFN

### 2 Applications

- Smart Phones / Cellular Phones
- Notebook Computers
- CD / MP3 Players
- Portable Gaming

### 3 Description

The TPA6132A2 (sometimes referred to as TPA6132) is a DirectPath™ stereo headphone amplifier that eliminates the need for external dc-blocking output capacitors. Differential stereo inputs and built-in resistors set the device gain, further reducing external component count. Gain is selectable at –6 dB, 0 dB, 3 dB or 6 dB. The amplifier drives 25 mW into 16 Ω speakers from a single 2.3 V supply. The TPA6132A2 (TPA6132) provides a constant maximum output power independent of the supply voltage, thus facilitating the design for prevention of acoustic shock.

The TPA6132A2 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity. For single-ended input signals, connect INL+ and INR+ to ground.

The device has built-in pop suppression circuitry to completely eliminate disturbing pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection along with ±8 kV HBM ESD protection, simplifying end equipment compliance to the IEC 61000-4-2 ESD standard.

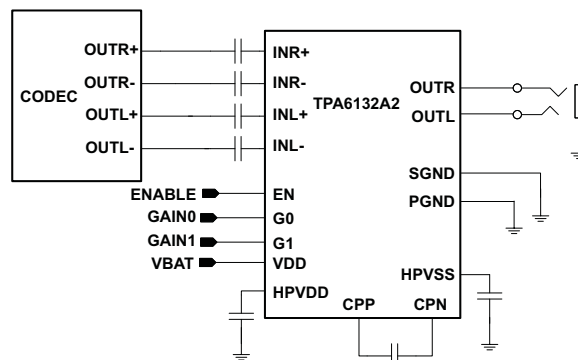
The TPA6132A2 operates from a single 2.3 V to 5.5 V supply with 2.1 mA of typical supply current. Shutdown mode reduces supply current to less than 1 μA.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6132A2	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 Simplified Schematic



## Table of Contents

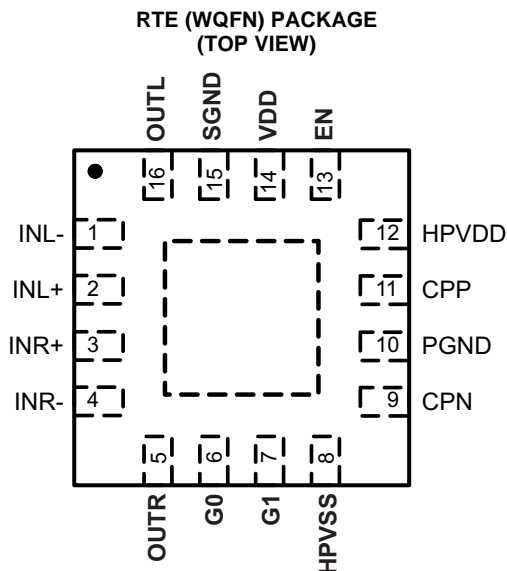
<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description .....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>14</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.1 Application Information .....	<b>14</b>
<b>5 Revision History</b> .....	<b>2</b>	9.2 Typical Applications .....	<b>14</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>17</b>
<b>7 Specifications</b> .....	<b>4</b>	10.1 Power Supply and HPVDD Decoupling Capacitors .....	<b>17</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	<b>11 Layout</b> .....	<b>18</b>
7.2 Handling Ratings .....	<b>4</b>	11.1 Layout Guidelines .....	<b>18</b>
7.3 Recommended Operating Conditions .....	<b>4</b>	11.2 Layout Example .....	<b>18</b>
7.4 Thermal Information .....	<b>4</b>	11.3 GND Connections .....	<b>18</b>
7.5 Electrical Characteristics .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>19</b>
7.6 Operating Characteristics .....	<b>5</b>	12.1 Trademarks .....	<b>19</b>
7.7 Typical Characteristics .....	<b>6</b>	12.2 Electrostatic Discharge Caution .....	<b>19</b>
<b>8 Detailed Description</b> .....	<b>10</b>	12.3 Glossary .....	<b>19</b>
8.1 Overview .....	<b>10</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>19</b>
8.2 Functional Block Diagram .....	<b>10</b>		

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (December 2008) to Revision A</b>	<b>Page</b>
• Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging sections. ....	<b>1</b>
• Added Input voltage: EN, G0, G1 to the <a href="#">Absolute Maximum Ratings</a> table .....	<b>4</b>
• Added Input voltage: INR+, INR-, INL+, INL- to the <a href="#">Recommended Operating Conditions</a> table .....	<b>4</b>
• Changed Output impedance in shutdown From: TYP = 50 Ω To: TYP = 20 Ω in the <a href="#">Operating Characteristics</a> table .....	<b>5</b>

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O/P	DESCRIPTION
NAME	NO.		
INL-	1	I	Inverting left input for differential signals; left input for single-ended signals
INL+	2	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
INR+	3	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications
INR-	4	O	Inverting right input for differential signals; right input for single-ended signals
OUTR	5	I	Right headphone amplifier output. Connect to right terminal of headphone jack
G0	6	I	Gain select
GAIN0		I	
G1	7	P	Gain select
GAIN1		P	
HPVSS	8	P	Charge pump output and negative power supply for output amplifiers; connect 1 $\mu$ F capacitor to GND
CPN	9	P	Charge pump negative flying cap. Connect to negative side of 1 $\mu$ F capacitor between CPP and CPN
PGND	10	P	Ground
CPP	11	P	Charge pump positive flying cap. Connect to positive side of 1 $\mu$ F capacitor between CPP and CPN
HPVDD	12	I	Positive power supply for headphone amplifiers. Connect to a 2.2 $\mu$ F capacitor. Do not connect to VDD
EN	13	P	Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate
VDD	14	I	Positive power supply for TPA6132A2
SGND	15	O	Amplifier reference voltage. Connect to ground terminal of headphone jack
OUTL	16	P	Left headphone amplifier output. Connect to left terminal of headphone jack
Thermal Pad	–		Solder the exposed metal pad on the TPA6132A2RTE QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating).

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	-0.3	6	V
Headphone amplifier supply voltage	HPVDD (do not connect to external supply)	-0.3	1.9	V
Input voltage, $V_I$	INR+, INR-, INL+, INL-	HPVSS -0.3	HPVDD + 0.3	V
	EN, G0, G1	-0.3	HPVDD + 0.3	V
Output continuous total power dissipation		See <a href="#">Thermal Information</a>		
Operating free-air temperature range, $T_A$		-40	85	$^\circ\text{C}$
Operating junction temperature range, $T_J$		-40	150	$^\circ\text{C}$

### 7.2 Handling Ratings

		MIN	MAX	UNIT		
$T_{\text{stg}}$	Storage temperature range	-65	85	$^\circ\text{C}$		
$V_{\text{(ESD)}}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	OUTL, OTR	-8	-8	kV
			All Other Pins	-2	-2	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		-1.5	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage, VDD		2.3	5.5	V
$V_{\text{IH}}$	High-level input voltage; EN, G0, G1	1.3		V
$V_{\text{IL}}$	Low-level input voltage; EN, G0, G1		0.6	V
$V_I$	Input voltage; INR+, INR-, INL+, INL-	0	HPVDD + 0.3	V
Voltage applied to Output; OTR, OUTL (when EN = 0 V)		-0.3	3.6	V
$T_A$	Operating free-air temperature	-40	85	$^\circ\text{C}$

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RTE	UNIT
		16 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	51.1	$^\circ\text{C}/\text{W}$
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	53.9	
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	24.3	
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	0.9	
$\Psi_{\text{JB}}$	Junction-to-board characterization parameter	24.3	
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	9.0	

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage		-0.5		0.5	mV
Power supply rejection ratio	$V_{DD} = 2.3\text{ V to }5.5\text{ V}$		100		dB
High-level output current (EN, G0, G1)				1	$\mu\text{A}$
Low-level output current (EN, G0, G1)				1	$\mu\text{A}$
Supply Current	$V_{DD} = 2.3\text{ V}$ , No load, EN = $V_{DD}$		2.1	3.1	mA
	$V_{DD} = 3.6\text{ V}$ , No load, EN = $V_{DD}$		2.1	3.1	
	$V_{DD} = 5.5\text{ V}$ , No load, EN = $V_{DD}$		2.2	3.2	$\mu\text{A}$
	EN = 0 V, $V_{DD} = 2.3\text{ V to }5.5\text{ V}$		0.7	1.2	

## 7.6 Operating Characteristics

 $V_{DD} = 3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 16\ \Omega$  (unless otherwise noted)

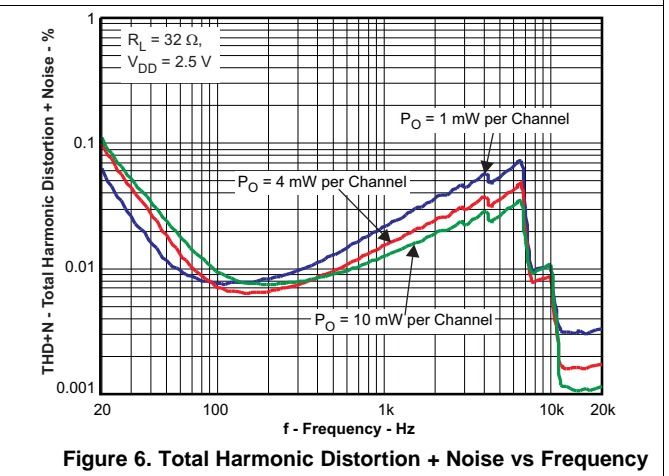
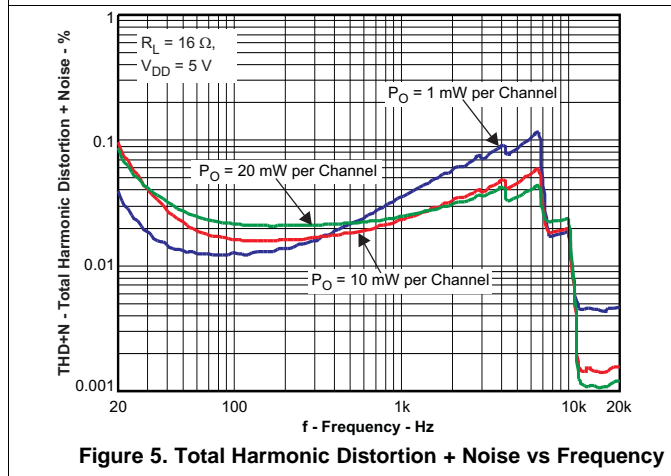
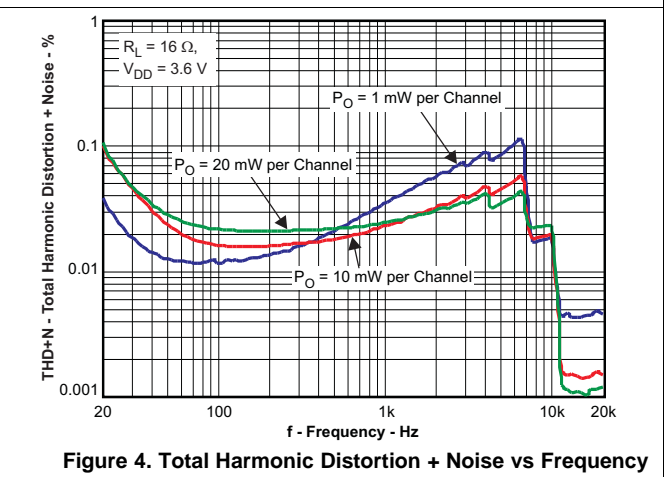
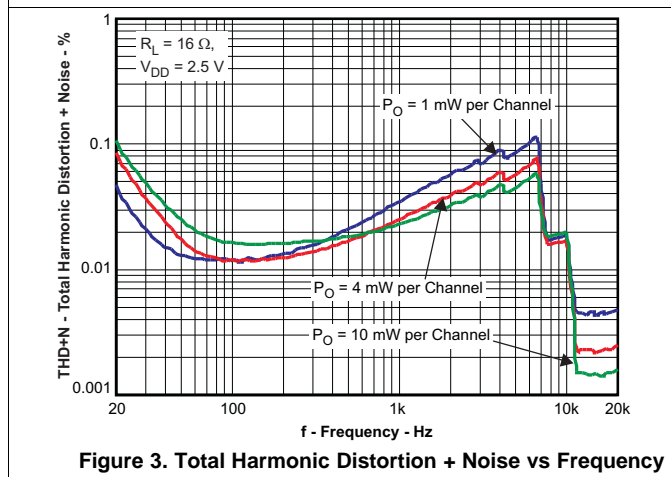
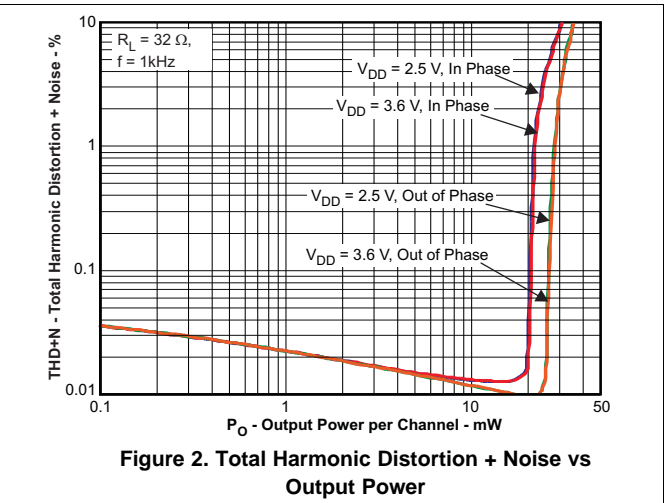
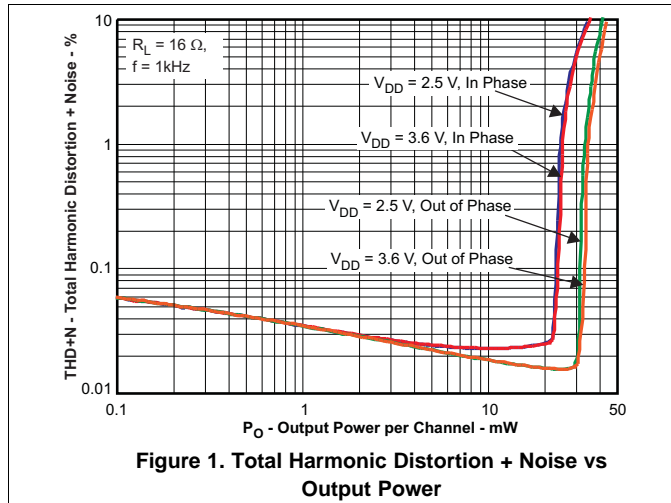
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$ Output power <sup>(1)</sup> (Outputs in phase)	THD = 1%, $f = 1\text{ kHz}$		25		mW
	THD = 1%, $f = 1\text{ kHz}$ , $R_L = 32\ \Omega$		22		
$V_O$ Output voltage <sup>(1)</sup> (Outputs in phase)	THD = 1%, $V_{DD} = 3.6\text{ V}$ , $f = 1\text{ kHz}$ , $R_L = 100\ \Omega$		1.1		$V_{RMS}$
$A_V$ Closed-loop voltage gain (OUT / IN-)	G0 = 0 V, G1 = 0 V, (-6 dB)	-0.45	-0.5	-0.55	V/V
	$G0 \geq 1.3\text{ V}$ , G1 = 0 V, (0 dB)	-0.95	-1.0	-1.05	
	G0 = 0 V, $G1 \geq 1.3\text{ V}$ , (3 dB)	-1.36	-1.41	-1.46	
	$G0 \geq 1.3\text{ V}$ , $G1 \geq 1.3\text{ V}$ , (6 dB)	-1.95	-2.0	-2.05	
$\Delta A_V$ Gain matching	Between Left and Right channels		1%		
$R_{IN}$	Input impedance (per input pin)	G0 = 0 V, G1 = 0 V, (-6 dB)		26.4	k $\Omega$
		$G0 \geq 1.3\text{ V}$ , G1 = 0 V, (0 dB)		19.8	
		G0 = 0 V, $G1 \geq 1.3\text{ V}$ , (3 dB)		16.5	
		$G0 \geq 1.3\text{ V}$ , $G1 \geq 1.3\text{ V}$ , (6 dB)		13.2	
	Input impedance in shutdown (per input pin)	EN = 0 V		10	
$V_{CM}$ Input common-mode voltage range		-0.5		1.5	V
	Output impedance in shutdown		20		$\Omega$
	Input-to-output attenuation in shutdown	EN = 0 V	80		dB
$k_{SVR}$ AC-power supply rejection ratio	200 mV <sub>pp</sub> ripple, $f = 217\text{ Hz}$		-100		dB
	200 mV <sub>pp</sub> ripple, $f = 10\text{ kHz}$		-90		
THD+N Total harmonic distortion plus noise <sup>(2)</sup>	$P_O = 20\text{ mW}$ , $f = 1\text{ kHz}$		0.02%		
	$P_O = 25\text{ mW}$ into $32\ \Omega$ , $V_{DD} = 5.5\text{ V}$ , $f = 1\text{ kHz}$		0.01%		
SNR Signal-to-noise ratio	$P_O = 20\text{ mW}$ ; $G0 \geq 1.3\text{ V}$ , G1 = 0 V, ( $A_V = 0\text{ dB}$ )		100		dB
$E_n$ Noise output voltage	A-weighted		5.5		$\mu\text{V}_{RMS}$
$f_{osc}$ Charge pump switching frequency		1200	1275	1350	kHz
$t_{ON}$ Start-up time from shutdown			5		ms
Crosstalk	$P_O = 20\text{ mW}$ , $f = 1\text{ kHz}$		-80		dB
Thermal shutdown	Threshold		150		$^\circ\text{C}$
	Hysteresis		20		$^\circ\text{C}$

(1) Per output channel

(2) A-weighted

### 7.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{ V}$ , Gain = 0 dB, EN = 3.6 V,  $C_{HPVDD} = C_{HPVSS} = 2.2\ \mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\ \mu\text{F}$ , Outputs in Phase



Typical Characteristics (continued)

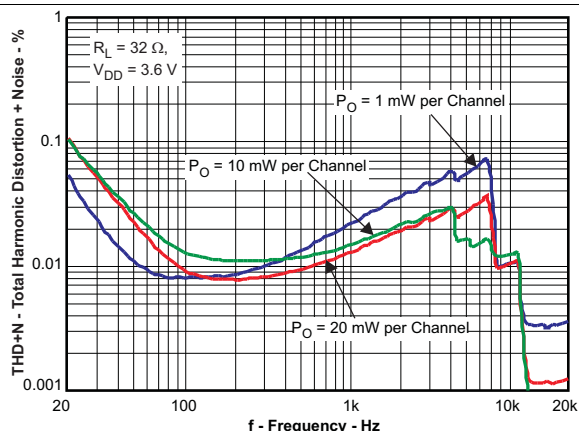


Figure 7. Total Harmonic Distortion + Noise vs Frequency

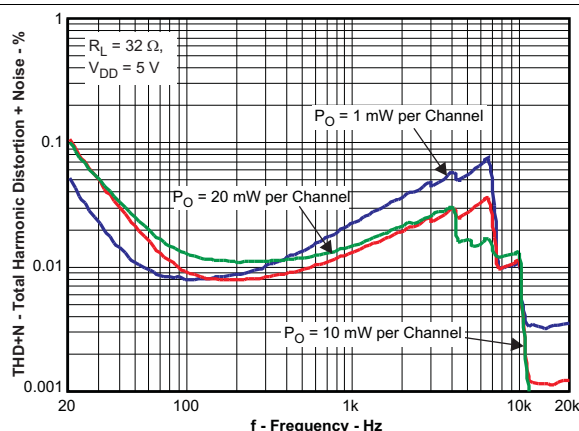


Figure 8. Total Harmonic Distortion + Noise vs Frequency

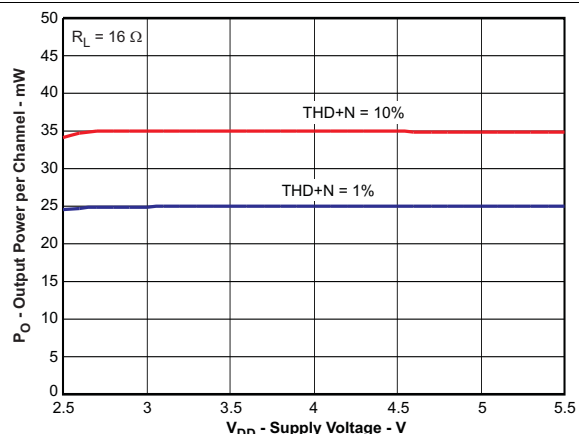


Figure 9. Output Power vs Supply Voltage

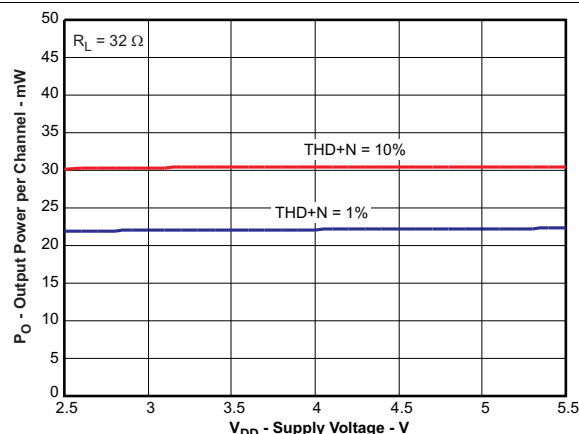


Figure 10. Output Power vs Supply Voltage

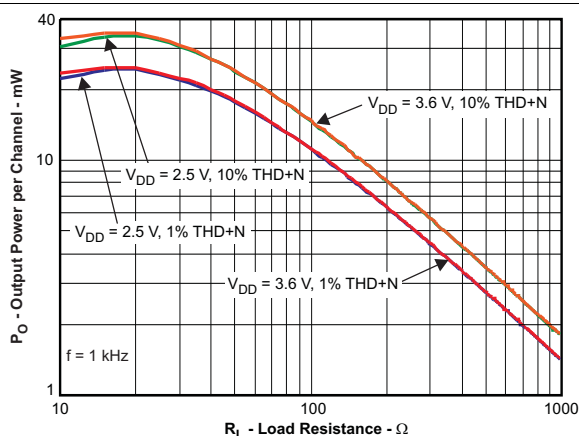


Figure 11. Output Power vs Load Resistance

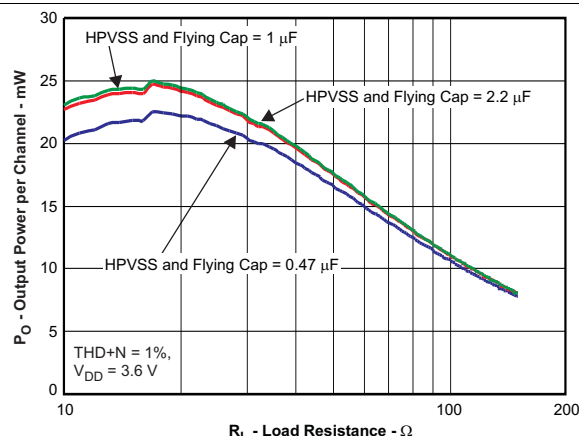


Figure 12. Output Power vs Load Resistance

Typical Characteristics (continued)

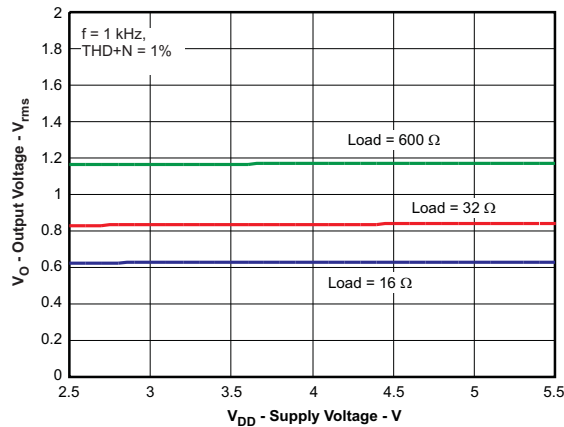


Figure 13. Output Voltage vs Supply Voltage

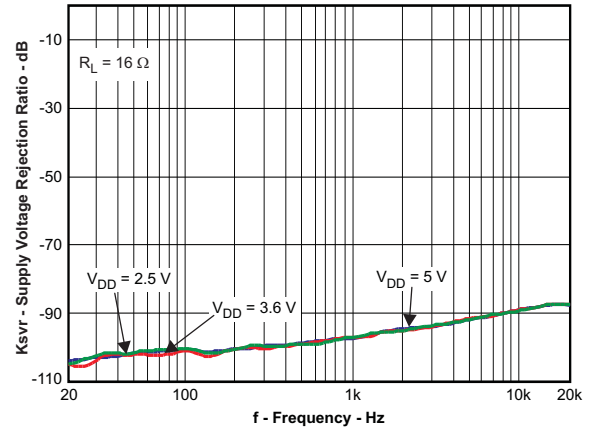


Figure 14. Supply Voltage Rejection Ratio vs Frequency

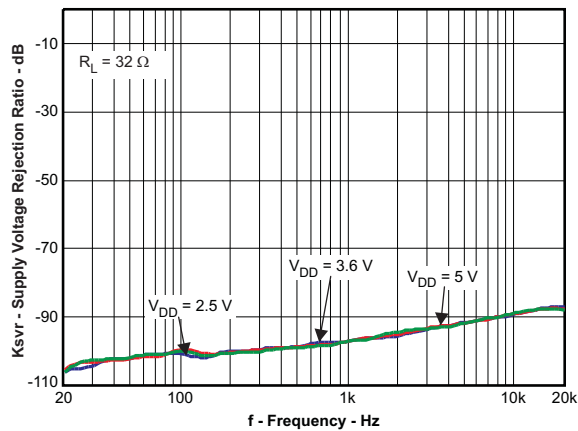


Figure 15. Supply Voltage Rejection Ratio vs Frequency

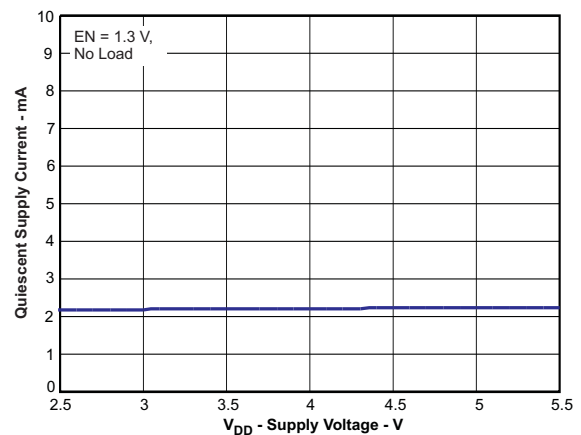


Figure 16. Quiescent Supply Current vs Supply Voltage

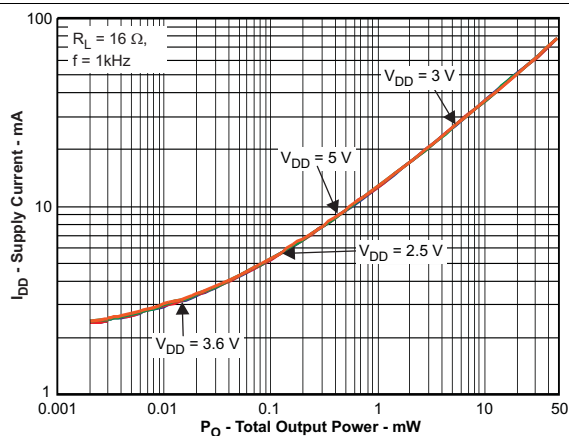


Figure 17. Supply Current vs Total Output Power

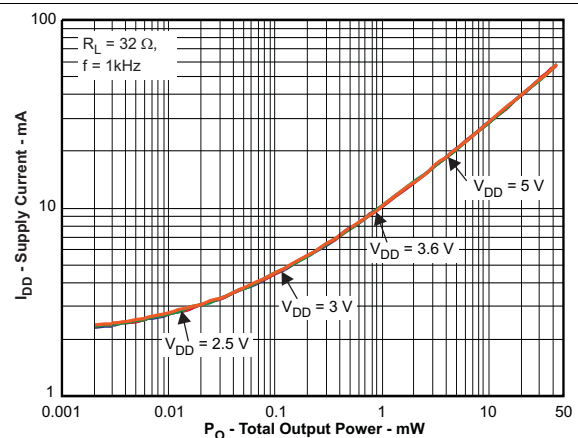


Figure 18. Supply Current vs Total Output Power



Typical Characteristics (continued)

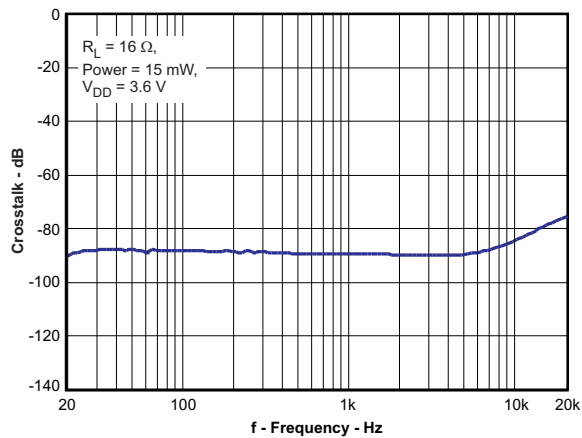


Figure 19. Crosstalk vs Frequency

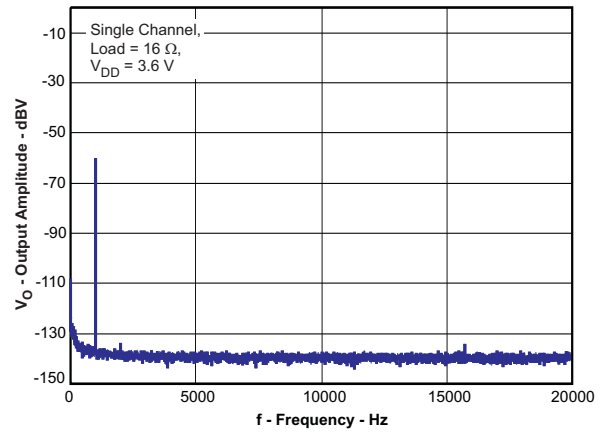


Figure 20. Output Spectrum vs Frequency

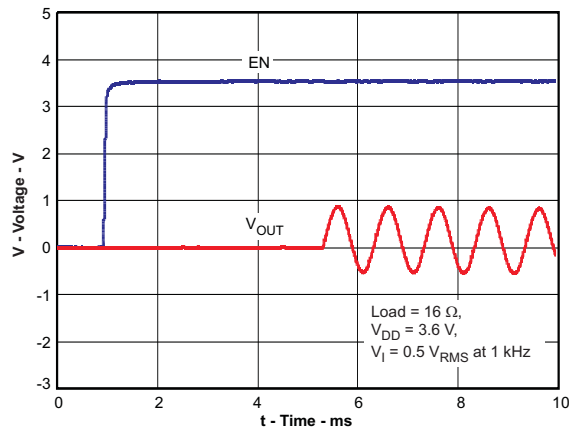


Figure 21. Startup Waveforms vs Time

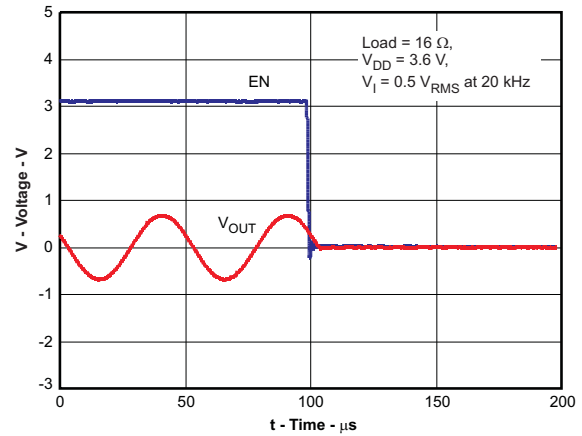


Figure 22. Shutdown Waveforms vs Time

## 8 Detailed Description

### 8.1 Overview

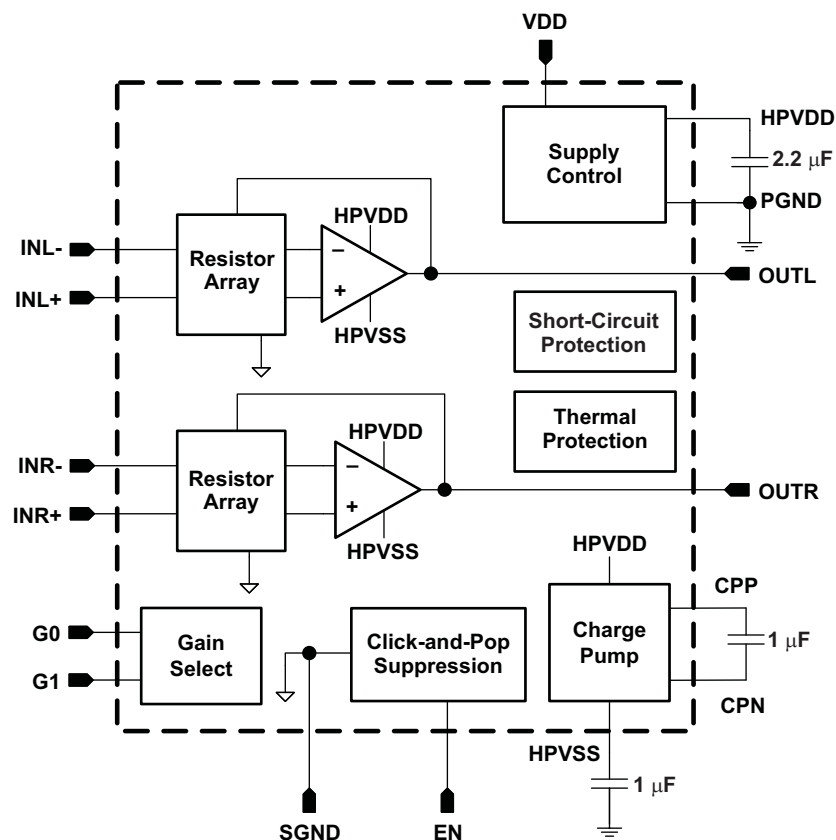
The TPA6132A2 is a DirectPath™ stereo headphone amplifier that requires no output DC blocking capacitors and is capable of delivering 25m-W/Ch into 16-Ω speakers. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection.

The TPA6132A2 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity.

Differential stereo inputs and built-in resistors set the device gain, reducing external component count. The TPA6132A2 has four gain settings which are controlled with pins G0 and G1. The combination of these pins set the device to –6-dB, 0-dB, 3-dB or 6-dB gain.

The TPA6132A2 operates from a single 2.3-V to 5.5-V supply with 2.1 mA of typical supply current, as it uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. Shutdown mode reduces supply current to less than 1 μA.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in [Figure 23](#) illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clip the output signal, and potentially damage the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16 Ω and 32 Ω. This combination creates a high-pass filter with a cutoff frequency as shown in [Equation 1](#), where  $R_L$  is the load impedance,  $C_O$  is the dc-block capacitor, and  $f_c$  is the cutoff frequency.

$$f_c = \frac{1}{2\pi R_L C_O} \quad (1)$$

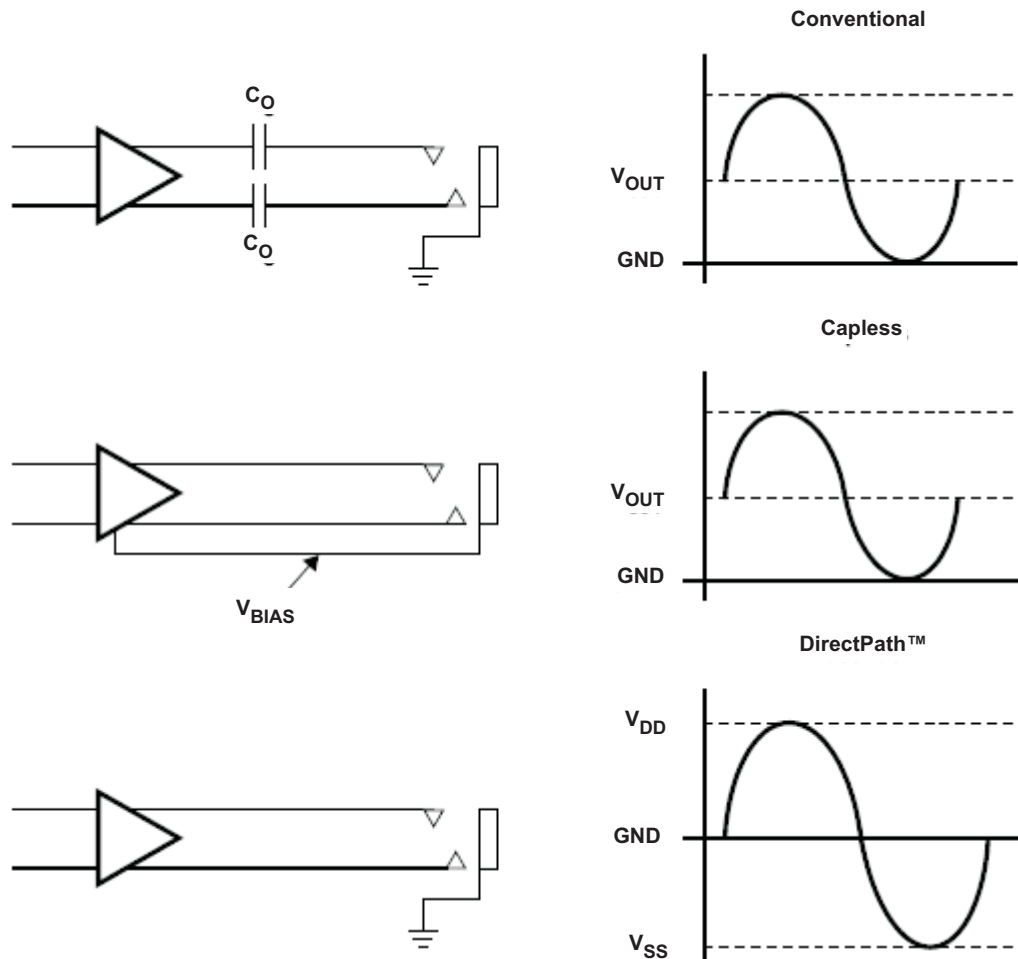
For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_c R_L} \quad (2)$$

Reducing  $f_c$  improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with 16 Ω headphones,  $C_O$  must be at least 500 μF. Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The Capless amplifier architecture is similar provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of [Figure 23](#). The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a Capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes Capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifiers are useful only with floating GND headphones.

**Feature Description (continued)**

**Figure 23. Amplifier Applications**

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 23. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6132A2 is a DirectPath amplifier.

**8.3.2 Eliminating Turn-on Pop and Power Supply Sequencing**

The TPA6132A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6132A2 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the TPA6132A2 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to deactivate the TPA6132A2; set to 1.3 V or higher to activate.

## Feature Description (continued)

### 8.3.3 RF and Power Supply Noise Immunity

The TPA6132A2 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6132A2 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

### 8.3.4 Constant Maximum Output Power and Acoustic Shock Prevention

Typically the output power increases with increasing supply voltage on an unregulated headphone amplifier. The TPA6132A2 maintains a constant output power independent of the supply voltage. Thus the design for prevention of acoustic shock (hearing damage due to exposure to a loud sound) is simplified since the output power will remain constant, independent of the supply voltage. This feature allows maximizing the audio signal at the lowest supply voltage.

## 8.4 Device Functional Modes

### 8.4.1 Gain Control

The TPA6132A2 has four gain settings which are controlled with pins G0 and G1. [Table 1](#) gives an overview of the gain function.

G0 VOLTAGE	G1 VOLTAGE	AMPLIFIER GAIN
≤ 0.5 V	≤ 0.5 V	–6 dB
≥ 1.3 V	≤ 0.5 V	0 dB
≤ 0.5 V	≥ 1.3 V	3 dB
≥ 1.3 V	≥ 1.3 V	6 dB

**Table 1. Windows Vista™ Premium Mobile Mode Specifications**

Device Type	Requirement	Windows Premium Mobile Vista Specifications	TPA6132A2 Typical Performance
Analog Speaker Line Jack ( $R_L = 10\text{ k}\Omega$ , FS = 0.707 Vrms)	THD+N	≤ –65 dB FS [20 Hz, 20 kHz]	–75 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ –80 dB FS A-Weight	–100 dB FS A-Weight
	Line Output Crosstalk	≤ –60 dB [20 Hz, 20 kHz]	–90 dB [20 Hz, 20 kHz]
Analog Headphone Out Jack ( $R_L = 32\Omega$ , FS = 0.300 Vrms)	THD+N	≤ –45 dB FS [20 Hz, 20 kHz]	–65 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ –80 dB FS A-Weight	–94 dB FS A-Weight
	Headphone Output Crosstalk	≤ –60 dB [20 Hz, 20 kHz]	–90 dB [20 Hz, 20 kHz]

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

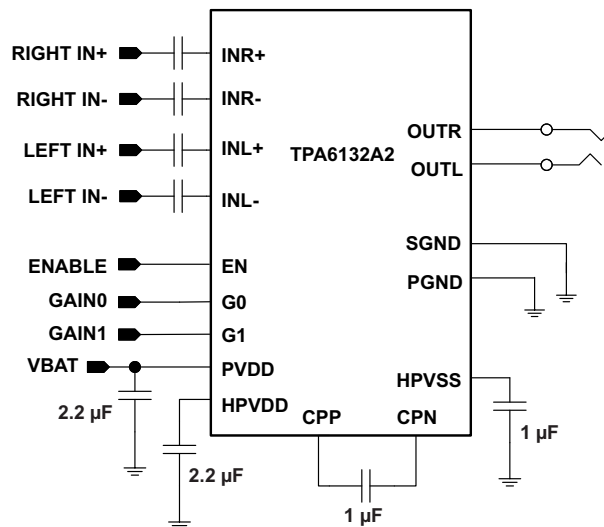
### 9.1 Application Information

The TPA6132A2 starts its operation by asserting the EN pin to logic 1. The device enters in shutdown mode when pulling low EN pin. The charge pump generates a negative supply voltage. The charge pump flying capacitor connected between CPP and CPN transfers charge to generate the negative supply voltage. The output voltages are capable of positive and negative voltage swings and are centered close to 0 V, eliminating the need for output capacitors. Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on, turn-off and enter or exit shutdown mode.

### 9.2 Typical Applications

#### 9.2.1 Configuration with Differential Input Signals

Figure 24 shows a typical application circuit for the TPA6132A2 with a stereo headphone jack output and differential input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.



**Figure 24. Typical Application Configuration with Differential Input Signals**

#### 9.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 2.

**Table 2. Design Parameters**

PARAMETERS	VALUES
Input voltage range	2.2 V to 5.3 V
Output voltage	1.1- $V_{RMS}$
Current	2 mA to 3.2 mA

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Input Coupling Capacitors

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6132A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6132A2 internal input resistors, creating a high-pass filter. Equation 3 calculates the high-pass filter corner frequency. The input impedance,  $R_{IN}$ , is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \tag{3}$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \tag{4}$$

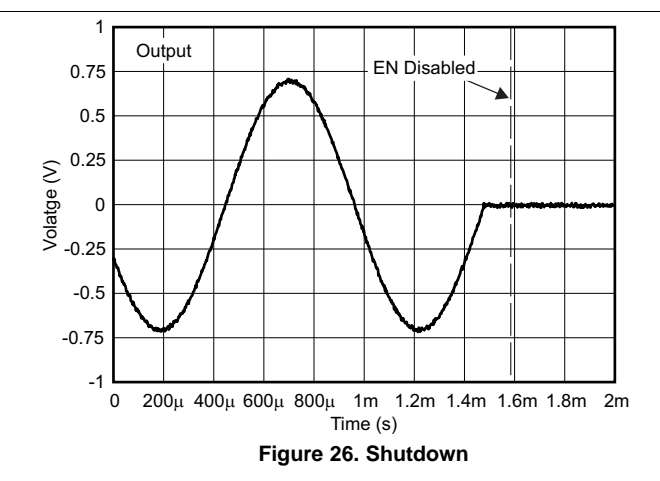
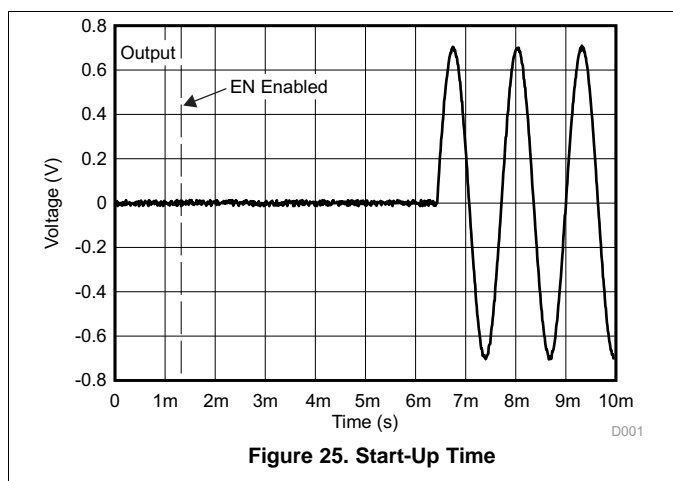
Example: Design for a 20 Hz corner frequency with a TPA6132A2 gain of +6 dB. The Operating Characteristics table gives  $R_{IN}$  as 13.2 kΩ. Equation 4 shows the input coupling capacitors must be at least 0.6 μF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 μF standard value capacitor for each TPA6132A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6132A2 inputs are driven differentially with less than ±1 V and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

#### 9.2.1.2.2 Charge Pump Flying Capacitor and HPVSS Capacitor

The TPA6132A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 μF to 2.2 μF for the HPVSS and flying capacitors. Although values down to 0.47 μF can be used, total harmonic distortion (THD) will increase.

### 9.2.1.3 Application Curves



### 9.2.2 Configuration with Single-Ended Input Signals

Figure 27 shows a typical application circuit for the TPA6132A2 with a stereo headphone jack output and single-ended input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.

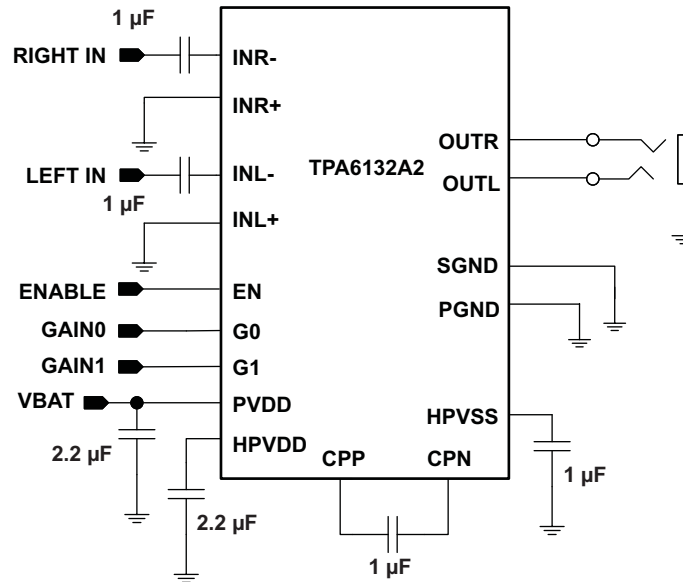


Figure 27. Typical Application Configuration with Single-Ended Input Signals

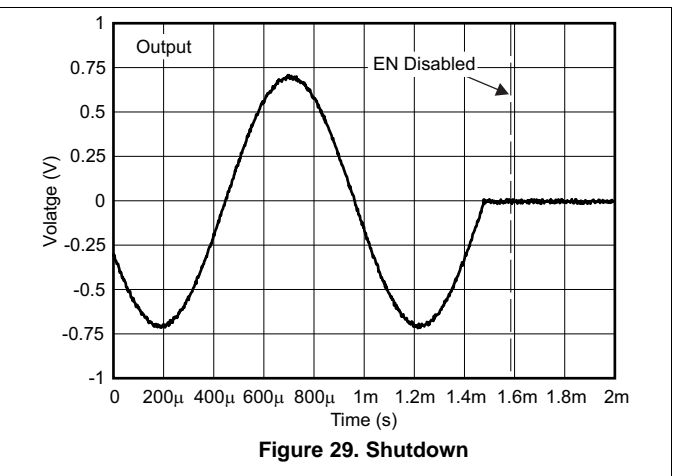
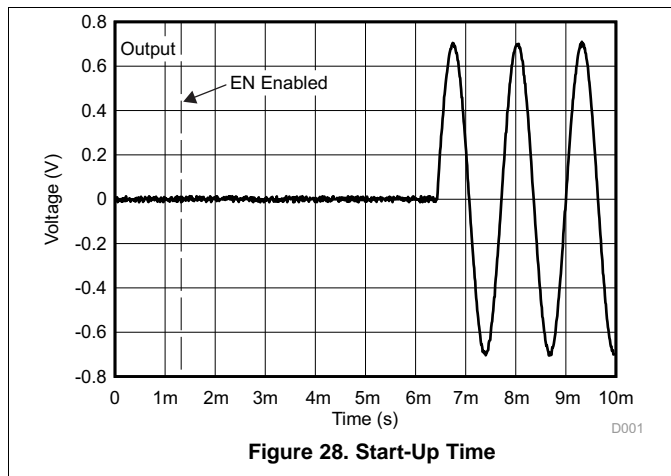
#### 9.2.2.1 Design Requirements

Refer to the [Configuration with Differential Input Signals](#) design requirements

#### 9.2.2.2 Detailed Design Procedure

Refer to the [Configuration with Differential Input Signals](#) detailed design procedures.

#### 9.2.2.3 Application Curves





## 10 Power Supply Recommendations

Connect the supply voltage to the VDD pin and decouple it with an X5R or better capacitor. Connect the HPVDD pin only to a 2.2  $\mu\text{F}$ , X5R or better, capacitor. Do not connect HPVDD to an external voltage supply. Place both capacitors within 5 mm of their associated pins on the TPA6132A2. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6132A2 may degrade audio or EMC performance.

### 10.1 Power Supply and HPVDD Decoupling Capacitors

The TPA6132A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2  $\mu\text{F}$  capacitor within 5 mm of the VDD pin. Reducing the distance between the decoupling capacitor and VDD minimizes parasitic inductance and resistance, improving TPA6132A2 supply rejection performance. Use 0402 or smaller size capacitors if possible.

For additional supply rejection, connect an additional 10  $\mu\text{F}$  or higher value capacitor between VDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6132A2 makes the 10  $\mu\text{F}$  capacitor unnecessary in most applications.

Connect a 2.2  $\mu\text{F}$  capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

#### WARNING

**DO NOT connect HPVDD directly to VDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.**

## 11 Layout

### 11.1 Layout Guidelines

- Solder the exposed metal pad on the TPA6132A2RTE QFN package to the landing pad on the PCB.
- Connect the landing pad to ground or leave it electrically unconnected (floating). *Do not connect the landing pad to VDD or to any other power supply voltage.*
- If the pad is grounded, it must be connected to the same ground as the PGND pin (10).
- See the layout and mechanical drawings at the end of the data sheet for proper sizing.
- Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

**WARNING**

**DO NOT connect the TPA6132A2RTE exposed metal pad to VDD or any other power supply voltage.**

### 11.2 Layout Example

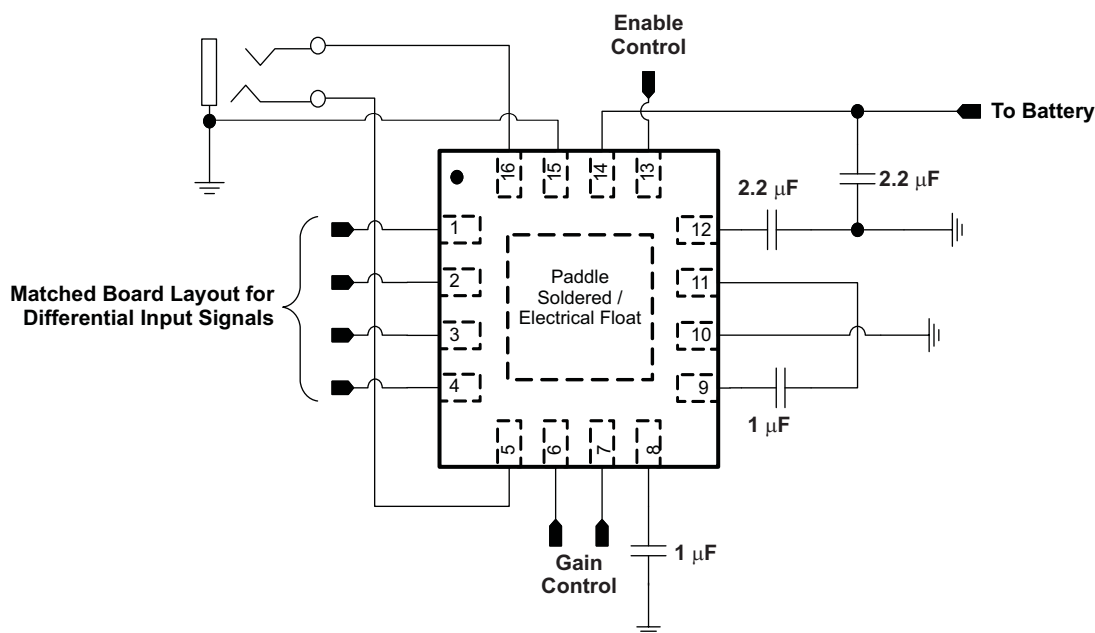


Figure 30. Board Layout Concept

### 11.3 GND Connections

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3$  V to SGND.

PGND is a power ground. Connect supply decoupling capacitors for VDD, HPVDD, and HPVSS to PGND.

## 12 Device and Documentation Support

### 12.1 Trademarks

DirectPath is a trademark of Texas Instruments.  
Windows Vista is a trademark of Microsoft Corporation.  
All other trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6132A2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6132A2RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPA6132A2RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6132A2RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPA6132A2RTET	WQFN	RTE	16	250	195.0	200.0	45.0
TPA6132A2RTET	WQFN	RTE	16	250	210.0	185.0	35.0

# MECHANICAL DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

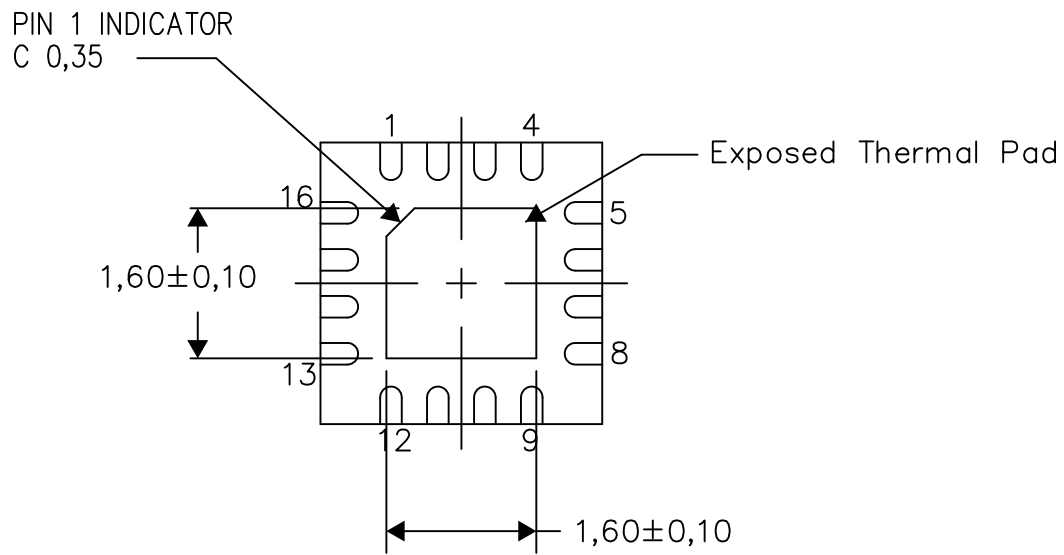
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446-2/U 08/15

NOTE: A. All linear dimensions are in millimeters

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

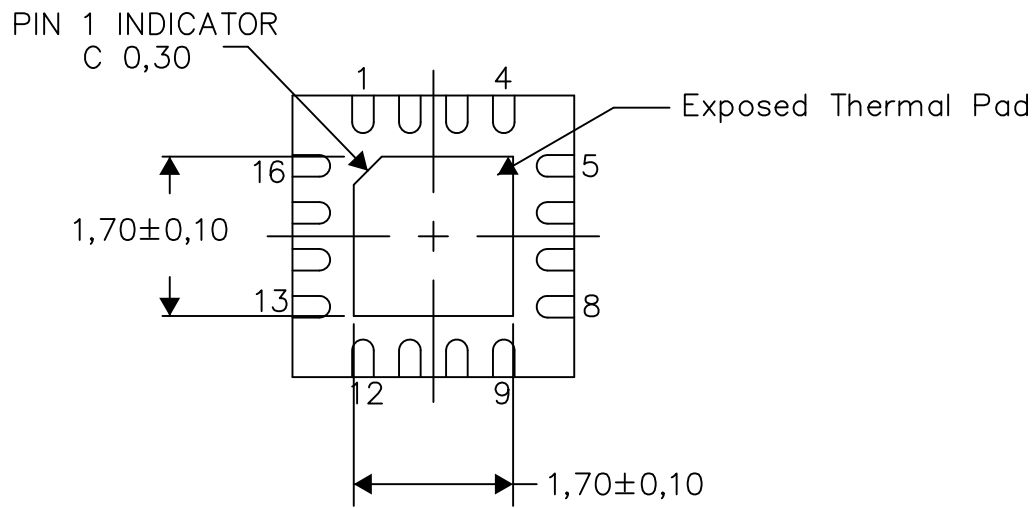
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

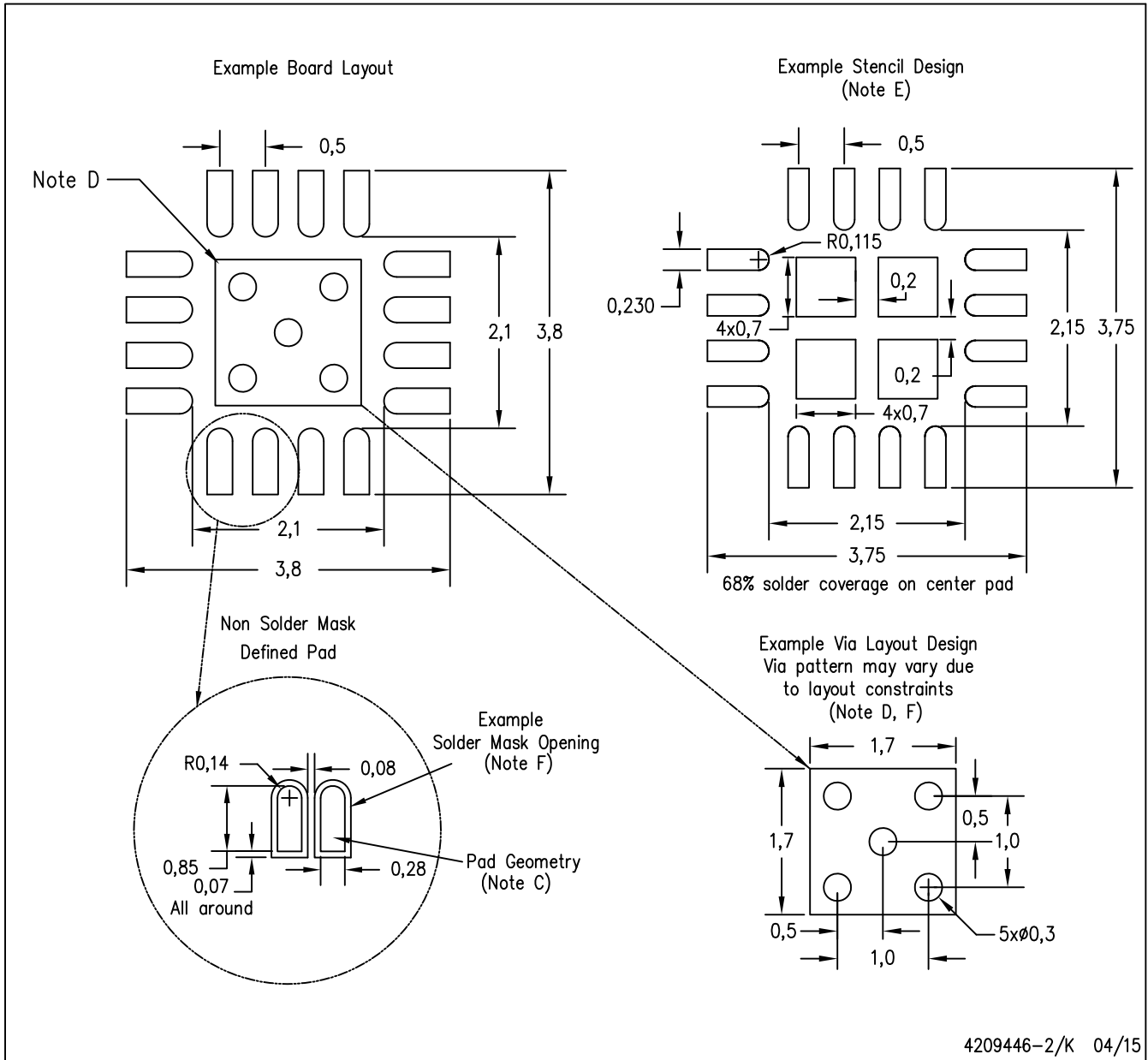
4206446-3/U 08/15

NOTE: A. All linear dimensions are in millimeters



RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

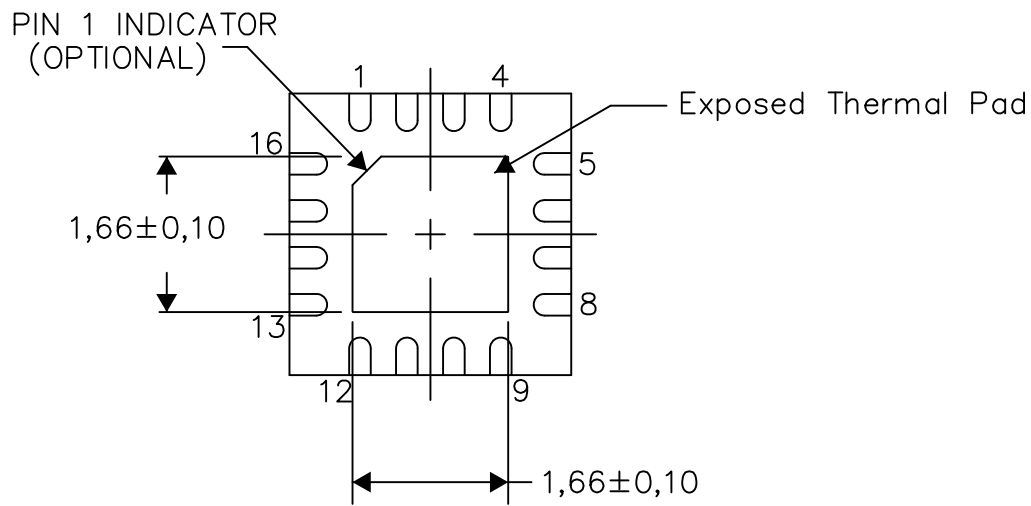
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

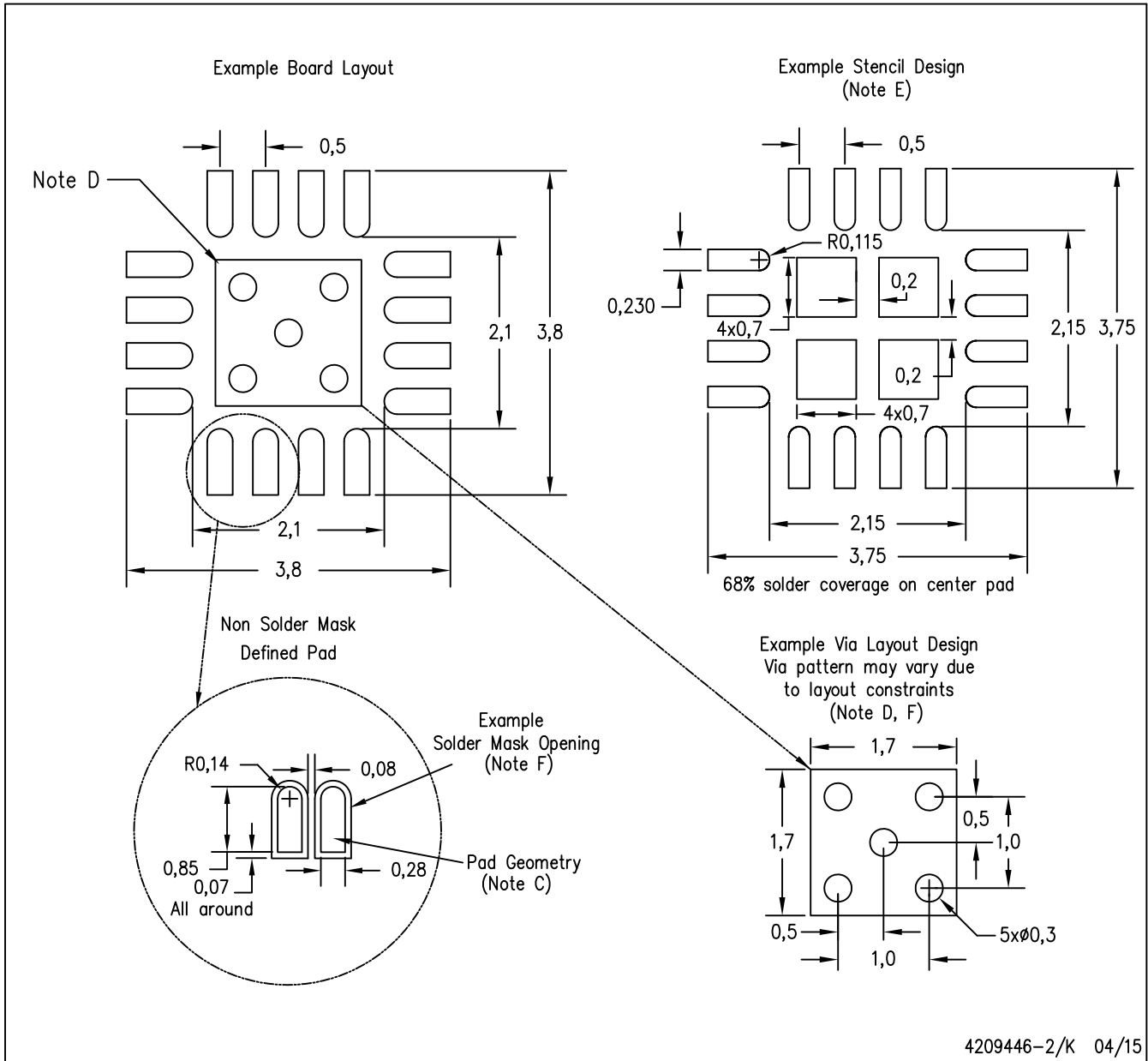
Exposed Thermal Pad Dimensions

4206446-8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.