High Voltage, Latch-Up Proof, Triple SPDT Switches

Data Sheet **ADG5433W**

FEATURES

Qualified for automotive applications
Fully specified at +12 V, +36 V , ±15 V, and ±20 V
Latch-up proof
Low on resistance (13.5 Ω)
9 V to 40 V single-supply operation
±9 V to ±22 V dual-supply operation
VSS to VDD analog signal range
Human body model (HBM) ESD rating: 8 kV

APPLICATIONS

Relay replacement
Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAM

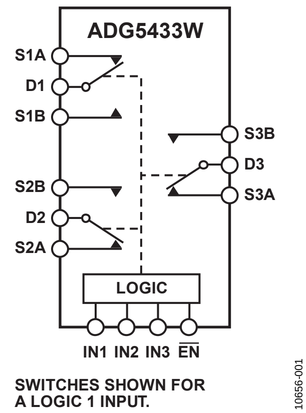

Figure 1.

GENERAL DESCRIPTION

The ADG5433W is a monolithic industrial CMOS analog switch comprising three independently selectable single-pole, double-throw (SPDT) switches.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG5433W (TSSOP package) is used to enable or disable the device. When disabled, all channels are switched off.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON}.
3. Dual-Supply Operation.
   For applications where the analog signal is bipolar, the ADG5433W can be operated from dual supplies up to ±22 V.
4. Single-Supply Operation.
   For applications where the analog signal is unipolar, the ADG5433W can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.

Rev. A Document Feedback

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REVISION HISTORY

4/13—Revision A: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}		13.5	22	Ω	V_S = ±10 V, I_S = −10 mA, V_{DD} = +13.5 V, V_{SS} = −13.5 V; see Figure 23
On-Resistance Match Between Channels, ΔR_{ON}		0.3	1.4	Ω	V_S = ±10 V, I_S = −10 mA
On-Resistance Flatness, $R_{FLAT (ON)}$		1.8	3	Ω	V_S = ±10 V, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)		±0.05	±10	nA	V_S = ±10 V, V_D = ∓10 V; see Figure 22
Drain Off Leakage, I_D (Off)		±0.1	±30	nA	V_S = ±10 V, V_D = ∓10 V; see Figure 22
Channel On Leakage, I_D (On), I_S (On)		±0.1	±30	nA	V_S = V_D = ±10 V; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{INL} or I_{INH}		0.002		μA	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA	
Digital Input Capacitance, C_{IN}		6		pF	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$		157	272	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
t_{ON} ($\overline{EN}$)		160	274	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V; see Figure 30
t_{OFF} ($\overline{EN}$)		91	140	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V; see Figure 30
Break-Before-Make Time Delay, t_D	21	45		ns	R_L = 300 Ω, C_L = 35 p,F V_{S1} = V_{S2} = 10 V; see Figure 29
Charge Injection, Q_{INJ}		130		pC	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Channel-to-Channel Crosstalk		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
Total Harmonic Distortion + Noise		0.01		%	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 26
−3 dB Bandwidth		145		MHz	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss		−0.9		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)		14		pF	V_S = 0 V, f = 1 MHz
C_D (Off)		24		pF	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)		53		pF	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}		45	70	μA	Digital inputs = 0 V or V_{DD}
I_{SS}		0.001	1	μA	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}	±9		±22	V	GND = 0 V

[1] Typical specifications represent average readings at 25°C.
[2] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}		12.5	21	Ω	V_S = ±15 V, I_S = −10 mA, V_{DD} = +18 V, V_{SS} = −18 V; see Figure 23
On-Resistance Match Between Channels, ΔR_{ON}		0.3	1.4	Ω	V_S = ±15 V, I_S = −10 mA
On-Resistance Flatness, $R_{FLAT (ON)}$		2.3	3.5	Ω	V_S = ±15 V, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)		±0.05	±10	nA	V_S = ±15 V, V_D = ∓ 15 V; see Figure 22
Drain Off Leakage, I_D (Off)		±0.1	±30	nA	V_S = ±15 V, V_D = ∓ 15 V; see Figure 22
Channel On Leakage, I_D (On), I_S (On)		±0.1	±30	nA	V_S = V_D = ±15 V; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{INL} or I_{INH}		0.002		µA	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA	
Digital Input Capacitance, C_{IN}		6		pF	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$		150	253	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V
t_{ON} ($\overline{EN}$)		152	253	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V; see Figure 30
t_{OFF} ($\overline{EN}$)		90	130	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V; see Figure 30
Break-Before-Make Time Delay, t_D	17	36		ns	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 10 V; see Figure 29
Charge Injection, Q_{INJ}		176		pC	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1MHz; see Figure 25
Channel-to-Channel Crosstalk		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
Total Harmonic Distortion + Noise		0.012		%	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 26
−3 dB Bandwidth		140		MHz	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss		−0.8		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)		15		pF	V_S = 0 V, f = 1 MHz
C_D (Off)		23		pF	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)		52		pF	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}		50		µA	Digital inputs = 0 V or V_{DD}
		70	110	µA	
I_{SS}		0.001		µA	Digital inputs = 0 V or V_{DD}
			1	µA	
V_{DD}/V_{SS}	±9		±22	V	GND = 0 V

[1] Typical specifications represent average readings at 25°C.
[2] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}		26	42	Ω	V_S = 0 V to 10 V, I_S = −10 mA, V_{DD} = 10.8 V, V_{SS} = 0 V; see Figure 23
On-Resistance Match Between Channels, ΔR_{ON}		0.3	1.6	Ω	V_S = 0 V to 10 V, I_S = −10 mA
On-Resistance Flatness, $R_{FLAT (ON)}$		5.5	12	Ω	V_S = 0 V to 10 V, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)		±0.05	±10	nA	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 22
Drain Off Leakage, I_D (Off)		±0.1	±30	nA	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 22
Channel On Leakage, I_D (On), I_S (On)		±0.1	±30	nA	V_S = V_D = 1 V/10 V; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{INL} or I_{INH}		0.002		μA	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA	
Digital Input Capacitance, C_{IN}		6		pF	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$		220	400	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V
t_{ON} ($\overline{EN}$)		228	426	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; see Figure 30
t_{OFF} ($\overline{EN}$)		90	151	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; see Figure 30
Break-Before-Make Time Delay, t_D	54	106		ns	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 8 V; see Figure 29
Charge Injection, Q_{INJ}		60		pC	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Channel-to-Channel Crosstalk		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
Total Harmonic Distortion + Noise		0.1		%	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 26
−3 dB Bandwidth		150		MHz	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss		−0.8		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)		18		pF	V_S = 6 V, f = 1 MHz
C_D (Off)		28		pF	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)		54		pF	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}		40		μA	Digital inputs = 0 V or V_{DD}
		50	65	μA	
V_{DD}	9		40	V	GND = 0 V, V_{SS} = 0 V

[1] Typical specifications represent average readings at 25°C.
[2] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}		14.5	23	Ω	V_S = 0 V to 30 V, I_S = −10 mA, V_{DD} = 32.4 V, V_{SS} = 0 V; see Figure 23
On-Resistance Match Between Channels, ΔR_{ON}		0.3	1.4	Ω	V_S = 0 V to 30 V, I_S = −10 mA
On-Resistance Flatness, $R_{FLAT (ON)}$		3.5	6.5	Ω	V_S = 0 V to 30 V, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)		±0.05	±10	nA	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 22
Drain Off Leakage, I_D (Off)		±0.1	±30	nA	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 22
Channel On Leakage, I_D (On), I_S (On)		±0.1	±30	nA	V_S = V_D = 1 V/30 V; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{INL} or I_{INH}		0.002		μA	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA	
Digital Input Capacitance, C_{IN}		6		pF	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$		180	289	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V
t_{ON} ($\overline{EN}$)		176	268	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V; see Figure 30
t_{OFF} ($\overline{EN}$)		98	129	ns	R_L = 300 Ω, C_L = 35 pF, V_S = 18 V; see Figure 30
Break-Before-Make Time Delay, t_D	21	50		ns	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 18 V; see Figure 29
Charge Injection, Q_{INJ}		150		pC	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Channel-to-Channel Crosstalk		−60		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 24
Total Harmonic Distortion + Noise		0.4		%	R_L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 26
−3 dB Bandwidth		135		MHz	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss		−1		dB	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)		18		pF	V_S = 18 V, f = 1 MHz
C_D (Off)		28		pF	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)		46		pF	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}		80		μA	Digital inputs = 0 V or V_{DD}
		100	130	μA	
V_{DD}	9		40	V	GND = 0 V, V_{SS} = 0 V

[1] Typical specifications represent average readings at 25°C.
[2] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V	80	58	36	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V	85	63	39	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V	63	45	28	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V	83	60	37	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	280 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

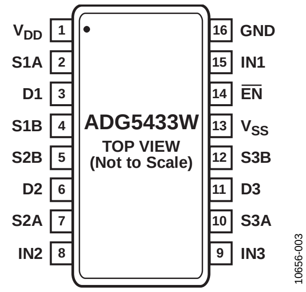

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	S1A	Source Terminal 1A. This pin can be an input or an output.
3	D1	Drain Terminal 1. This pin can be an input or an output.
4	S1B	Source Terminal 1B. This pin can be an input or an output.
5	S2B	Source Terminal 2B. This pin can be an input or an output.
6	D2	Drain Terminal 2. This pin can be an input or an output.
7	S2A	Source Terminal 2A. This pin can be an input or an output.
8	IN2	Logic Control Input 2.
9	IN3	Logic Control Input 3.
10	S3A	Source Terminal 3A. This pin can be an input or an output.
11	D3	Drain Terminal 3. This pin can be an input or an output.
12	S3B	Source Terminal 3B. This pin can be an input or an output.
13	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin must be connected to ground.
14	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, the INx logic inputs determine the on switches.
15	IN1	Logic Control Input 1.
16	GND	Ground (0 V) Reference.

Table 8. Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X[1]	Off	Off
0	0	Off	On
0	1	On	Off

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

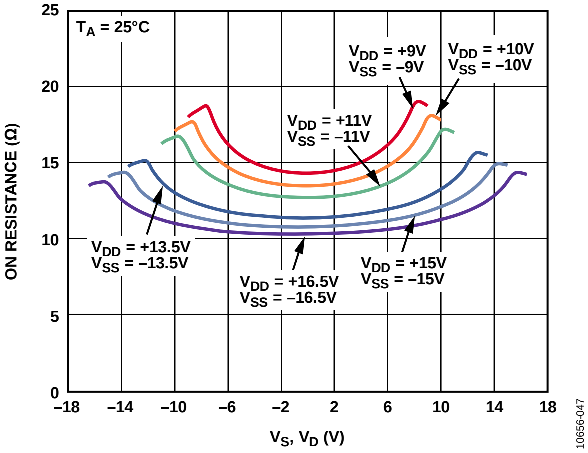

Figure 3. On Resistance as a Function of V_S, V_D (Dual Supply)

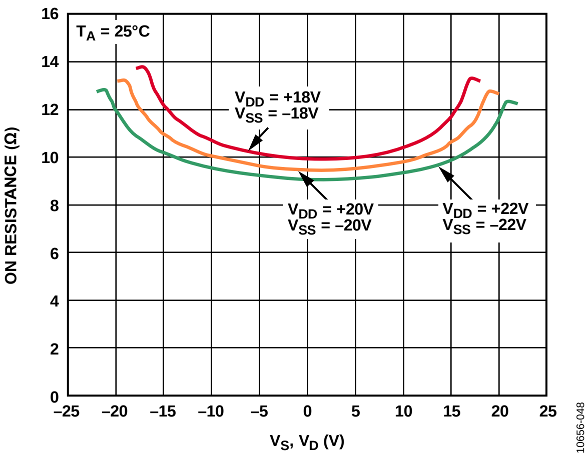

Figure 4. On Resistance as a Function of V_S, V_D (Dual Supply)

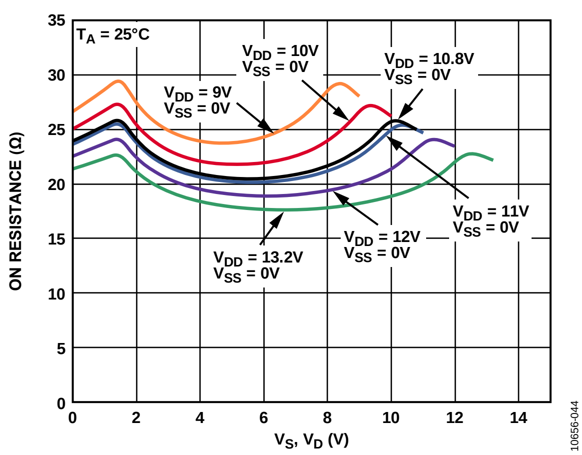

Figure 5. On Resistance as a Function of V_S, V_D (Single Supply)

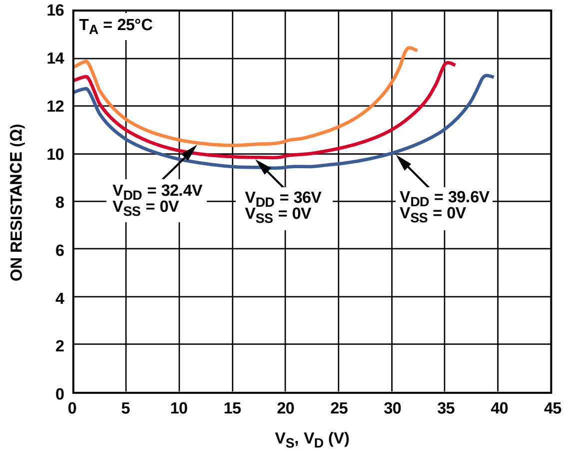

Figure 6. On Resistance as a Function of V_S, V_D (Single Supply)

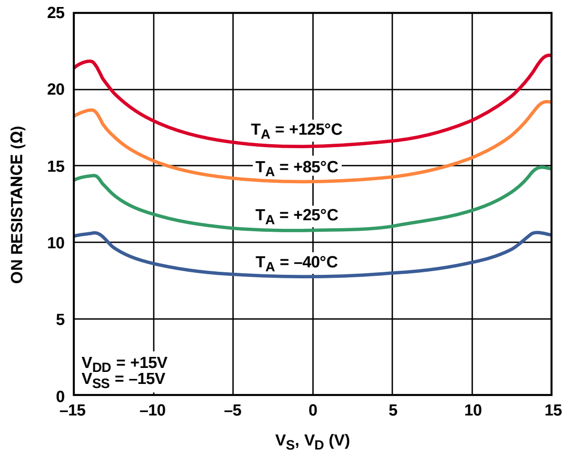

Figure 7. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

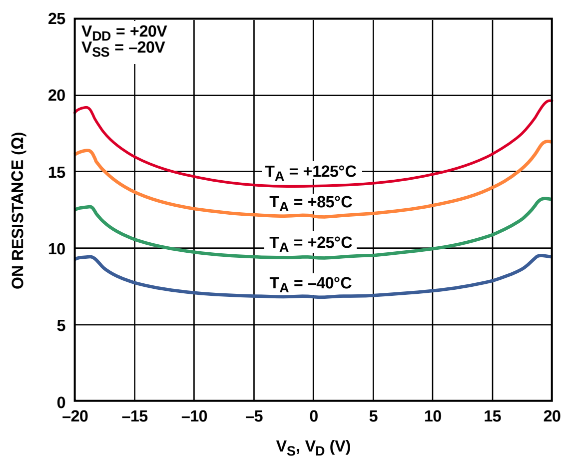

Figure 8. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

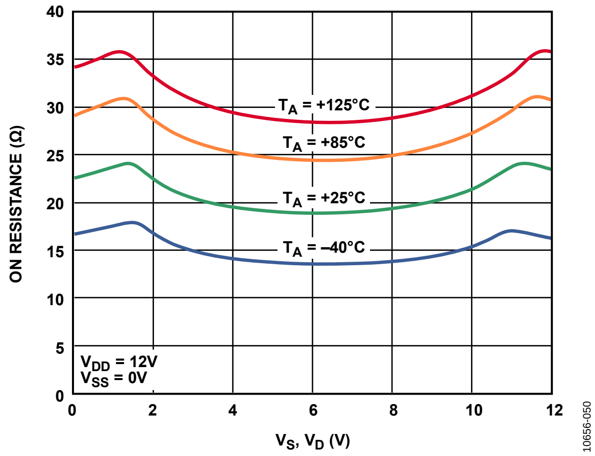

Figure 9. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

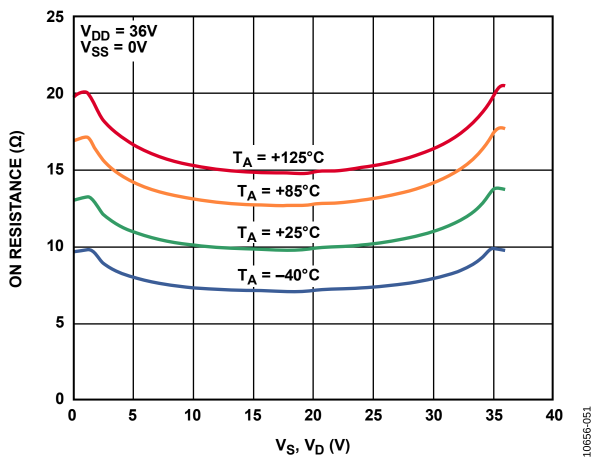

Figure 10. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

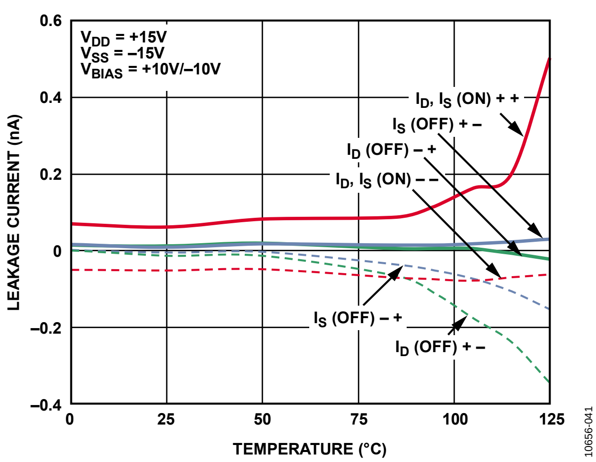

Figure 11. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

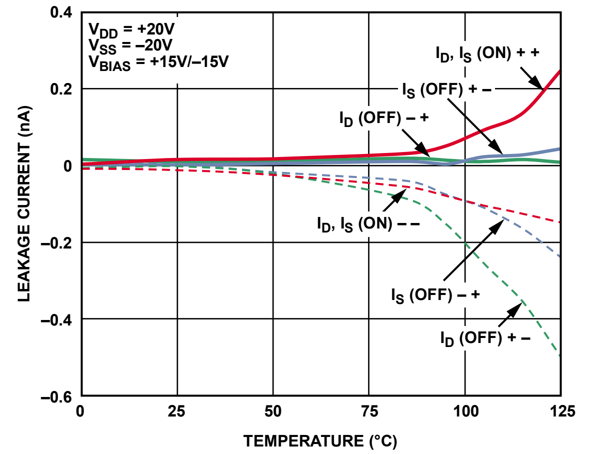

Figure 12. Leakage Currents as a Function of Temperature, ±20 V Dual Supply

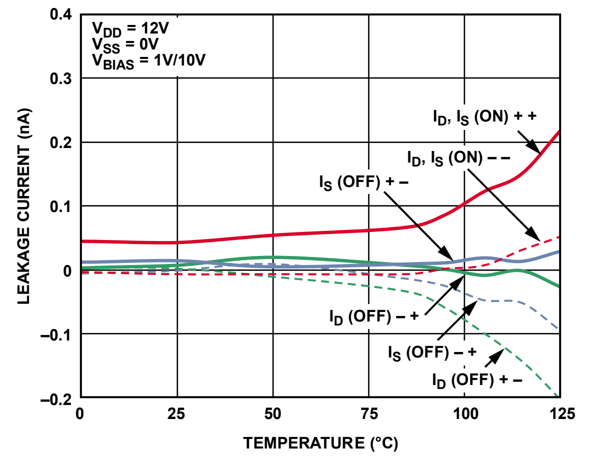

Figure 13. Leakage Currents as a Function of Temperature, 12 V Single Supply

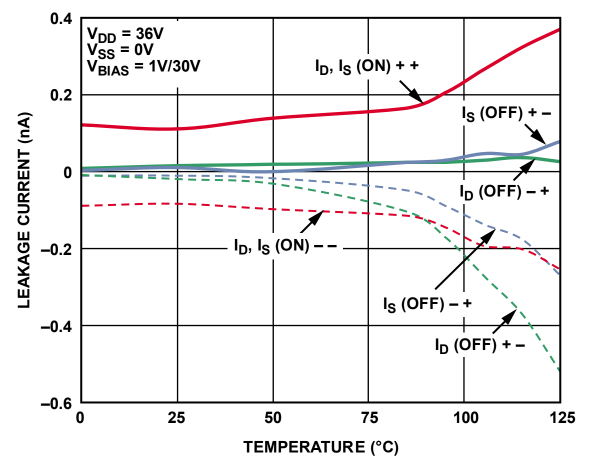

Figure 14. Leakage Currents as a Function of Temperature, 36 V Single Supply

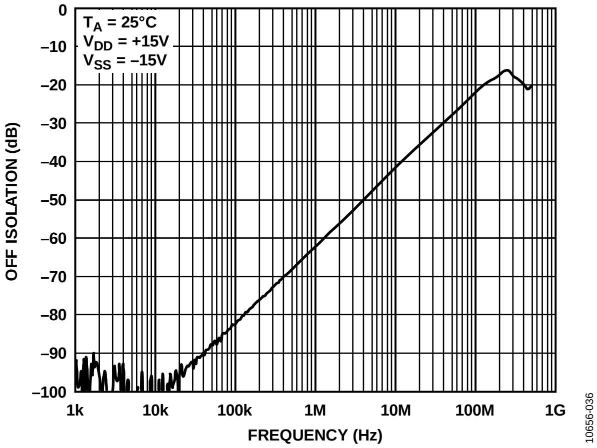

Figure 15. Off Isolation vs. Frequency

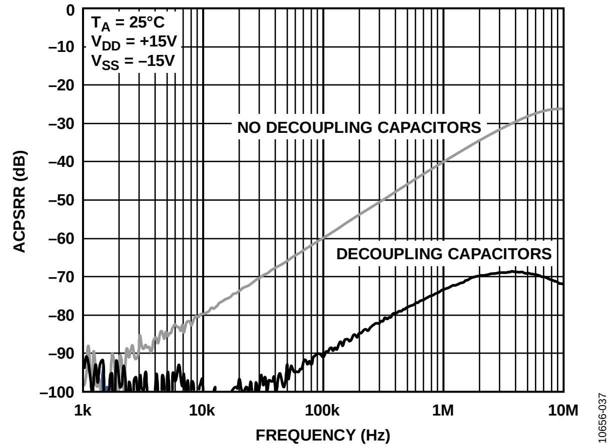

Figure 18. ACPSRR vs. Frequency

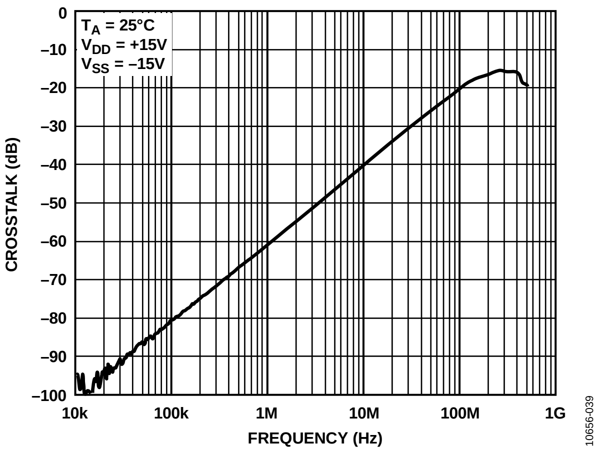

Figure 16. Crosstalk vs. Frequency

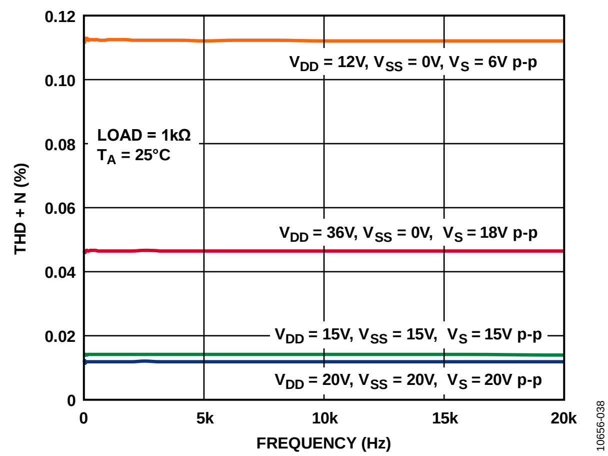

Figure 19. THD + N vs. Frequency

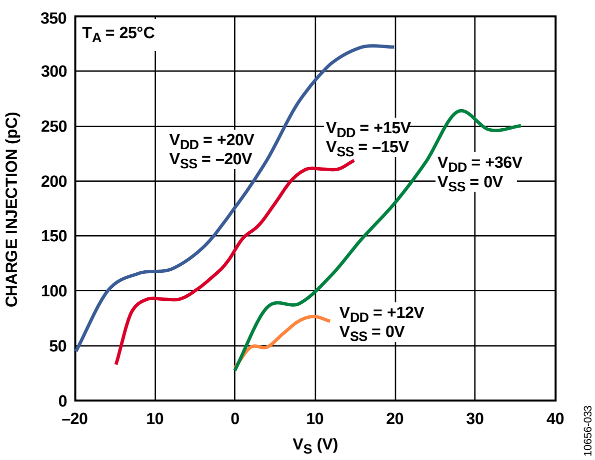

Figure 17. Charge Injection vs. Source Voltage

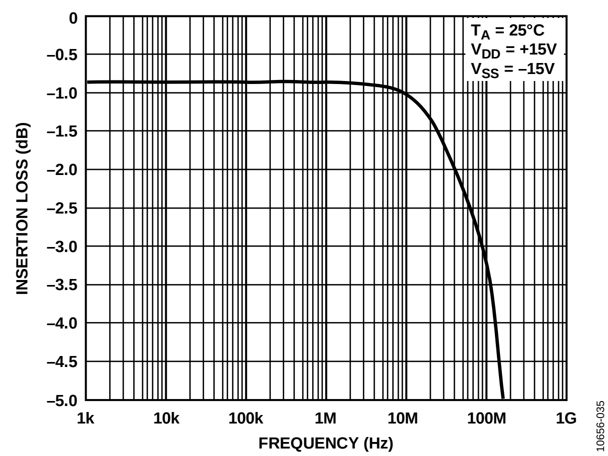

Figure 20. Bandwidth

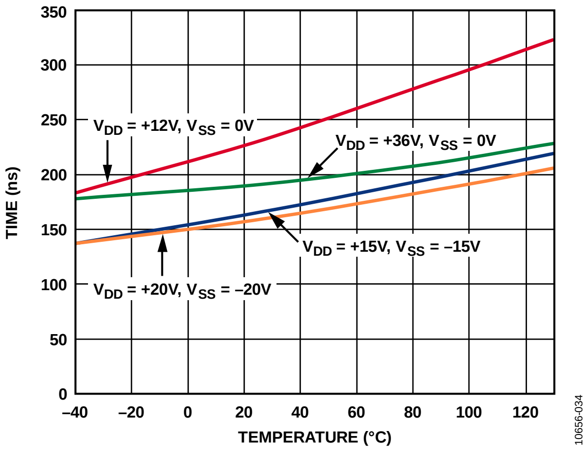

Figure 21. $t_{TRANSITION}$ Times vs. Temperature

TEST CIRCUITS

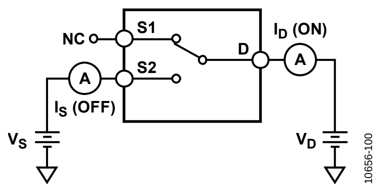

Figure 22. On and Off Leakage

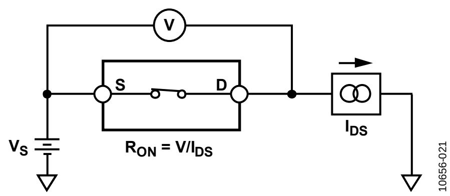

Figure 23. On Resistance

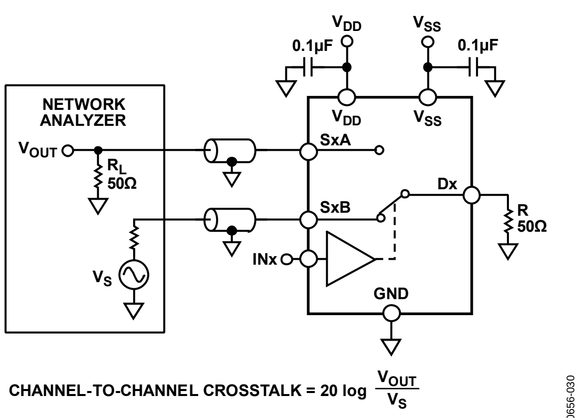

Figure 24. Channel-to-Channel Crosstalk

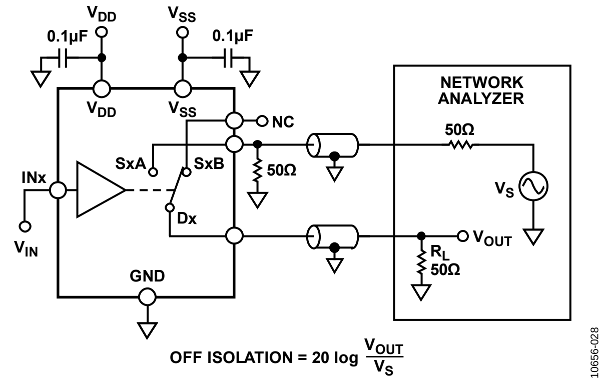

Figure 25. Off Isolation

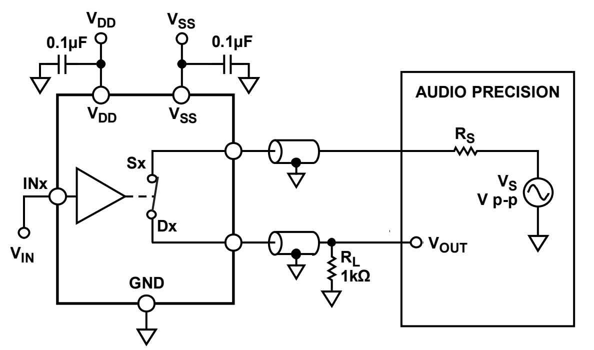

Figure 26. THD + Noise

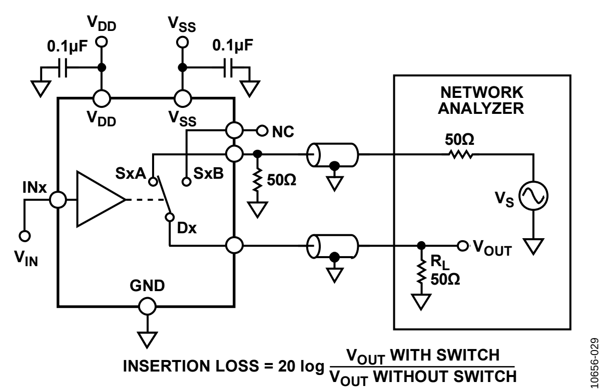

Figure 27. Bandwidth

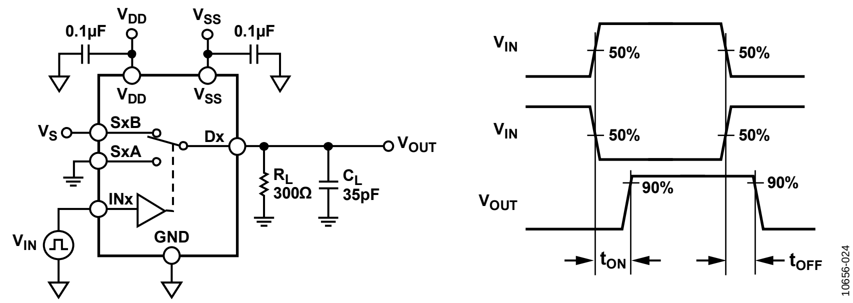

Figure 28. Switching Timing

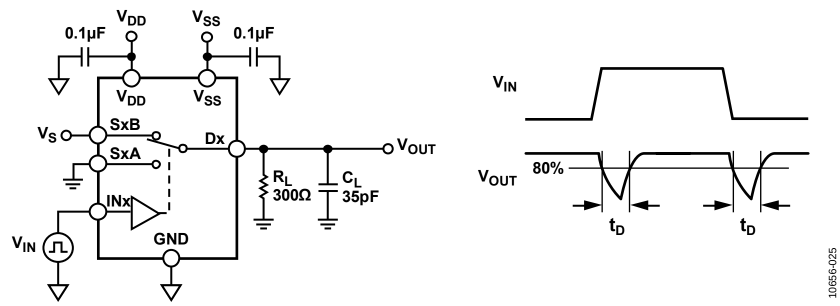

Figure 29. Break-Before-Make Delay, t_D

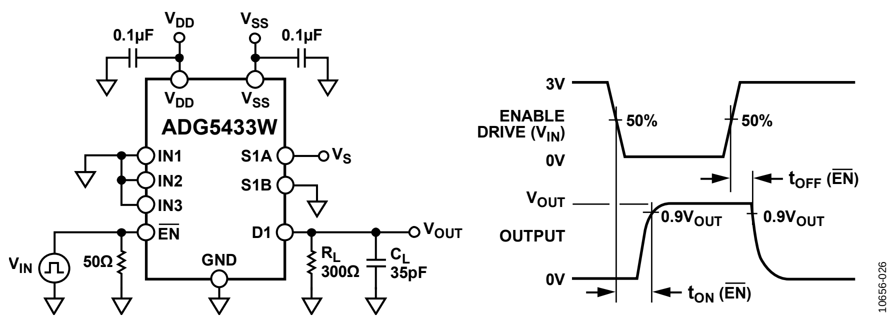

Figure 30. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

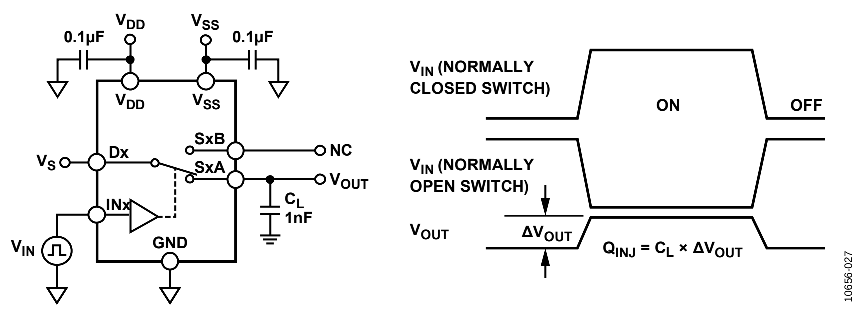

Figure 31. Charge Injection

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents digital input capacitance.

t_{ON} ($\overline{EN}$)
t_{ON} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)
t_{OFF} ($\overline{EN}$) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5433W, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

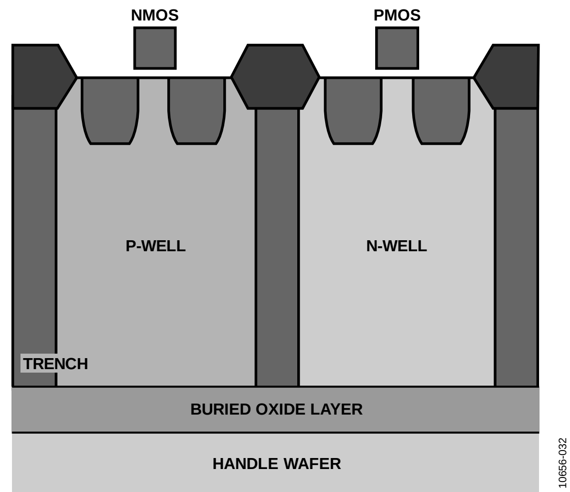

Figure 32. Trench Isolation

APPLICATIONS INFORMATION

The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5433W high voltage switch allows single-supply operation from 9 V to 40 V and dual supply operation from ±9 V to ±22 V. The ADG5433W (as well as other select devices within this family) achieves 8 kV human body model ESD ratings, which provide a robust solution eliminating the need for separate protect circuitry designs in some applications.

OUTLINE DIMENSIONS

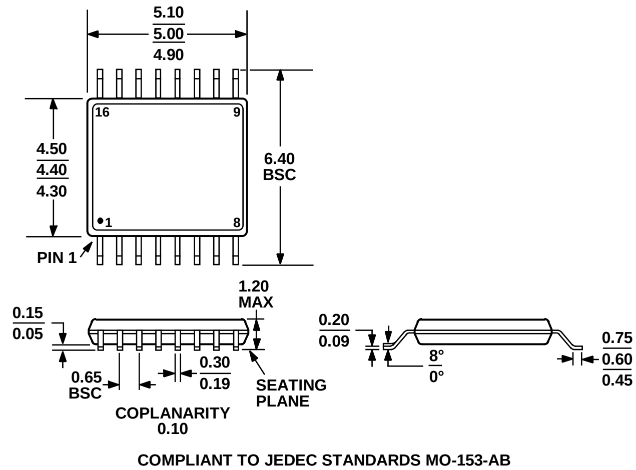

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Description	Package Option
ADG5433WBRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5433WBRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADG5433W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES