Approval Sheet

Customer	
Product Number	**M1SF-1GMCVC03-J**
Module speed	**PC-3200**
Pin	**200 pin**
CAS Latency	**CL-3**
Operating Temp	**0 ℃ ~ 70 ℃**
Date	**16th March 2018**

Rev 1.2

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-3200	**F**	266	333	400	15	15	55

- JEDEC Standard 200-pin Small Outline Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8μs ($T_A \leq +70°C$)
- SDRAM Operation Temperature
  - $-0°C \leq T_A \leq +70°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5, 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

DDR SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to 65	°C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	kPa	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
Following JEDEC specifications.

3. Ordering Information

DDR SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1SF-1GMCVC03-J	1GB	PC-3200	128M x64	16	2	N/A

4. Pin Assignments and Descriptions

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	/CK1
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	/RAS	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	/WE	120	/CAS	169	DQS6	170	DM6
21	VDD	22	VDD	71	CB0	72	CB4	121	/S0	122	/S1	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	A13	124	DU	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	DU (/RESET)	135	DQ34	136	DQ38	185	VSS	186	VSS
37	K0	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	CK2	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	/CK2	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	VDDSPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	VSS	150	VSS	199	VSSID	200	NC,TEST

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.
Note: Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.
Note: Pins 89, 91are reserved for x72 modules or registered modules.

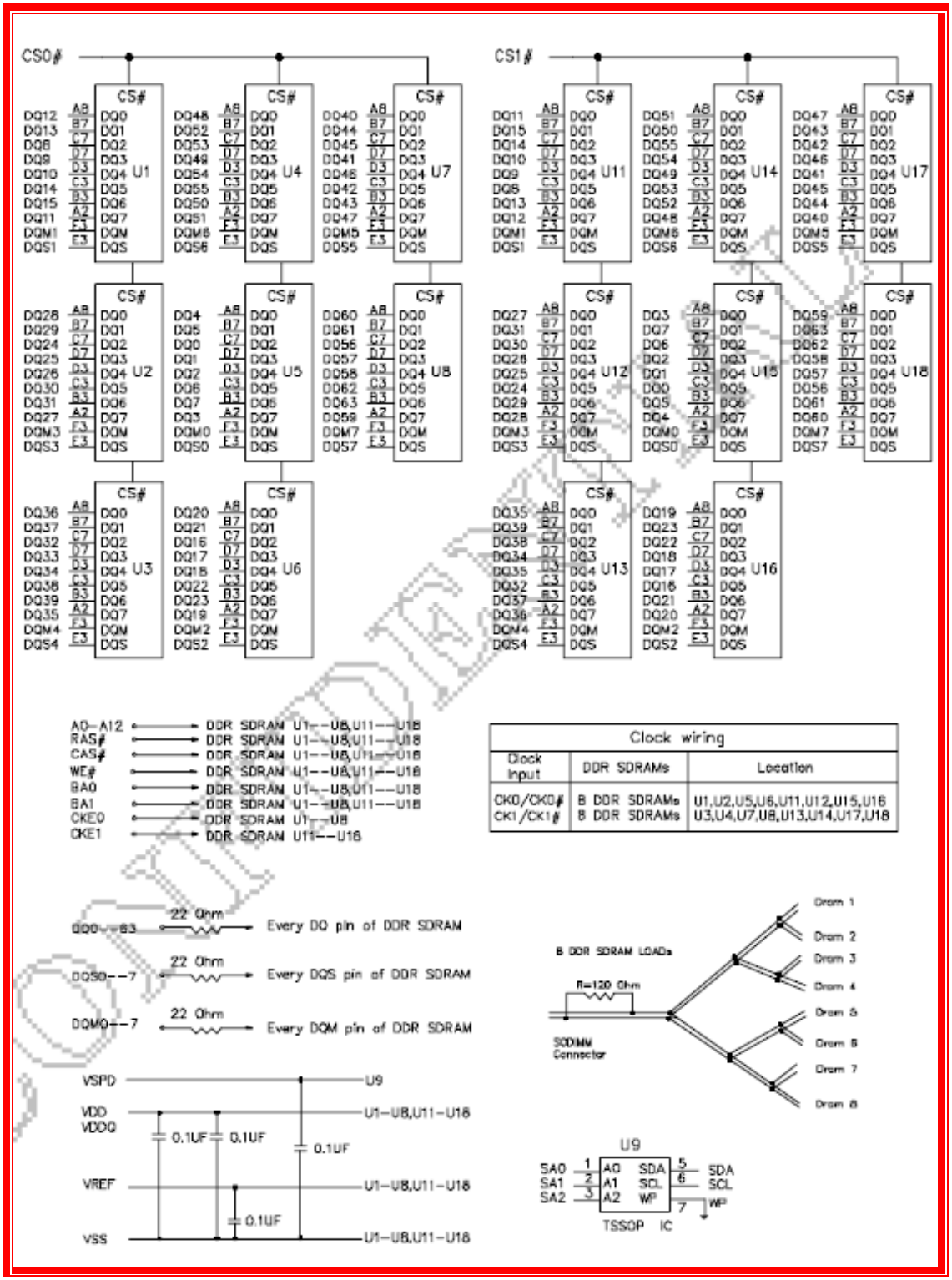
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
CK[0:2]	Clock Inputs, positive line	SA(0:2)	SPD address
/CK[0:2]	Clock inputs, negative line	DQ[63:0]	Data Input/Output
CKE[0:1]	Clock Enables	CB[7:0]	Data check bits Input/Output
/RAS	Row Address Strobe	DM(0:8)	Data Masks
/CAS	Column Address Strobe	DQS(0:8)	Data strobes
/WE	Write Enable	V_{DD}	Core and I/O Power
/S[0:1]	Chip Selects	V_{SS}	Ground
A(0:9,11:13)	Address Inputs	V_{REF}	Input/Output Reference
A10,AP	Address Input/Autoprecharge	V_{DD}SPD	SPD Power
BA(0:1)	SDRAM Bank Address	TEST	Reserved for test equipment use
SCL	Serial Presence Detect (SPD) Clock Input	DU	Reserved for future use
SDA	SPD Data Input/Output		

6. Function Block Diagram:

- (1GB, 2 Ranks, 64Mx8 DDR SDRAM base SODIMM)



7. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-55	150	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0	3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5	VDDQ+0.5	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0	3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0	3.6	V
I_{OS}	Output short Circuit Current		50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

AC Input Operating Conditions

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	1
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} - 0.31	V	1
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	2
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} - 0.2	0.5* V_{DDQ} + 0.2	V	3
$V_{REF(AC)}$	I/O reference voltage	0.49*V_{DDQ}	0.51*V_{DDQ}	V	4

Note:

1. VIH overshoot: VIH,max = VDDQ + 1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL,min = –1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.
2. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
3. The value of VIX and VMP is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
4. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed ±2% of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	1
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	1
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	1
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	1
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	VREF + 0.15	-	VDD + 0.3	V	2
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	VREF - 0.15	V	2
V_{TT}	Termination Voltage	VREF-0.04		VREF+0.04	V	3
I_I	Input leakage current:	-2		2	uA	
V_{REF}	I/O Reference Voltage	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	VDDQ + 0.3	V	4
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	VDDQ + 0.6	V	4,5

Note:

1. VDD and VDDQ must track each other.
2. To maintain a valid level, the transitioning edge of the input must:
   Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
   Reach at least the target AC level.
   After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, it is expected to be set equal to VREF, and it must track variations in the DC level of VREF.
4. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed ±2% of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.
5. VID is the magnitude of the difference between the input level on CK and the input level on CK#.

9. Operating, Standby, and Refresh Currents

- 1GB SODIMM (2 Rank, 64Mx8 DDR SDRAMs)

Symbol	Parameter/Condition	PC-3200	Unit
I DD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	mA
I DD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1360	mA
I DD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	80	mA
I DD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	368	mA
I DD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	288	mA
I DD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	640	mA
I DD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	1920	mA
I DD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1920	mA
I DD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1920	mA
I DD6	CKE=<0.2V; External clock on; tCK=tCK(min)	80	mA
I DD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	3680	mA

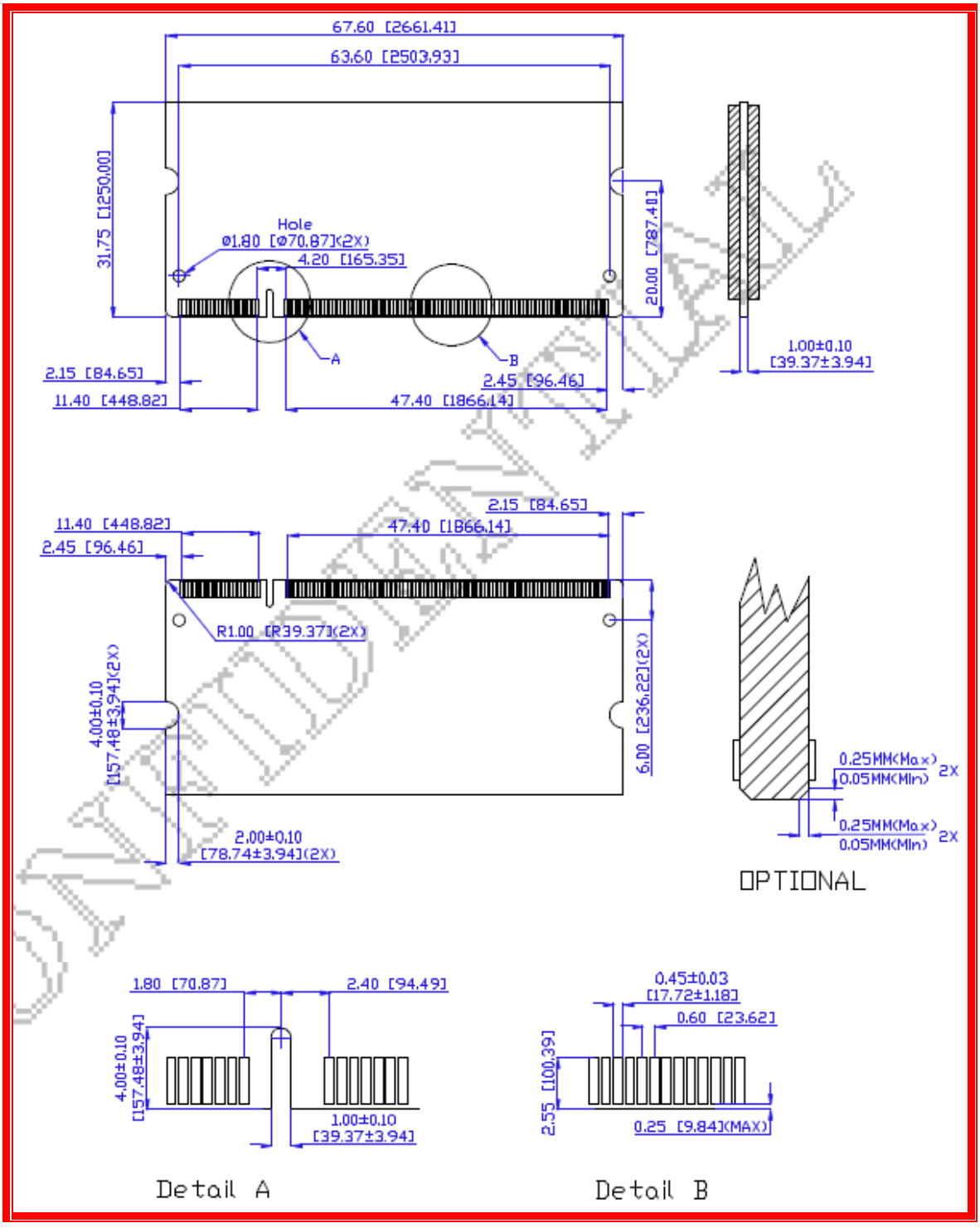
10. AC Timing Specifications

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.60	0.60	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	7.5	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-	0.7	ns
tLZ	Data-out Low-Z window from CK/CK#	-0.7	-	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP –tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.72	1.28	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK
tMRD	Mode register set command cycle time	10	-	ns
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.25		tCK
tIH	Address and control input hold time	0.6	-	ns
tIS	Address and control input setup time	0.6	-	ns

t_{RPRE}	Read preamble	0.9	1.1	t_{CK}
t_{RPST}	Read postamble	0.4	0.6	t_{CK}
t_{RRD}	Active bank A to Active bank B command	10	-	ns
t_{REFI}	Average Periodic Refresh Interval	-	7.8	µs
t_{WR}	Write recovery time without Auto-Precharge	15		ns
t_{WTR}	Internal write to read command delay	2	-	t_{CK}
t_{XSNR}	Exit self refresh to a Non-read command	70	-	ns
t_{XSRD}	Exit self refresh to a Read command	200	-	t_{CK}

11. PACKAGE DIMENSION

- (1GB, 2 Ranks, 64Mx8 DDR SDRAMs)



Note: All dimensions are in millimeters and should be kept within a tolerance of ±0.15, unless otherwise specified.

12. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

13. Revision Log

Rev	Date	Modification
0.1	28th July 2014	Preliminary Edition
1.0	28th July 2014	Official Released.
1.1	23rd December 2016	Modified page 10 (9. Operating, Standby, and Refresh Currents)
1.2	16th March 2018	Updated RoHS