SPICE Device Model Si4190ADY



Vishay Siliconix

N-Channel 100 V (D-S) MOSFET

DESCRIPTION

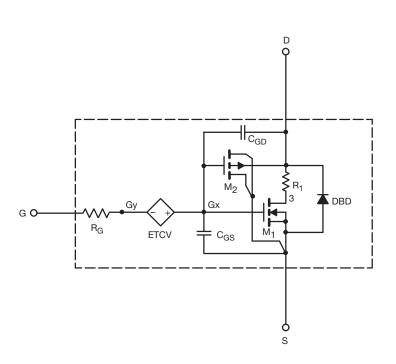
The attached spice model describes the typical electrical characteristics of the N-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2.1	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	0.0075	0.0073	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	0.0098	0.0096	
Forward Transconductance ^a	g fs	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	51	54	S
Body Diode Voltage	V _{SD}	I _S = 5 A	0.75	0.76	V
Dynamic ^b				·	
Input Capacitance	C _{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	2020	1970	pF
Output Capacitance	C _{oss}		687	695	
Reverse Transfer Capacitance	C _{rss}		62	62	
Total Gate Charge	0	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	38	44.4	nC
	Qg	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	21	20.7	
Gate-Source Charge	Q _{gs}		6.1	6.1	
Gate-Drain Charge	Q _{gd}		9.1	9.1	

Notes

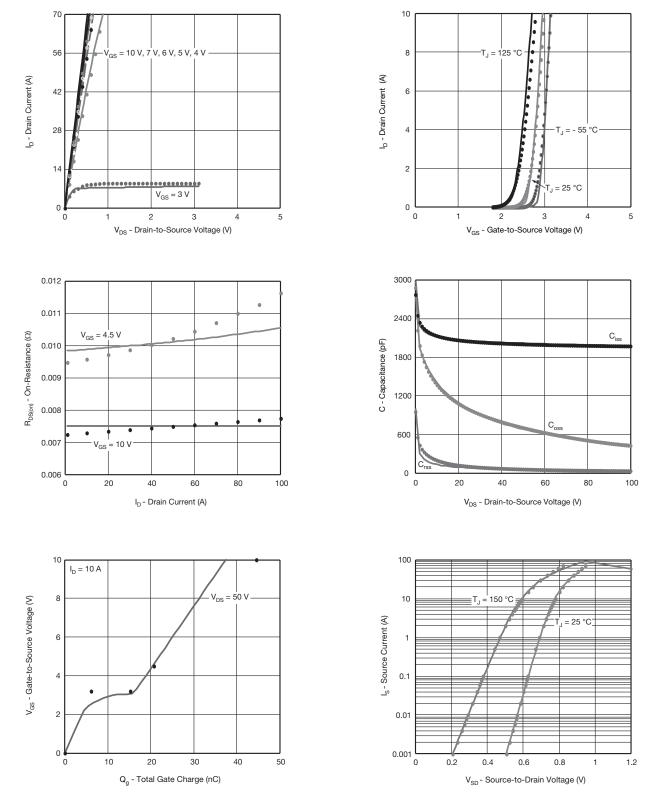
a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%.$

b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data.

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