OPA656 Wideband, Unity-Gain Stable, FET-Input Operational Amplifier

1 Features

- 500 MHz Unity-gain Bandwidth
- Low Input Bias Current: 2 pA
- Low Offset And Drift: ±250 µV, ±2 µV/°C
- Low Distortion: 74-dB SFDR at 5 MHz
- High-Output Current: 70 mA
- Low Input Voltage Noise: 7 nV/√Hz

2 Applications

- Wideband Photodiode Amplifiers
- Sample-and-Hold Buffers
- CCD Output Buffers
- ADC Input Buffers
- Wideband Precision Amplifiers
- Test and Measurement Front Ends

3 Description

The OPA656 device combines a very wideband, unity-gain stable, voltage-feedback operational amplifier with a FET-input stage to offer an ultra high dynamic-range amplifier for Analog-to-Digital Converter (ADC) buffering and transimpedance applications. Extremely low DC errors give good precision in optical applications.

The high unity-gain stable bandwidth and JFET input allows exceptional performance in high-speed, low-noise integrators.

The high input impedance and low bias current provided by the FET input is supported by the ultra-low 7-nV/√Hz input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

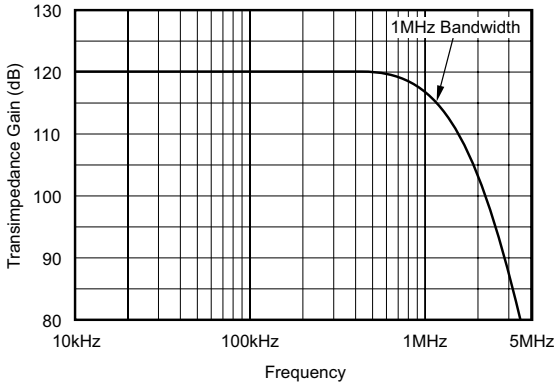
Broad transimpedance bandwidths are achievable given the OPA656 device's high 230-MHz gain bandwidth product. As shown below, a –3-dB bandwidth of 1 MHz is provided even for a high 1-MΩ transimpedance gain from a 47-pF source capacitance.

Device Information(1)

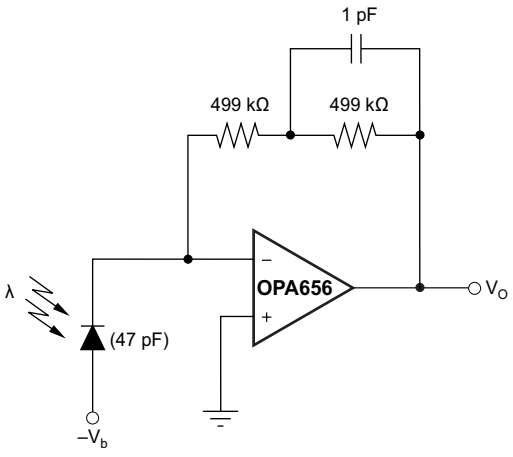
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA656	SOIC (8)	2.90 mm × 1.60 mm
	SOT-23 (5)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1-MΩ Transimpedance Bandwidth



Wideband Photodiode Transimpedance Amplifier



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2008) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision F (March 2006) to Revision G — **Page**

- Changed Storage Temperature Range from –40°C to 125°C to –65°C to 12°C ... 4
- Deleted in the DC Performance section: Drift from Input Offset Current specifications ... 6

Changes from Revision E (March 2006) to Revision F — **Page**

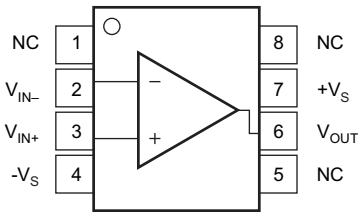
- Added Design-In Tools paragraph and table ... 23

5 Related Operational Amplifier Products

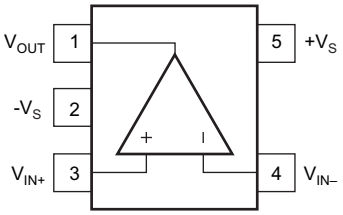
DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA656	±5	230	290	7	Unity-Gain Stable FET-Input
OPA657	±5	1600	700	4.8	Gain of +7 stable FET Input
OPA659	±6	350	2550	8.9	Unity-Gain Stable FET-Input
LMH6629	5	4000	1600	0.69	Gain of +10 stable Bipolar Input
THS4631	±15	210	1000	7	Unity-Gain Stable FET-Input
OPA857	5	4750	220	—	Programmable Gain (5 kΩ / 20 kΩ) Transimpedance Amplifier

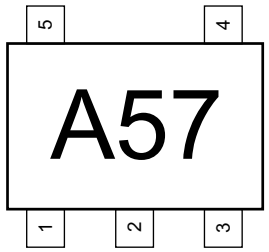
6 Pin Configuration and Functions

D Package
8-Pin SOIC Surface-Mount
Top View



DBV Package
5-Pin SOT-23
Top View





Pin Orientation/Package Marking

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
NC	1	—	—	No Connection
	5			
	8			
V_{IN-}	2	4	I	Inverting Input
V_{IN+}	3	3	I	Noninverting Input
$-V_S$	4	2	POW	Negative Power Supply
V_{OUT}	6	1	O	Output of amplifier
$+V_S$	7	5	POW	Positive Power Supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage (Total Bipolar Supplies)		±6.5	V
Internal power dissipation	See *Thermal Information*		
Differential input voltage	$-V_S$	$+V_S$	
Input voltage	$-V_S$	$+V_S$	
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	8	10	12	V
T_A	Ambient temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC (1)		OPA656		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.2	140.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.9	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.2	24.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.4	61.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

R_F = 250 Ω, R_L = 100 Ω, and G = 2 V/V, unless otherwise noted. See Figure 1 for AC performance.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE (Figure 29)							
Small-Signal Bandwidth	G = +1 V/V, V_O = 200 mV_{PP}, R_F = 0 Ω	T_J = 25°C(2)	C		500		MHz
	G = +2 V/V, V_O = 200 mV_{PP}	T_J = 25°C(2)	C		200		MHz
	G = +5 V/V, V_O = 200 mV_{PP}	T_J = 25°C(2)	C		59		MHz
	G = +10 V/V, V_O = 200 mV_{PP}	T_J = 25°C(2)	C		23		MHz
Gain-Bandwidth Product	G > +10 V/V	T_J = 25°C(2)	C		230		MHz
Bandwidth for 0.1-dB flatness	G = +2 V/V, V_O = 200 mV_{PP}	T_J = 25°C(2)	C		30		MHz
Peaking at a Gain of +1	V_O < 200 mV_{PP}, R_F = 0 Ω	T_J = 25°C(2)	C		1.5		dB
Large-Signal Bandwidth	G = +2 V/V, V_O = 2 V_{PP}	T_J = 25°C(2)	C		75		MHz
Slew Rate	G = +2 V/V, 1-V Step	T_J = 25°C(2)	C		290		V/µs
Rise-and-Fall Time	0.2-V Step	T_J = 25°C(2)	C		1.5		ns
Settling Time to 0.02%	G = +2 V/V, V_O = 2-V Step	T_J = 25°C(2)	C		21		ns
Harmonic Distortion	G = +2 V/V, f = 5 MHz, V_O = 2 V_{PP}						
2nd-Harmonic	R_L = 200 Ω	T_J = 25°C(2)	C		–71		dBc
	R_L > 500 Ω	T_J = 25°C(2)			–74		
3rd-Harmonic	R_L = 200 Ω	T_J = 25°C(2)	C		–81		dBc
	R_L > 500 Ω	T_J = 25°C(2)			–100		
Input Voltage Noise	f > 100 kHz	T_J = 25°C(2)			7		nV/√Hz
Input Current Noise	f > 100 kHz	T_J = 25°C(2)	C		1.3		fA/√Hz
Differential Gain	G = +2 V/V, PAL, R_L = 150 Ω	T_J = 25°C(2)	C		0.02%		
Differential Phase	G = +2 V/V, PAL, R_L = 150 Ω	T_J = 25°C(2)	C		0.05		
DC PERFORMANCE(3)							
Open-Loop Voltage Gain (AOL)	V_O = 0 V, R_L = 100 Ω	T_J = 25°C(2)	A	60	65		dB
		T_J = 0°C to +70°C(4)		59			
		T_J = –40°C to +85°C(4)		58			
Input Offset Voltage	V_{CM} = 0 V	T_J = 25°C(2)	A		±0.25	±1.8	mV
		T_J = 0°C to +70°C(4)				±2.2	
		T_J = –40°C to +85°C(4)				±2.6	
Average Offset Voltage Drift	V_{CM} = 0 V	T_J = 25°C(2)	A		±2	±12	µV/°C
		T_J = 0°C to +70°C(4)				±12	
		T_J = –40°C to +85°C(4)				±12	
Input Bias Current	V_{CM} = 0 V	T_J = 25°C(2)	A		±2	±20	pA
		T_J = 0°C to +70°C(4)				±1800	
		T_J = –40°C to +85°C(4)				±5000	
Input Bias Current	V_{CM} = 0 V	T_J = 25°C(2)	A		±2	±20	pA
		T_J = 0°C to +70°C(4)				±1800	
		T_J = –40°C to +85°C(4)				±5000	

(1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for 25°C min/max specifications.
(3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(4) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature minimum and maximum specifications.

Electrical Characteristics (continued)

R_F = 250 Ω, R_L = 100 Ω, and G = 2 V/V, unless otherwise noted. See Figure 1 for AC performance.

PARAMETER		TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Input Offset Current		V_{CM} = 0 V	T_J = 25°C(2)	B		±1	±10	pA
			T_J = 0°C to +70°C(4)				±900	
			T_J = –40°C to +85°C(4)				±2500	
INPUT								
Most Positive Input Voltage(5)			T_J = 25°C(2)	A	2.1	2.75		V
			T_J = 0°C to +70°C(4)		2.05			
			T_J = –40°C to +85°C(4)		2			
Most Negative Input Voltage(5)			T_J = 25°C(2)	A	–4	–4.5		V
			T_J = 0°C to +70°C(4)		–3.9			
			T_J = –40°C to +85°C(4)		–3.8			
Most Positive Input Voltage(6)			T_J = 25°C(2)	A	2.6	3.25		V
			T_J = 0°C to +70°C(4)		2.5			
			T_J = –40°C to +85°C(4)		2.4			
Most Negative Input Voltage(6)			T_J = 25°C(2)	A	–4	–4.5		V
			T_J = 0°C to +70°C(4)		–3.9			
			T_J = –40°C to +85°C(4)		–3.8			
Common-Mode Rejection Ratio (CMRR)		V_{CM} = ±0.5 V	T_J = 25°C(2)	A	80	86		dB
			T_J = 0°C to +70°C(4)		78			
			T_J = –40°C to +85°C(4)		76			
Input Impedance	Differential		T_J = 25°C(2)	C		10^{12} || 0.7		Ω || pF
	Common-Mode			C		10^{12} || 2.8		Ω || pF
OUTPUT								
Voltage Output Swing		No Load	T_J = 25°C(2)	A		±3.9 ±3.7		V
		R_L = 100 Ω	T_J = 25°C(2)	A	±3.3	±3.5		V
			T_J = 0°C to +70°C(4)		±3.2			
			T_J = –40°C to +85°C(4)		±3.1			
Current Output, Sourcing			T_J = 25°C(2)	A	50	70		mA
			T_J = 0°C to +70°C(4)		48			
			T_J = –40°C to +85°C(4)		46			
Current Output, Sinking			T_J = 25°C(2)	A	–50	–70		mA
			T_J = 0°C to +70°C(4)		–48			
			T_J = –40°C to +85°C(4)		–46			
Closed-Loop Output Impedance		G = +1 V/V, f = 0.1 MHz	T_J = 25°C(2)	C		0.01		Ω
POWER SUPPLY								
Specified Operating Voltage			T_J = 25°C(2)	C		±5		V
Maximum Operating Voltage Range			T_J = 25°C(2)	A			±6	V
			T_J = 0°C to +70°C(4)				±6	
			T_J = –40°C to +85°C(4)				±6	
Maximum Quiescent Current			T_J = 25°C(2)	A		14	16	mA
			T_J = 0°C to +70°C(4)				16.2	
			T_J = –40°C to +85°C(4)				16.3	
Minimum Quiescent Current			T_J = 25°C(2)	A	11.7	14		dB
			T_J = 0°C to +70°C(4)		11.4			
			T_J = –40°C to +85°C(4)		11.1			

(5) Tested <3dB below minimum specified CMRR at ±CMIR limits.
(6) Input range to give > 53-dB CMRR.

Electrical Characteristics (continued)

R_F = 250 Ω, R_L = 100 Ω, and G = 2 V/V, unless otherwise noted. See Figure 1 for AC performance.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.50 V to 5.50 V	T_J = 25°C(2)	A	72	76		mA
		T_J = 0°C to +70°C(4)		70			
		T_J = –40°C to +85°C(4)		68			
(–PSRR)	$–V_S$ = 4.50 V to –5.50 V	T_J = 25°C(2)	A	56	62		dB
		T_J = 0°C to +70°C(4)		54			
		T_J = –40°C to +85°C(4)		52			
TEMPERATURE RANGE							
Specified Operating Range: U,N Package	Junction-to-Ambient	T_J = 25°C(2)		–40		85	°C
Thermal Resistance, $θ_{JA}$							
U: SO-8		T_J = 25°C(2)			125		°C/W
N: SOT23-5		T_J = 25°C(2)			150		°C/W

7.6 Electrical Characteristics: V_S = ±5 V: High Grade DC Specifications

R_F = 250 Ω, R_L = 100 Ω, and G = +2 V/V, unless otherwise noted.(1)

PARAMETER	TEST CONDITIONS		TEST LEVEL(2)	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{CM} = 0 V	T_J = 25°C(3)	A	±0.6	±0.1		mV
		T_J = 0°C to +70°C(4)		±0.85			
		T_J = –40°C to +85°C(4)		±0.9			
Input Offset Voltage Drift	V_{CM} = 0 V	T_J = 25°C(3)	A		±2	±6	µV/°C
		T_J = 0°C to +70°C(4)				±6	
		T_J = –40°C to +85°C(4)				±6	
Input Bias Current	V_{CM} = 0 V	T_J = 25°C(3)	A		±1	±5	pA
		T_J = 0°C to +70°C(4)				±450	
		T_J = –40°C to +85°C(4)				±1250	
Input Offset Current	V_{CM} = 0 V	T_J = 25°C(3)	A		±0.5	±5	pA
		T_J = 0°C to +70°C(4)				±450	
		T_J = –40°C to +85°C(4)				±1250	
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5 V	T_J = 25°C(3)	A	88	95		dB
		T_J = 0°C to +70°C(4)		86			
		T_J = –40°C to +85°C(4)		84			
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.5 V to 5.5 V	T_J = 25°C(3)	A	74	78		dB
		T_J = 0°C to +70°C(4)		72			
		T_J = –40°C to +85°C(4)		70			
(–PSRR)	$–V_S$ = –4.5 V to –5.5 V	T_J = 25°C(3)	A	62	68		dB
		T_J = 0°C to +70°C(4)		60			
		T_J = –40°C to +85°C(4)		58			

(1) All other specifications are the same as the standard-grade.
(2) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation.
(3) Junction temperature = ambient for 25°C min/max specifications.M
(4) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature min/max specifications.

7.7 Typical Characteristics: V_S = ±5 V

T_A = 25°C, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, unless otherwise noted.

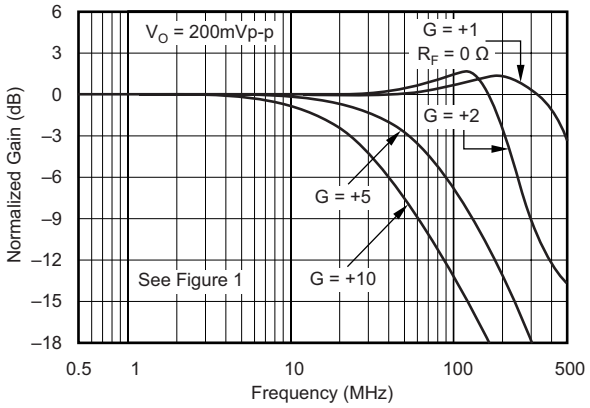


Figure 1. Noninverting Small-Signal Frequency Response

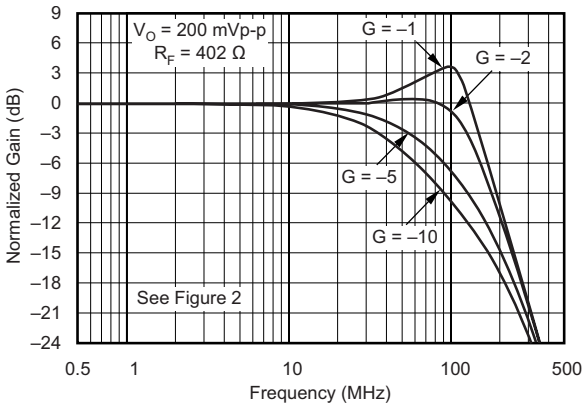


Figure 2. Inverting Small-Signal Frequency Response

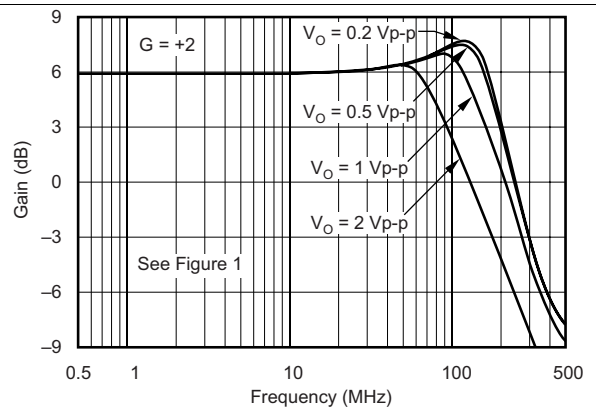


Figure 3. Noninverting Large-Signal Frequency Response

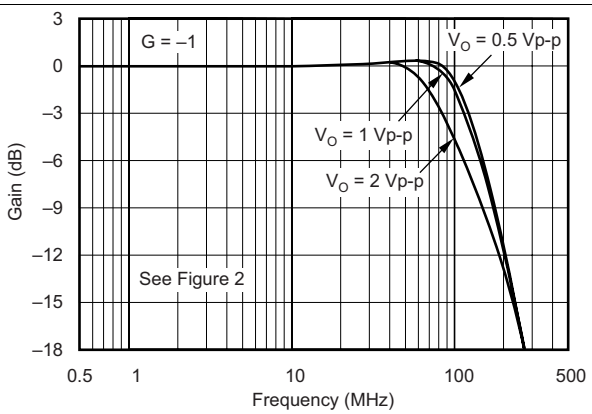


Figure 4. Inverting Large-Signal Frequency Response

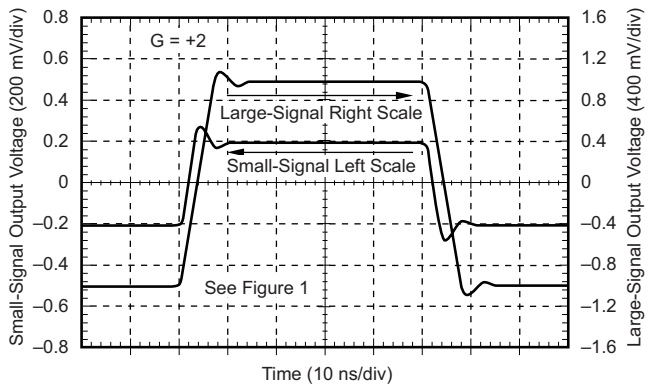


Figure 5. Noninverting Pulse Response

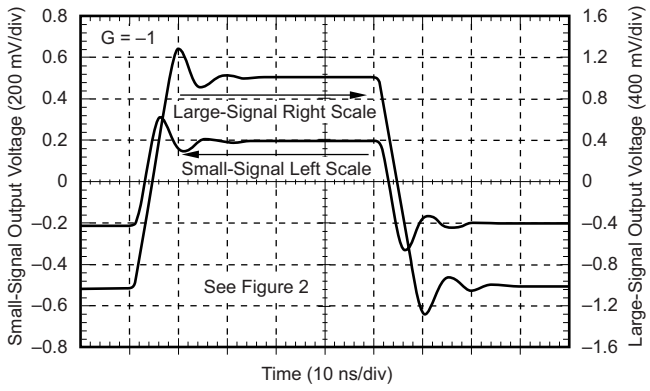


Figure 6. Inverting Pulse Response

Typical Characteristics: V_S = ±5 V (continued)

T_A = 25°C, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, unless otherwise noted.

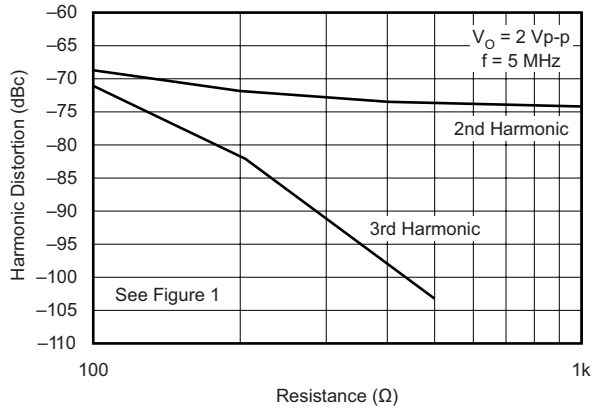


Figure 7. Harmonic Distortion vs Load Resistance

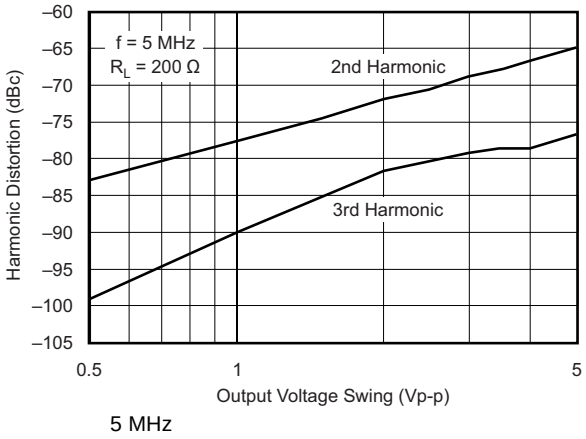


Figure 8. Harmonic Distortion vs Output Voltage

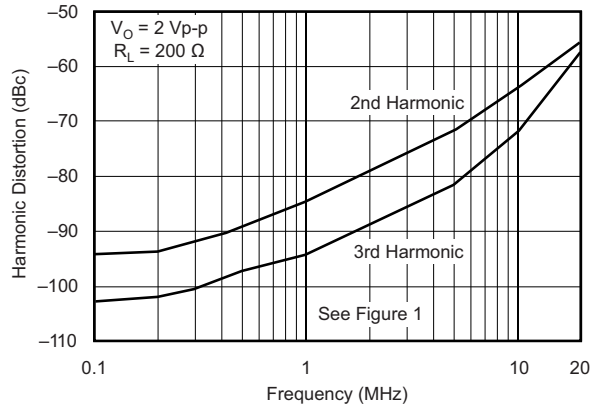


Figure 9. Harmonic Distortion vs Frequency

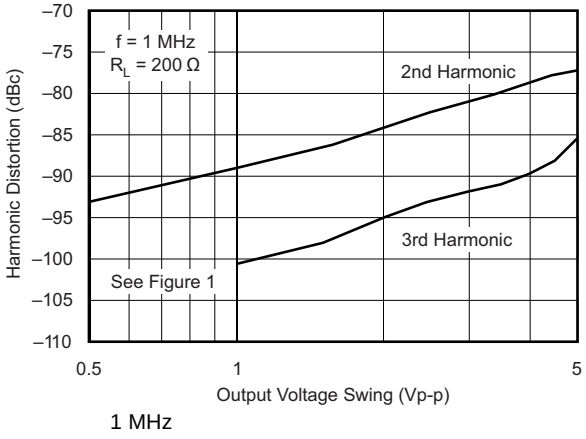


Figure 10. Harmonic Distortion vs Output Voltage

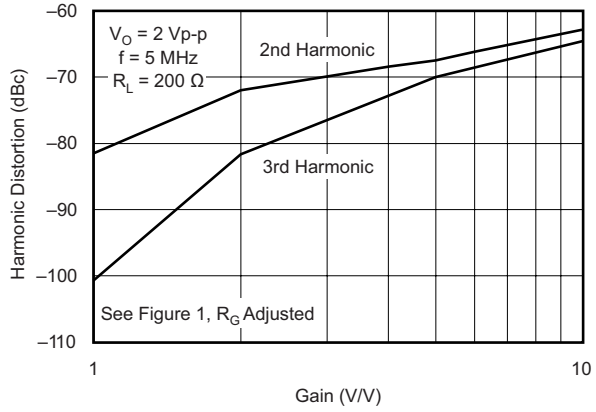


Figure 11. Harmonic Distortion vs Noninverting Gain

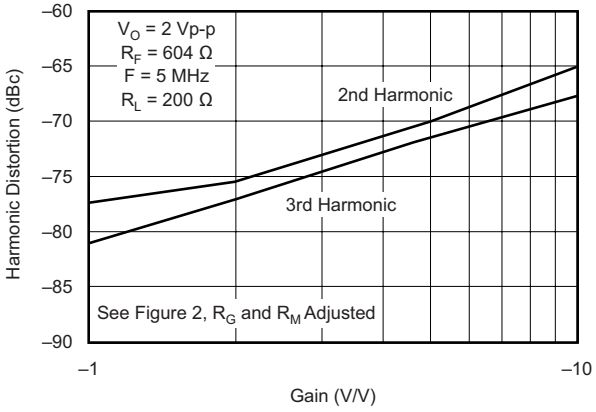


Figure 12. Harmonic Distortion vs Inverting Gain

Typical Characteristics: V_S = ±5 V (continued)

T_A = 25°C, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, unless otherwise noted.

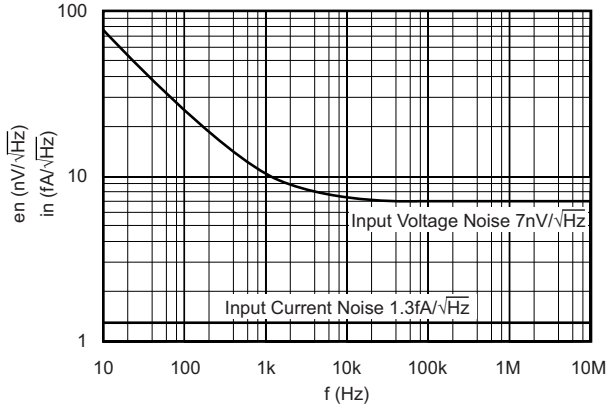


Figure 13. Input Current and Voltage Noise Density

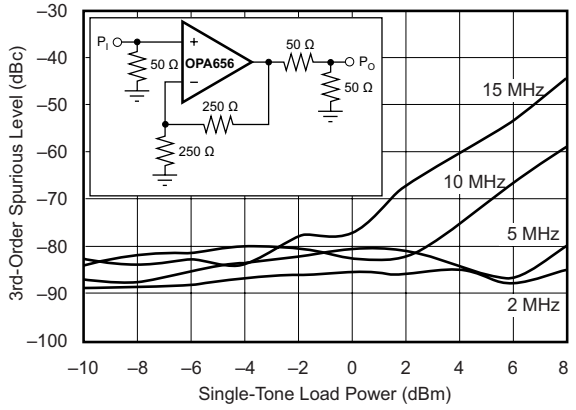


Figure 14. 2-Tone, 3rd-Order Intermodulation Spurious

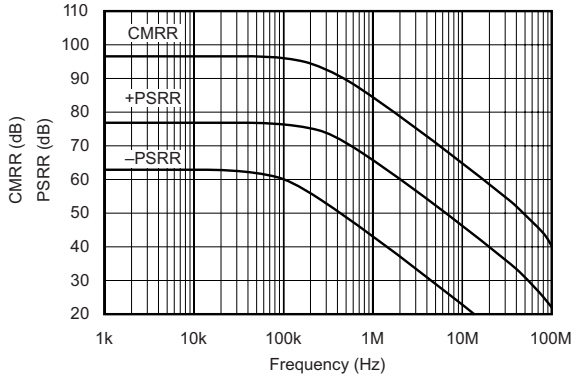


Figure 15. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

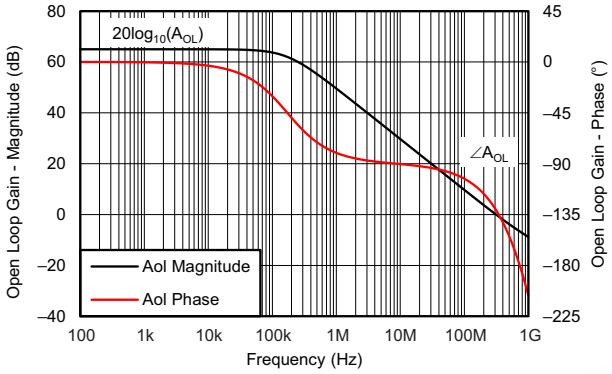


Figure 16. Open-Loop Gain and Phase

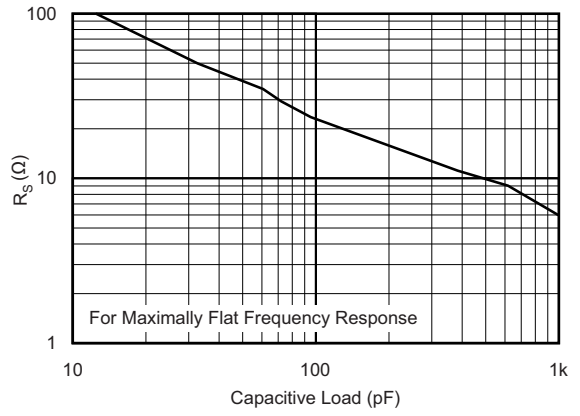


Figure 17. Recommended R_S vs Capacitive Load

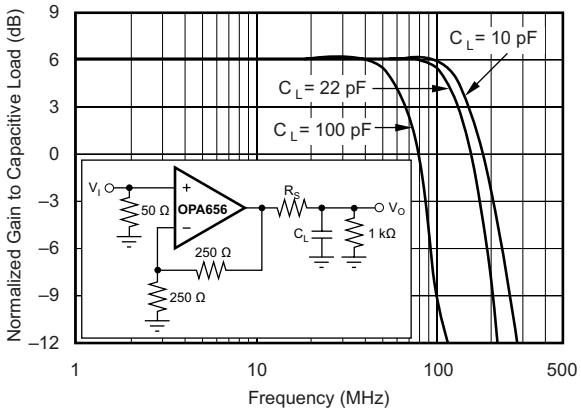


Figure 18. Frequency Response vs Capacitive Load

Typical Characteristics: V_S = ±5 V (continued)

T_A = 25°C, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, unless otherwise noted.

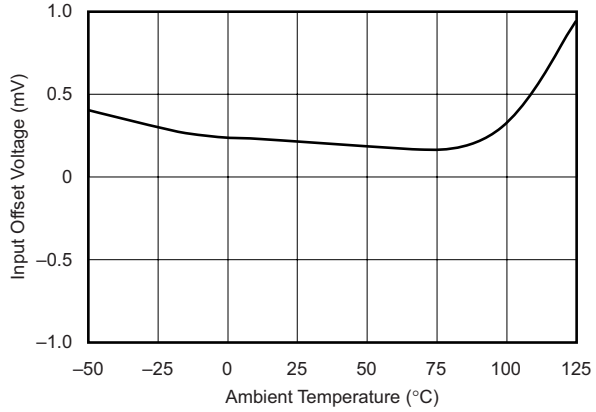


Figure 19. Typical Input Offset Voltage Over Temperature

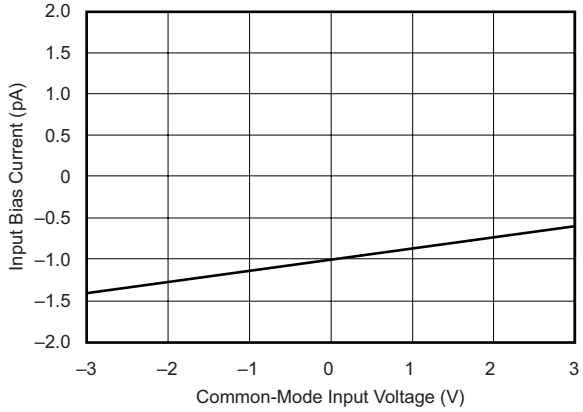


Figure 20. Typical Input Bias Current vs Common-Mode Input Voltage

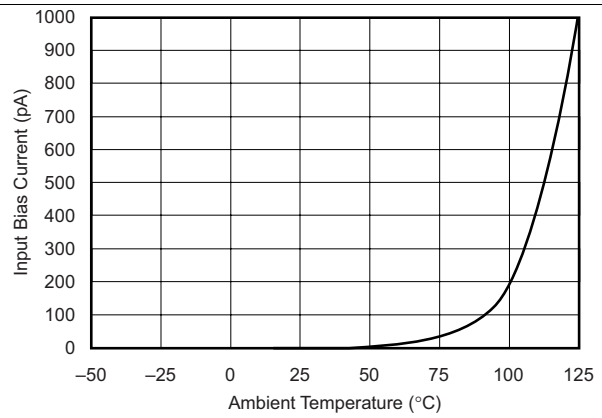


Figure 21. Typical Input Bias Current Over Temperature

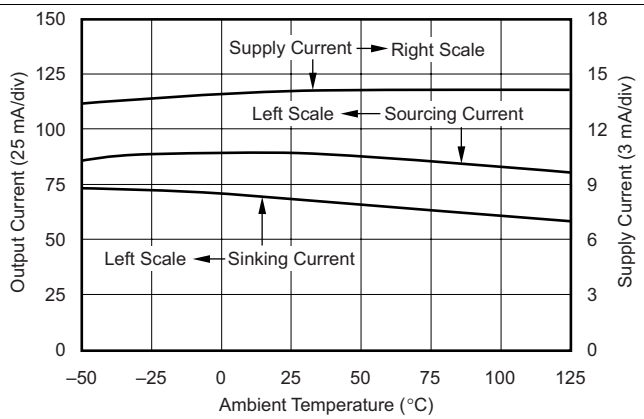


Figure 22. Supply and Output Current vs Temperature

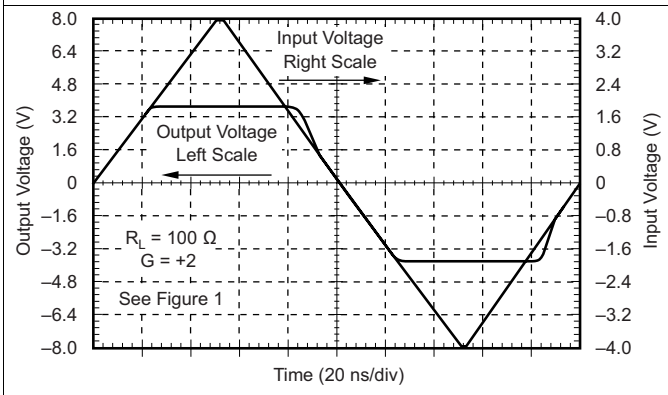


Figure 23. Noninverting Input Overdrive Recovery

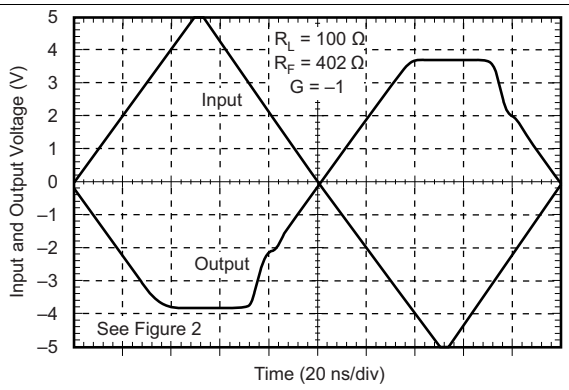


Figure 24. Inverting Overdrive Recovery

Typical Characteristics: V_S = ±5 V (continued)

T_A = 25°C, G = +2 V/V, R_F = 250 Ω, R_L = 100 Ω, unless otherwise noted.

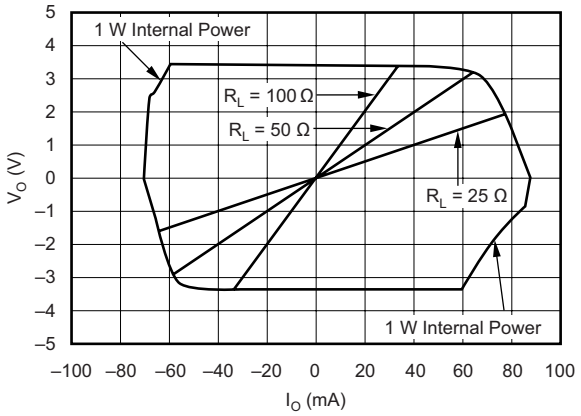


Figure 25. Output Voltage and Current Limitations

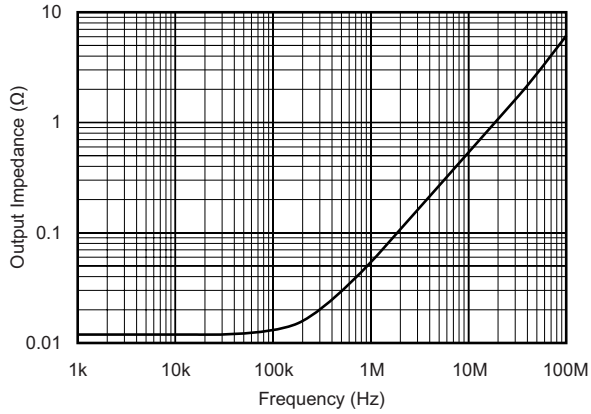


Figure 26. Closed-Loop Output Impedance vs Frequency

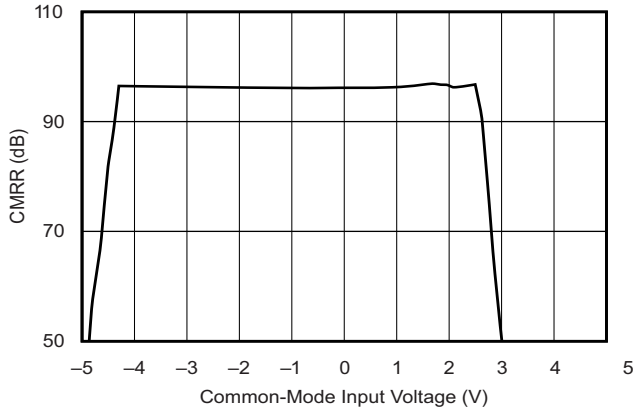


Figure 27. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

8 Detailed Description

8.1 Overview

The OPA656 is high gain-bandwidth, voltage feedback operational amplifier featuring a low noise JFET input stage. The OPA656 is compensated to be unity gain stable. The OPA656 finds wide use in optical front-end applications and in test and measurement systems that require high input impedance.

8.2 Feature Description

8.2.1 Input and ESD Protection

The OPA656 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 28.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA656), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

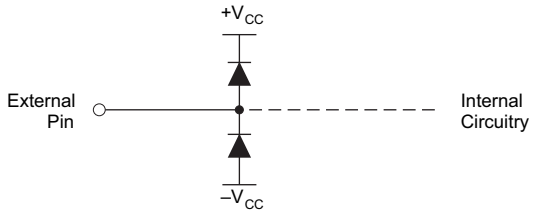


Figure 28. Internal ESD Protection

8.3 Device Functional Modes

8.3.1 Split-Supply Operation (±4 V to ±6 V)

To facilitate testing with common lab equipment, the OPA656 may be configured to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground. Figure 29 and Figure 30 show the OPA656 configured in a simple noninverting and inverting configuration respectively with ±5-V supplies. The input and output will swing symmetrically around ground. Due to its ease of use, split-supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.

8.3.2 Single-Supply Operation (8 V to 12 V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA656 is designed for use with split-supply configuration; however, it can be used with a single-supply with no change in performance, as long as the input and output are biased within the linear operation of the device. To change the circuit from split supply to single supply, level shift all the voltages by 1/2 the difference between the power supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of –PSRR will be minimized because the low supply rail has been grounded.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Wideband, Noninverting Operation

The OPA656 provides a unique combination of a broadband, unity gain stable, voltage-feedback amplifier with the DC precision of a trimmed JFET-input stage. Its very high Gain Bandwidth Product (GBP) of 230 MHz can be used to either deliver high signal bandwidths for low-gain buffers, or to deliver broadband, low-noise transimpedance bandwidth to photodiode-detector applications. To achieve the full performance of the OPA656, careful attention to printed-circuit-board (PCB) layout and component selection is required as discussed in the remaining sections of this data sheet.

Figure 29 shows the noninverting gain of +2 V/V circuit used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 29, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 29) while output power specifications are at the matched 50-Ω load. The total 100-Ω load at the output combined with the 500-Ω total feedback network load, presents the OPA656 with an effective output load of 83 Ω for the circuit of Figure 29.

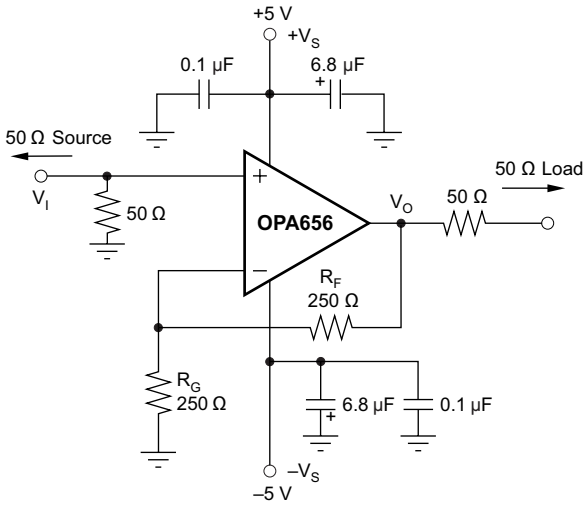


Figure 29. Noninverting G = +2 V/V Specifications and Test Circuit

Voltage-feedback operational amplifiers, unlike current feedback products, can use a wide range of resistor values to set their gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 29, the parallel combination of R_F || R_G should always < 200 Ω. In the noninverting configuration, the parallel combination of R_F || R_G will form a pole with the parasitic input capacitance at the inverting node of the OPA656 (including layout parasitics). For best performance, this pole should be at a frequency greater than the closed loop bandwidth for the OPA656. For this reason, TI recommends a direct short from output to inverting input for the unity gain follower application.

Application Information (continued)

9.1.2 Wideband, Inverting Gain Operation

The circuit of Figure 30 shows the inverting gain of –1 V/V test circuit used for most of the inverting Typical Characteristics. In this case, an additional resistor R_M is used to achieve the 50-Ω input impedance required by the test equipment using in characterization. This input impedance matching is optional in a circuit board environment where the OPA656 is used as an inverting amplifier at the output of a prior stage.

In this configuration, the output sees the feedback resistor as an additional load in parallel with the 100-Ω load used for test. It is often useful to increase the R_F value to decrease the loading on the output (improving harmonic distortion) with the constraint that the parallel combination of R_F || R_G < 200 Ω. For higher inverting gains with the DC precision provided by the FET input OPA656, consider the higher gain bandwidth product OPA657.

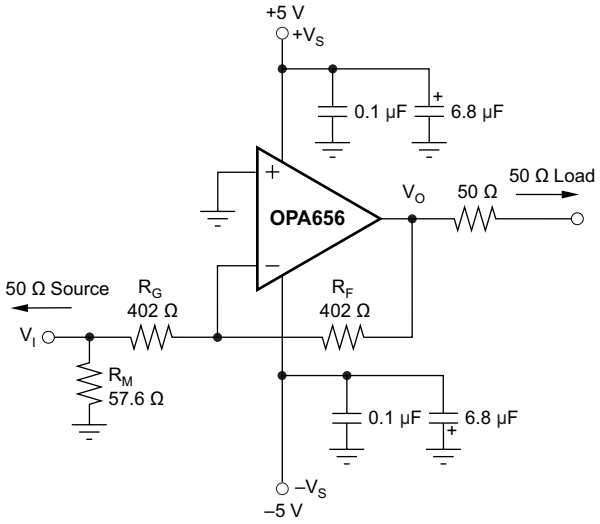


Figure 30. Inverting G = –1 V/V Specifications and Test Circuit

Figure 30 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the DC errors caused by input bias current effects. This is only useful when the input bias currents are matched. For a JFET part like the OPA656, the input bias currents do not match but are so low to begin with (< 5 pA) that DC errors due to input bias currents are negligible. Hence, no resistor is recommended at the noninverting inputs for the inverting signal path condition.

9.1.3 Operating Suggestions

9.1.3.1 Setting Resistor Values to Minimize Noise

The OPA656 provides a very low input noise voltage while requiring a low 14-mA quiescent supply current. To take full advantage of this low input noise, careful attention to the other possible noise contributors is required. Figure 31 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

Application Information (continued)

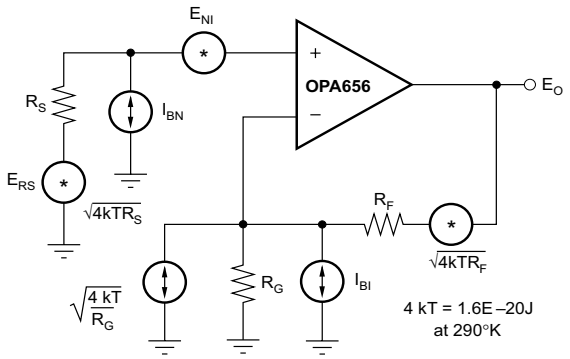


Figure 31. Operational Amplifier Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 31.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain ($GN = 1+R_F/R_G$) will give the equivalent input referred spot noise voltage at the noninverting input as shown in Equation 2.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Putting high resistor values into Equation 2 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 3 kΩ will add a Johnson voltage noise term equal to just that for the amplifier itself (7 nV/√Hz). While the JFET input of the OPA656 is ideal for high source impedance applications, both the overall bandwidth and noise will be limited by higher source impedances in the noninverting configuration of Figure 29.

9.1.3.2 Frequency Response Control

Voltage-feedback op amps like the OPA656 exhibit decreasing signal bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the *Electrical Characteristics*. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most high-speed amplifiers will exhibit a more complex response with lower phase margin. The OPA656 is compensated to give a maximally flat 2nd-order Butterworth closed loop response at a noninverting gain of +2 V/V (Figure 29). This results in a typical gain of +2 V/V bandwidth of 200 MHz, far exceeding that predicted by dividing the 230-MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10 V/V the OPA656 will show the 23-MHz bandwidth predicted using the simple formula and the typical GBP of 230 MHz.

Unity-gain stable operational amplifiers like the OPA656 can also be bandlimited using a capacitor across the feedback resistor. For the noninverting configuration of Figure 29, a capacitor across the feedback resistor will decrease the gain with frequency down to a gain of +1 V/V. For instance, to bandlimit the gain of +2 V/V design to 20 MHz, a 32-pF capacitor can be placed in parallel with the 250-Ω feedback resistor. This will, however, only decrease the gain from +2 V/V to +1 V/V. Using a feedback capacitor to limit the signal bandwidth is more effective in the inverting configuration of Figure 30. Adding that same capacitor to the feedback of Figure 30 will set a pole in the signal frequency response at 20 MHz, but in this case it will continue to attenuate the signal gain to below 1. However, the output noise contribution due the input voltage noise of the OPA656 will still only be reduced to a gain of +1 V/V with the addition of the feedback capacitor.

Application Information (continued)

9.1.3.3 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an operational amplifier is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA656 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The *Typical Characteristics: V_S = ±5 V* show the recommended R_S versus Capacitive Load and the resulting frequency response at the load. In this case, a design target of a maximally flat frequency response was used. Lower values of R_S may be used if some peaking can be tolerated. Also, operating at higher gains (than the +2 used in *Typical Characteristics: V_S = ±5 V*) will require lower values of R_S for a minimally peaked frequency response. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA656. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA656 output pin (see Layout section).

9.1.3.4 Distortion Performance

The OPA656 is capable of delivering a low distortion signal at high frequencies over a wide range of gains. The distortion plots in the *Typical Characteristics: V_S = ±5 V* show the typical distortion under a wide variety of conditions.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is sum of R_F + R_G, while in the inverting configuration this is just R_F (see Figure 29). Increasing output voltage swing increases harmonic distortion directly. A 6-dB increase in output swing will generally increase the 2nd-harmonic 12 dB and the 3rd-harmonic 18 dB. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again a 6-dB increase in gain will increase the 2nd- and 3rd-harmonic by about 6 dB even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open loop pole at approximately 100 kHz. Starting from the –70 dBc 2nd-harmonic for a 5 MHz, $2V_{PP}$ fundamental into a 200-Ω load at G = +2 V/V (from the *Typical Characteristics: V_S = ±5 V*), the 2nd-harmonic distortion for frequencies lower than 100 kHz will be < –105 dBc.

The OPA656 has an extremely low 3rd-order harmonic distortion. This also shows up in the 2-tone 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low < –80 dBc) at low output power levels. The output stage continues to hold them low even as the fundamental power reaches higher levels. As the *Typical Characteristics: V_S = ±5 V* show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 10 MHz, with 4 dBm/tone into a matched 50-Ω load (that is, $1V_{PP}$ for each tone at the load, which requires 4 VPP for the overall 2-tone envelope at the output pin), the *Typical Characteristics: V_S = ±5 V* show a 78-dBc difference between the test tone and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies and/or higher load impedances.

Application Information (continued)

9.1.3.5 DC Accuracy and Offset Control

The OPA656 can provide excellent DC accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and its trimmed input offset voltage (and drift) along with the negligible errors introduced by the low input bias current. For the best DC precision, a highgrade version (OPA656UB or OPA656NB) screens the key DC parameters to an even tighter limits. Both standard- and high-grade versions take advantage of a new final test technique to 100% test input offset voltage drift over temperature. This discussion will use the high-grade typical and minimum and maximum electrical characteristics for illustration; however, an identical analysis applies to the standard-grade version.

The total output DC offset voltage in any configuration and temperature will be the combination of a number of possible error terms. In a JFET part like the OPA656, the input bias current terms are typically quite low but are unmatched. Using bias current cancellation techniques, more typical in bipolar input amplifiers, does not improve output DC offset errors. Errors due to the input bias current will only become dominant at elevated temperatures. The OPA656 shows the typical 2× increase in every 10°C common to JFET-input stage amplifiers. Using the 5-pA maximum tested value at 25°C, and a 20°C internal self heating (see *Thermal Considerations*), the maximum input bias current at 85°C ambient will be 5 pA × $2^{(105\ -\ 25)}$/10 = 1280 pA. For noninverting configurations, this term only begins to be a significant term versus the input offset voltage for source impedances > 750 kΩ. This would also be the feedback-resistor value for transimpedance applications (see Figure 32) where the output DC error due to inverting input bias current is on the order of that contributed by the input offset voltage. In general, except for these extremely high impedance values, the output DC errors due to the input bias current may be neglected.

After the input offset voltage itself, the most significant term contributing to output offset voltage is the PSRR for the negative supply. This term is modeled as an input offset voltage shift due to changes in the negative power-supply voltage (and similarly for the +PSRR). The high-grade test limit for –PSRR is 62 dB. This translates into 1.59-mV/V input offset voltage shift = $10^{(-62/20)}$. In the worst case, a ±0.38 V (±7.6%) shift in the negative supply voltage will produce a ±0.6 mV apparent input offset voltage shift. Because this is comparable to the tested limit of ±0.6 mV input offset voltage, a careful control of the negative supply voltage is required. The +PSRR is tested to a minimum value of 74 dB. This translates into $10^{(-74/20)}$ = 0.2 mV/V sensitivity for the input offset voltage to positive power supply changes.

As an example, compute the worst-case output DC error for the transimpedance circuit of Figure 32 at 25°C and then the shift over the 0°C to 70°C range given the following assumptions.

Negative Power Supply = –5 V ±0.2V with a ±5mV/°C worst-case shift

Positive Power Supply = +5 V ±0.2V with a ±5mV/°C worst-case shift

Initial 25°C Output DC Error Band

= ±0.3 mV (due to the –PSRR = 1.59 mV/V × ±0.2 V)
±0.04 mV (due to the +PSRR = 0.2 mV/V × ±0.2 V)
±0.6 mV Input Offset Voltage

Total = ±0.94 mV

This would be the worst-case error band in volume production at 25°C acceptance testing given the conditions stated.

Over the temperature range of 0°C to 70°C, we can expect the following worst-case shifting from initial value. A 20°C internal junction self heating is assumed here.

±0.36 mV (OPA656 high-grade input offset drift) = ±6 µV/°C × (70°C + 20°C – 25°C))
±0.23 mV (–PSRR of 60 dB with 5 mV × (70°C – 25°C) supply shift)
±0.06 mV (+PSRR of 72 dB with 5 mV × (70°C – 25°C) supply shift)
Total = ±0.65 mV

This would be the worst-case shift from initial offset over a 0°C to 70°C ambient for the conditions stated. Typical initial output DC error bands and shifts over temperature will be much lower than these worst-case estimates.

Application Information (continued)

In the transimpedance configuration, the CMRR errors can be neglected because the input common mode voltage is held at ground. For noninverting gain configurations (see Figure 29), the CMRR term must be considered but will typically be far lower than the input offset voltage term. With a tested minimum of 80 dB (100 µV/V), the added apparent DC error will be no more than ±0.2 mV for a ±2-V input swing to the circuit of Figure 29.

9.2 Typical Application

The high GBP and low input voltage and current noise for the OPA656 make it an ideal wideband transimpedance amplifier for moderate to high transimpedance gains.

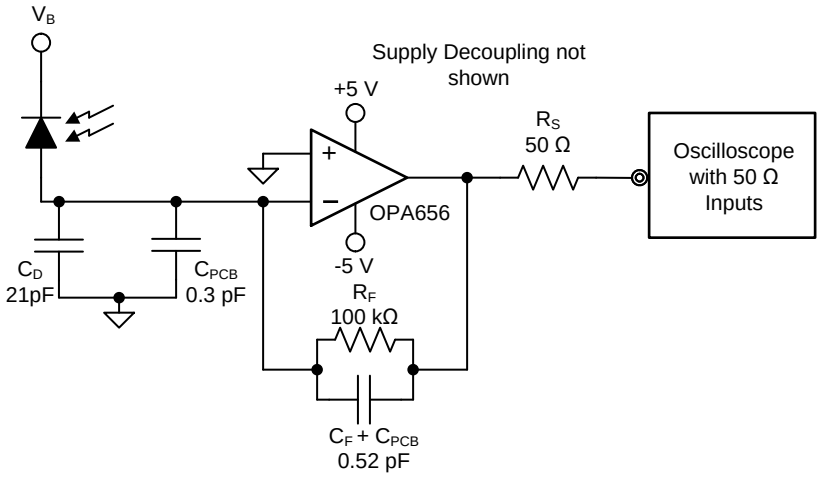


Figure 32. Wideband, High-Sensitivity, Transimpedance Amplifier

9.2.1 Design Requirements

Design a high-bandwidth, high-gain transimpedance amplifier with the design requirements shown in Table 1.

Table 1. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (KΩ)	PHOTODIODE CAPACITANCE (pF)
4	100	21

9.2.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA656. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_B) applied the desired transimpedance gain, R_F, and the GBP for the OPA656 (230 MHz). Figure 32 shows a transimpedance circuit with the parameters as described in Table 1. With these three variables set (and including the parasitic input capacitance for the OPA656 and the PCB added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response. To achieve a maximally-flat second-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (3)$$

The input capacitance of the amplifier is the sum of its common-mode and differential capacitance (0.7+2.8) pF. The parasitic capacitance from the photo-diode package and the PCB is approximately 0.3 pF. This results in a total input capacitance, CD {D should be a subscript} = 24.8 pF. From Equation 3, the feedback pole should be set at 2.7 MHz. Setting the pole at 2.7 MHz requires a total feedback capacitance of 0.585 pF

The approximate –3-dB bandwidth of the transimpedance amplifier circuit is given by:

$$f_{-3dB} = \sqrt{GBP / (2\pi R_F C_D)}\ Hz \quad (4)$$

Equation 4 estimates a closed-loop bandwidth of 3.84 MHz. The total feedback capacitance for the circuit used in the measurement is estimated to be 0.520 pF. The total feedback capacitance includes the physical 0.4-pF feedback capacitor in parallel with 120-fF of parasitic capacitance due to the feedback resistor and PCB trace. The parasitic capacitance from the PCB trace can be minimized by removing the ground and power planes in the feedback path. A TINA SPICE simulation of the circuit in Figure 32 resulted in a closed-loop bandwidth of 4.2 MHz.

Figure 33 shows the measured output noise of the system. The low-frequency output noise of 45 nV/√Hz gets input-referred to 0.45 pA/√Hz. The transimpedance gain resistor is the dominant noise source with the operational amplifier itself contributing a negligible amount, reflecting one of the main benefits in using a JFET input amplifier in a high-gain transimpedance application. If the total output noise of the TIA is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent output noise voltage can be derived as shown in Equation 5.

$$V_{OUTN} = \sqrt{(I_N R_F)^2 + 4kTR_F + E_N{}^2 + \frac{(E_N 2\pi C_D R_F F)^2}{3}} \quad (5)$$

where

- V_{OUTN} = Equivalent output noise when band limited to F < 1 / (2 ΩRfCf)
- I_N = Input current noise for the operational amplifier inverting input
- E_N = Input voltage noise for the operational amplifier
- C_D = Diode capacitance including operational amplifier and PCB parasitic capacitance
- F = Band-limiting frequency in Hz (usually a postfilter before further signal processing)
- 4 kT = 1.6 e – 20 J at T = 290°K

Figure 34 shows the measured pulse response to a 2-µA input current pulse. The output voltage measured on the scope is 0.1 V because of the 50-Ω termination to the scope. The measured rise/fall time and overshoot match very well with simulation. Based on the measured rise and fall time of 85 ns, the approximate bandwidth of the circuit = 0.35/85 ns = 4.1 MHz,which also matches the theoretical value calculated using Equation 4.

9.2.3 Application Curves

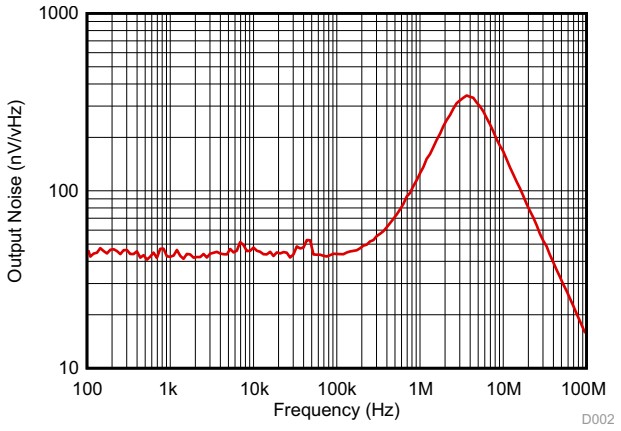
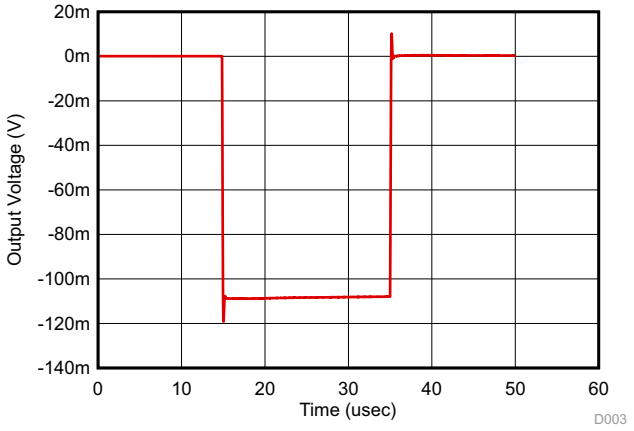


Figure 33. Measured Total TIA Noise



Rise Time = 84.9 ns
Fall Time = 85.4 ns

Figure 34. Transient Pulse Response to 2-µA Input Current Pulse

10 Power Supply Recommendations

The OPA656 is intended for operation on ±5-V supplies. Single-supply operation is allowed with minimal change from the stated specifications and performance from a single supply of 8 V to 12 V maximum. The limit to lower supply voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of 12 V can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at 12-V operation with minimal increase in supply current.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA656 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include.

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components will preserve the high frequency performance of the OPA656.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 1.5 kΩ, this parasitic capacitance can add a pole and/or zero below 500 MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be to keep $R_F \parallel R_G <$ 250 Ω for voltage amplifier applications. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance. Transimpedance applications (see) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5 pF) may not need an R_S because the OPA656 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA656 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device— this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

Layout Guidelines (continued)

5. **Socketing a high speed part like the OPA656 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA656 onto the board.

11.1.1 Demonstration Fixtures

Two printed-circuit-boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA656 device in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 2.

Table 2. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA656U	SO-8	DEM-OPA-SO-1A	SBOU009
OPA656N	SOT23-5	DEM-OPA-SOT-1A	SBOU010

The demonstration fixtures can be requested at the Texas Instruments website (www.ti.com) through the OPA656 product folder.

11.2 Layout Example

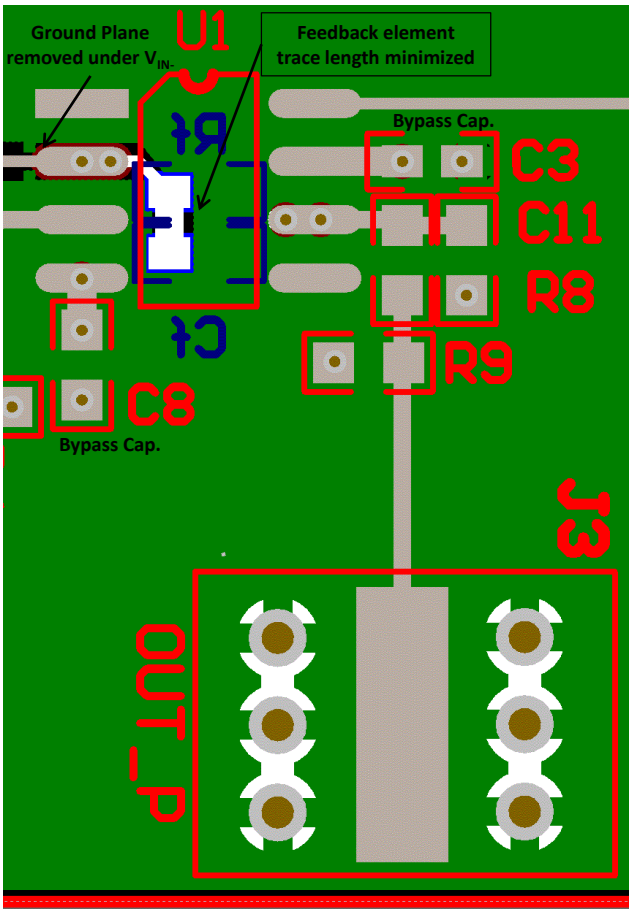


Figure 35. Layout Recommendation

11.3 Thermal Considerations

The OPA656 will not require heatsinking or airflow in most applications. Maximum allowed junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S{}^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA656N (SOT23-5 package) in the circuit of Figure 29 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100-Ω load.

$P_D = 10\ V \times 16.1\ mA + 5^2/(4 \times (100\ \Omega \parallel 800\ \Omega)) = 231\ mW$

Maximum $T_J = 85°C + (0.23\ W \times 150°C/W) = 120°C$.

All actual applications will be operating at lower internal power and junction temperature.

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA656N/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B56	Samples
OPA656N/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B56	Samples
OPA656NB/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B56	Samples
OPA656U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 656U	Samples
OPA656U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 656U	Samples
OPA656UB	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 656U B	Samples
OPA656UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 656U B	Samples
OPA656UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 656U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

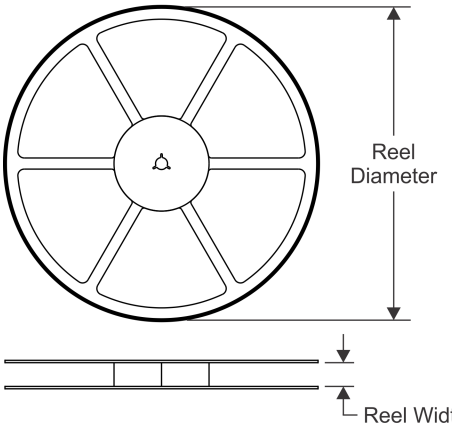
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

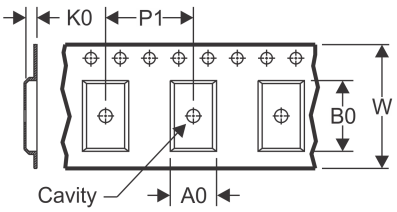
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

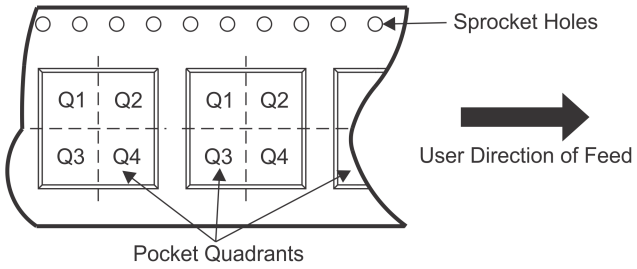


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

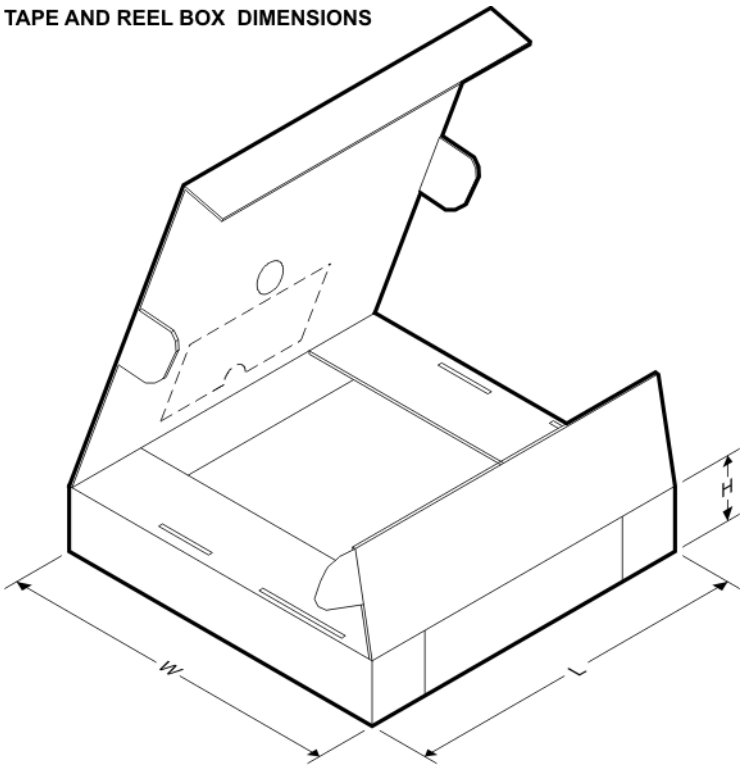
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

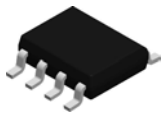
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA656U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA656UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA656U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA656UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

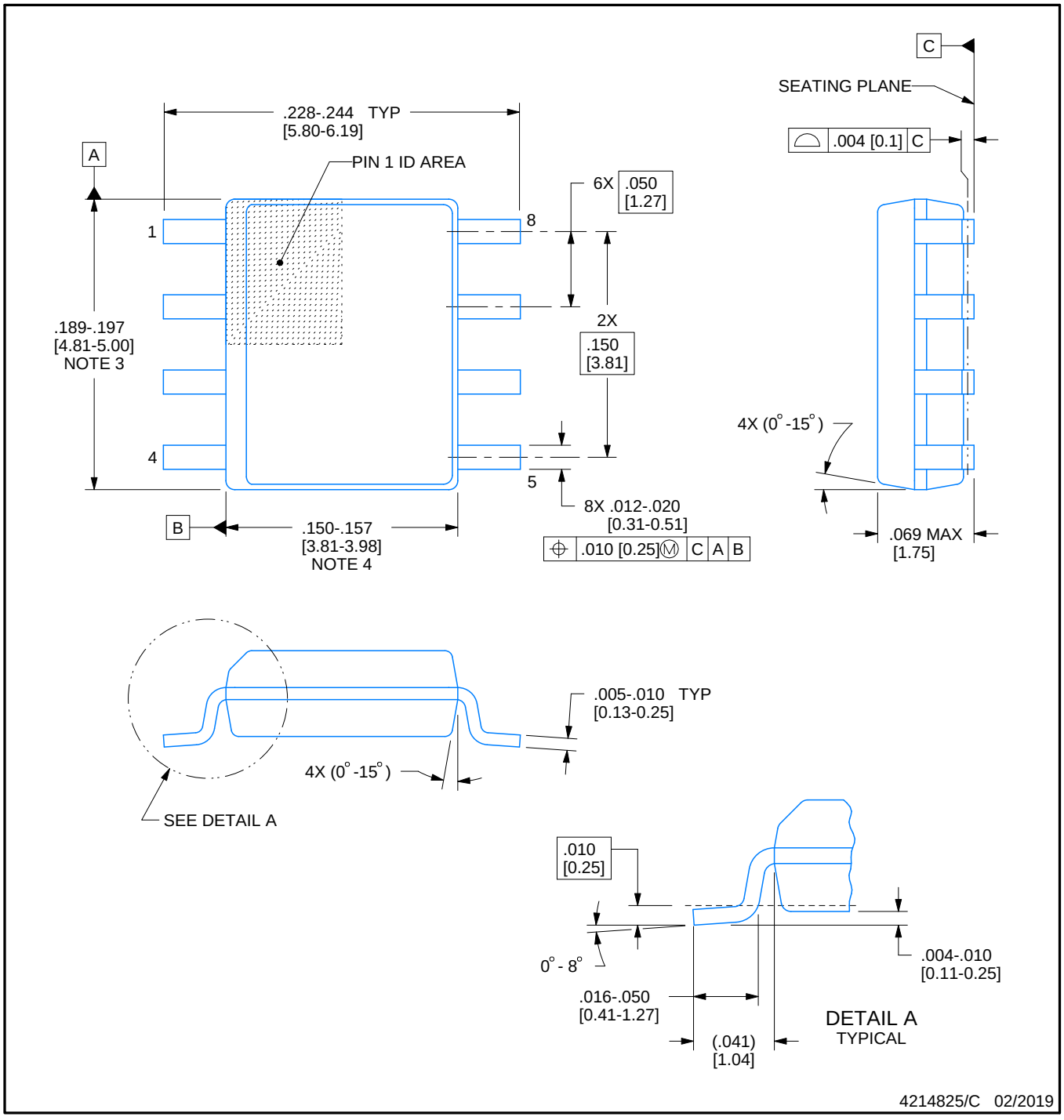


PACKAGE OUTLINE

D0008A

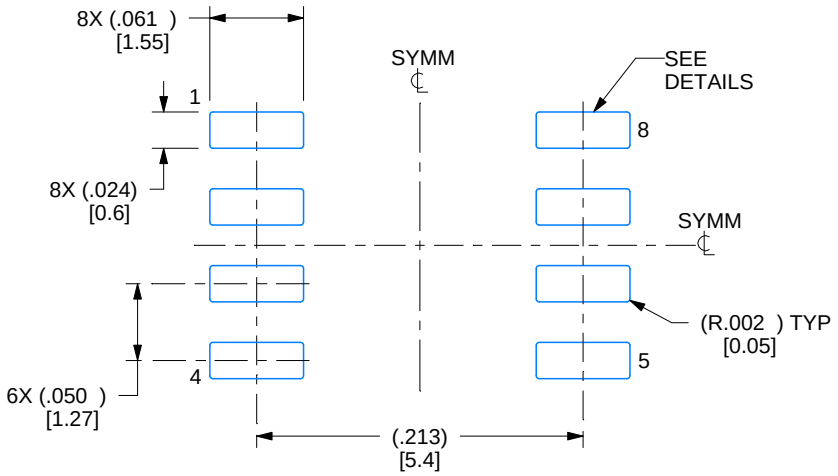
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

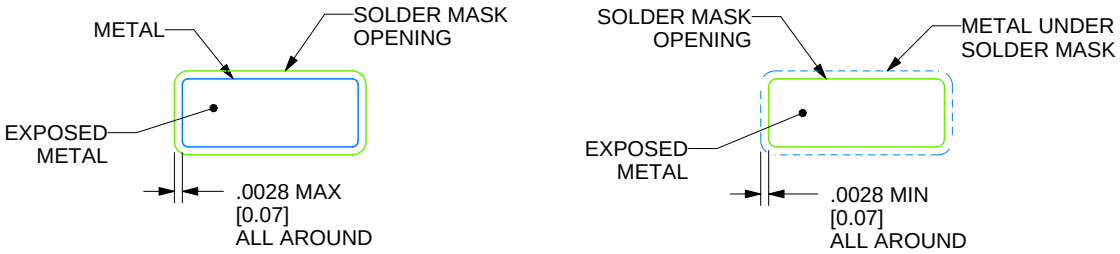


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

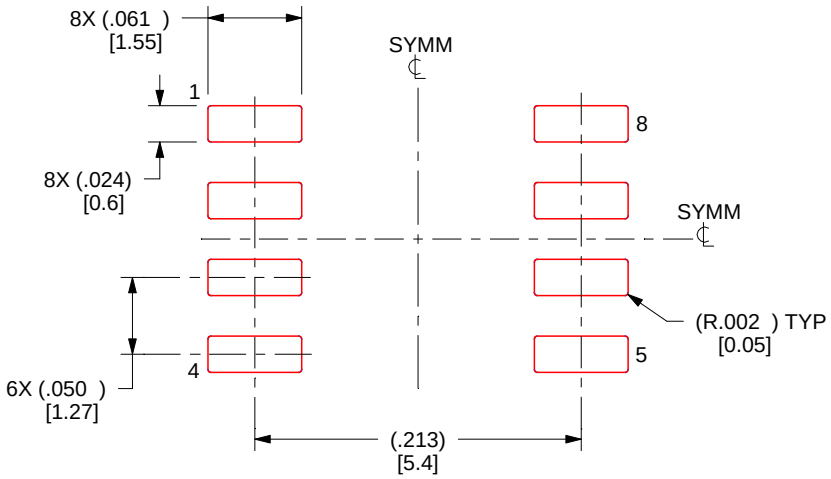
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

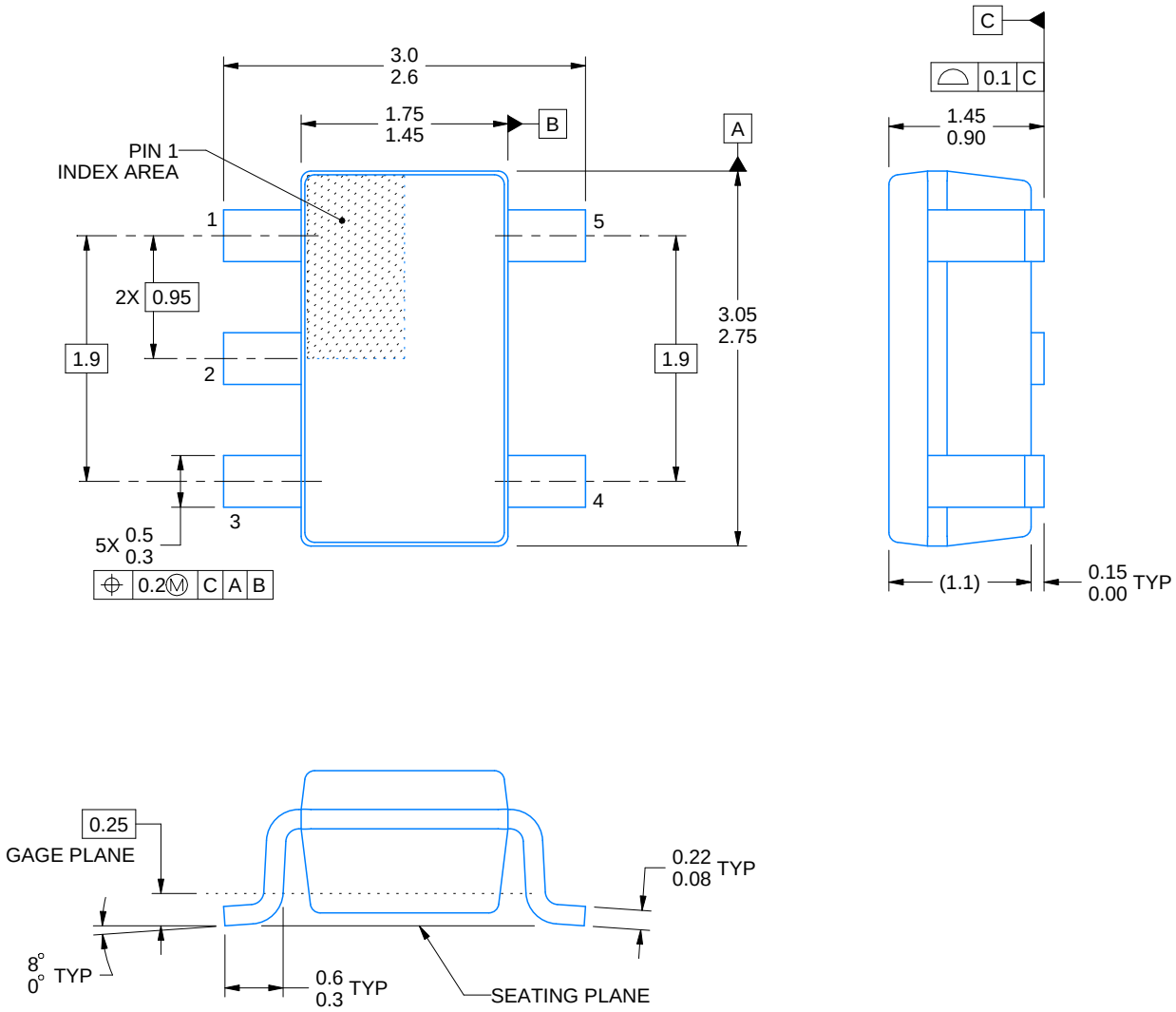
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

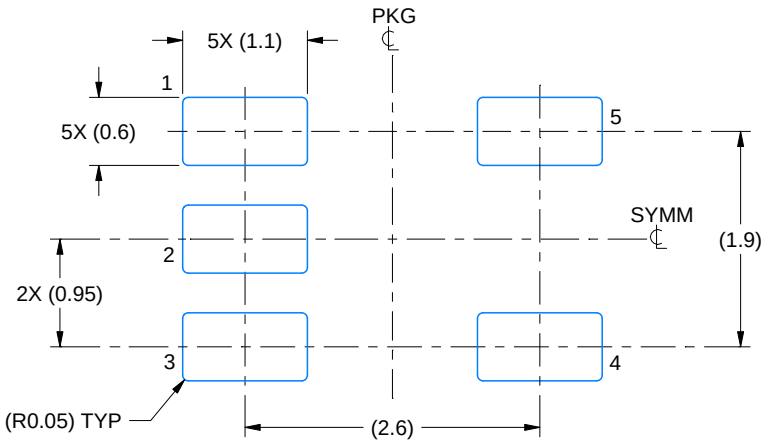
SMALL OUTLINE TRANSISTOR



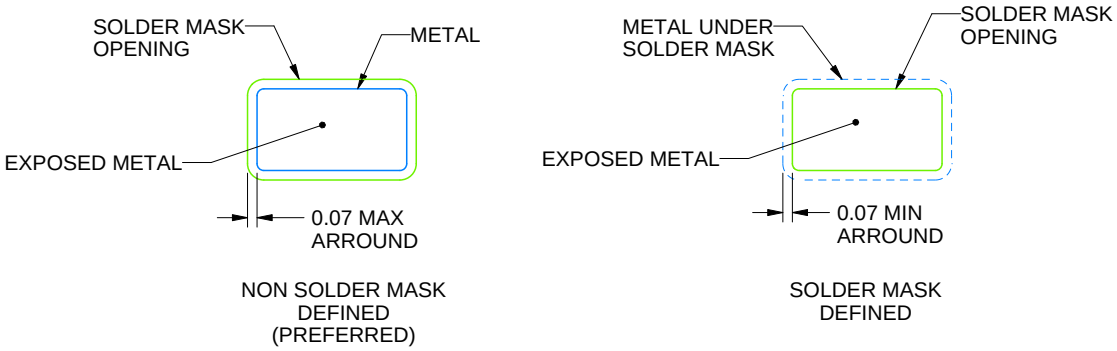
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

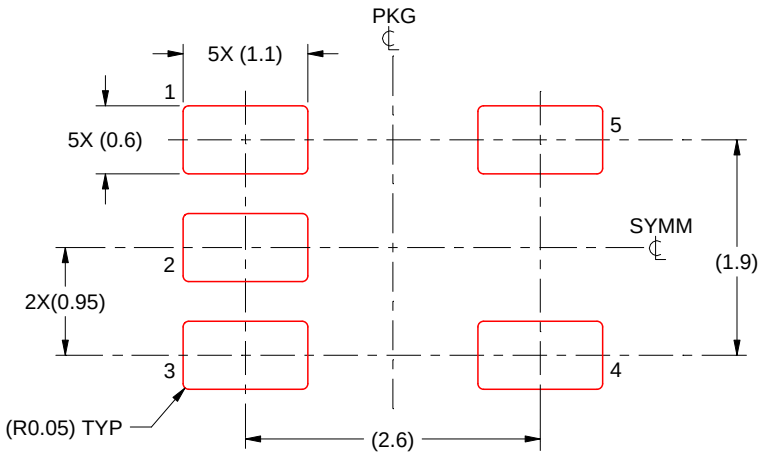


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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