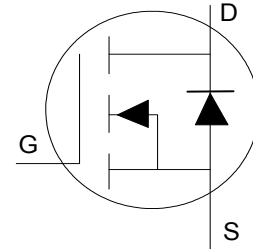


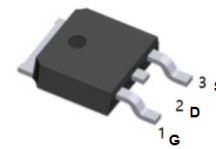
Application

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters



Features

V_{DS}	60V
I_D (at $V_{GS}=10V$)	71A
$R_{DS(ON)}$ (at $V_{GS}=5V$)	< 7.9m Ω



TO-252(DPAK) top view

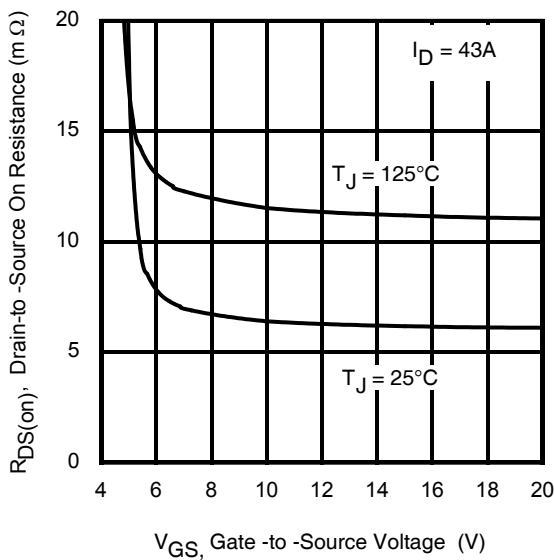


Fig 1. Typical On-Resistance vs. Gate Voltage

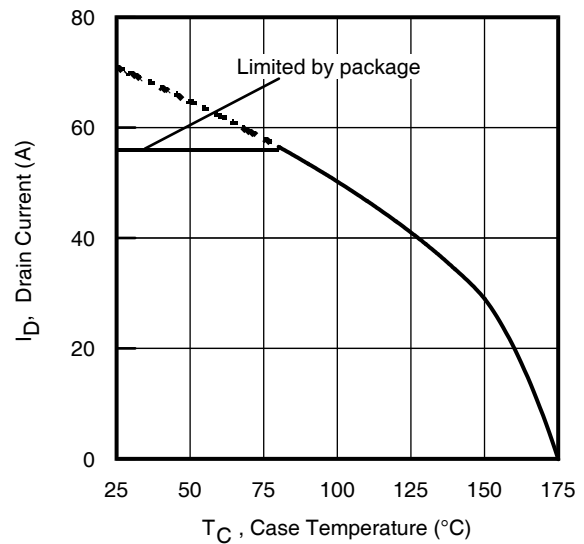


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	71 ^①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	50	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	56	
I_{DM}	Pulsed Drain Current ^②	280	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	99	W
	Linear Derating Factor	0.66	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Max.	Units
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	120	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^④	178	
I_{AR}	Avalanche Current ^②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ^②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑤	—	1.52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount)	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	47	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.6	7.9	m Ω	$V_{GS} = 10\text{V}, I_D = 43\text{A}$
		—	8.5	—		$V_{GS} = 6.0\text{V}, I_D = 21\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	1.5	—	Ω	

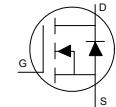
Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 130\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 43\text{A}$, $V_{GS} = 10\text{V}$.
- ④ $I_{SD} \leq 43\text{A}$, $di/dt \leq 1020\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_{θ} is measured at T_J approximately 90°C .
- ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 19\text{A}$, $V_{GS} = 10\text{V}$.

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	56	—	—	S	$V_{DS} = 25\text{V}$, $I_D = 43\text{A}$
Q_g	Total Gate Charge	—	58	87	nC	$I_D = 43\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$
Q_{gs}	Gate-to-Source Charge	—	14	—		
Q_{gd}	Gate-to-Drain Charge	—	18	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	26	—		
$t_{d(on)}$	Turn-On Delay Time	—	8.1	—	ns	$V_{DD} = 30\text{V}$ $I_D = 43\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
t_r	Rise Time	—	28	—		
$t_{d(off)}$	Turn-Off Delay Time	—	36	—		
t_f	Fall Time	—	20	—		
C_{iss}	Input Capacitance	—	3020	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$, See Fig.7
C_{oss}	Output Capacitance	—	280	—		
C_{riss}	Reverse Transfer Capacitance	—	180	—		
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	290	—		
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	370	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	71 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	280		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 43\text{A}$, $V_{GS} = 0\text{V}$ ⑤
dv/dt	Peak Diode Recovery dv/dt	—	12	—	V/ns	$T_J = 175^\circ\text{C}$, $I_S = 43\text{A}$, $V_{DS} = 60\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	26	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$
		—	29	—		$T_J = 125^\circ\text{C}$ $I_F = 43\text{A}$,
Q_{rr}	Reverse Recovery Charge	—	22	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤
		—	30	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.5	—	A	$T_J = 25^\circ\text{C}$

60V N-Channel MOSFET

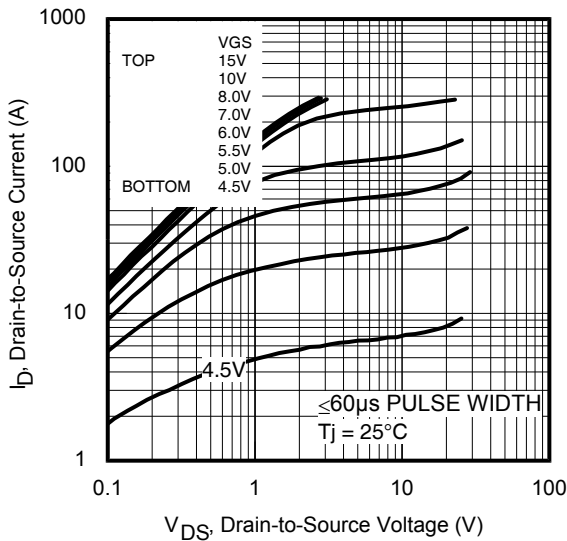


Fig 3. Typical Output Characteristics

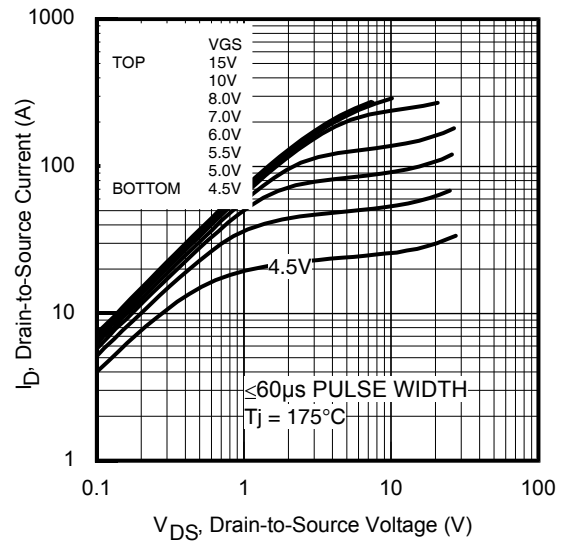


Fig 4. Typical Output Characteristics

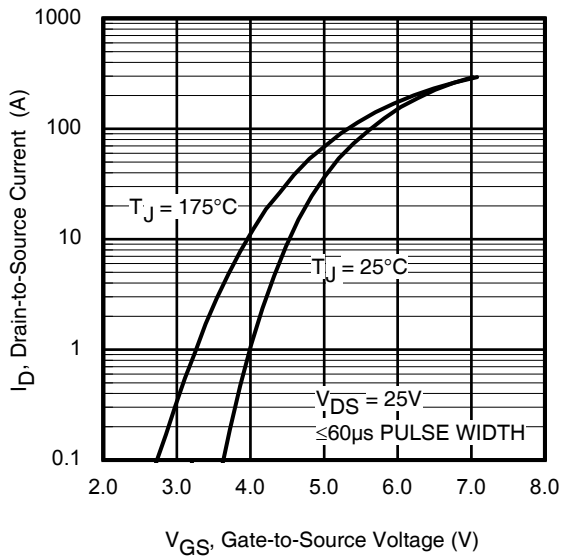


Fig 5. Typical Transfer Characteristics

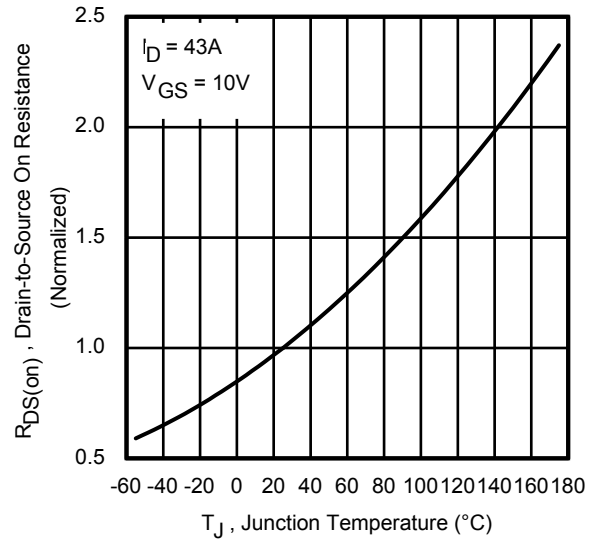


Fig 6. Normalized On-Resistance vs. Temperature

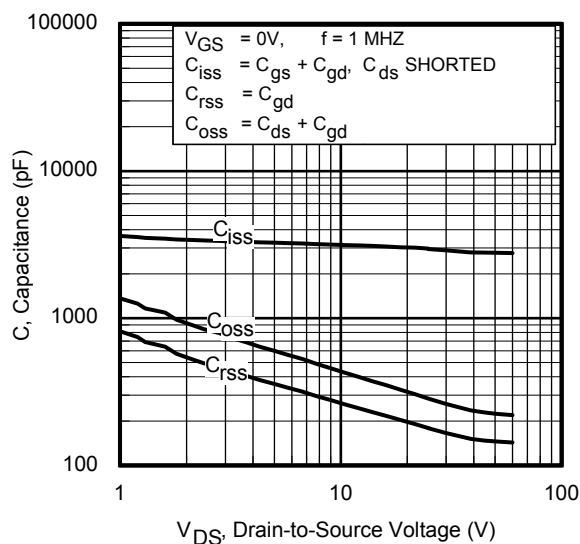


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

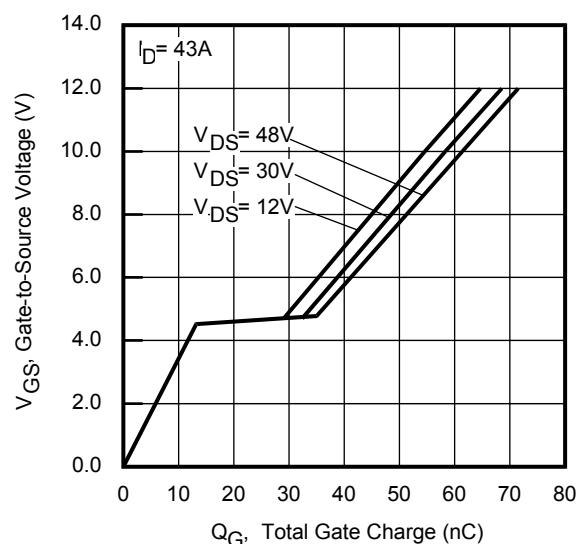


Fig 8. Typical Gate Charge vs.

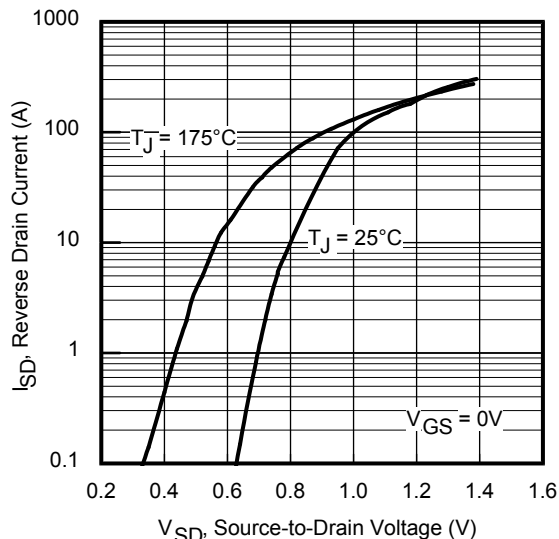


Fig 9. Typical Source-Drain Diode Forward Voltage

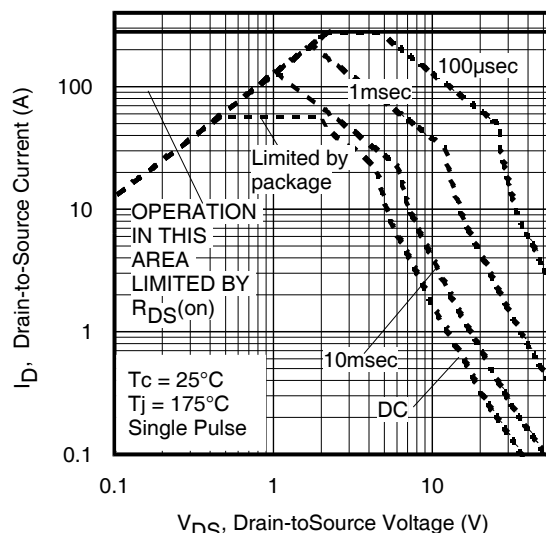


Fig 10. Maximum Safe Operating Area

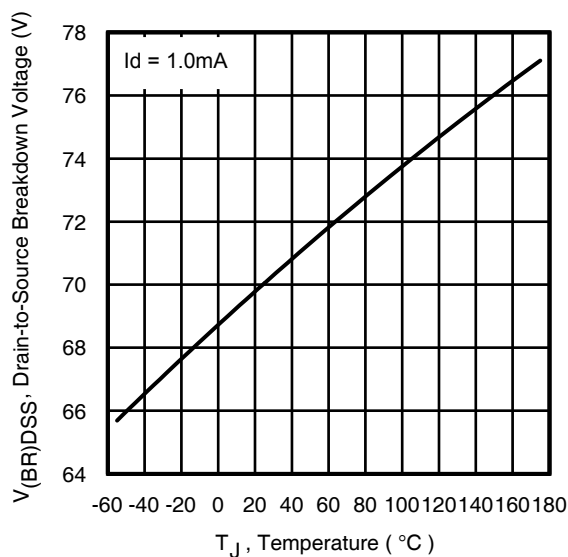


Fig 11. Drain-to-Source Breakdown Voltage

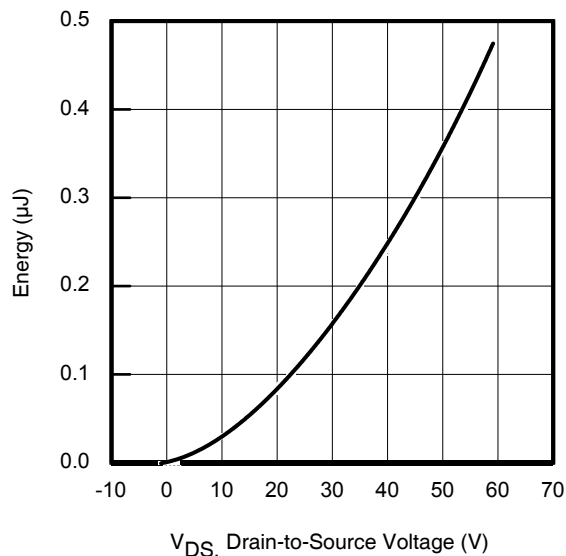


Fig 12. Typical C_{oss} Stored Energy

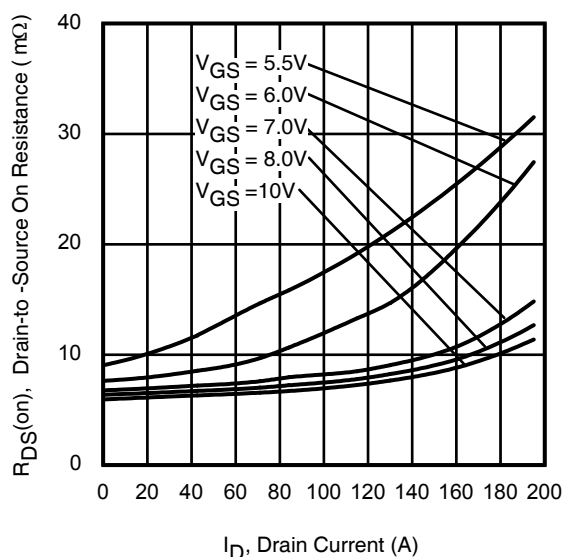


Fig 13. Typical On-Resistance vs. Drain Current

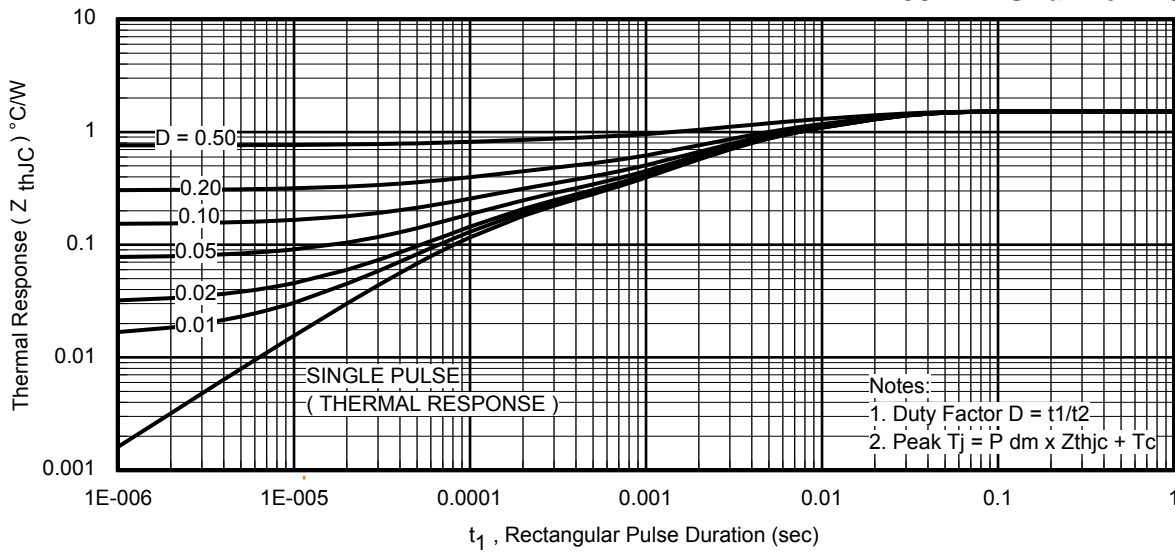


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

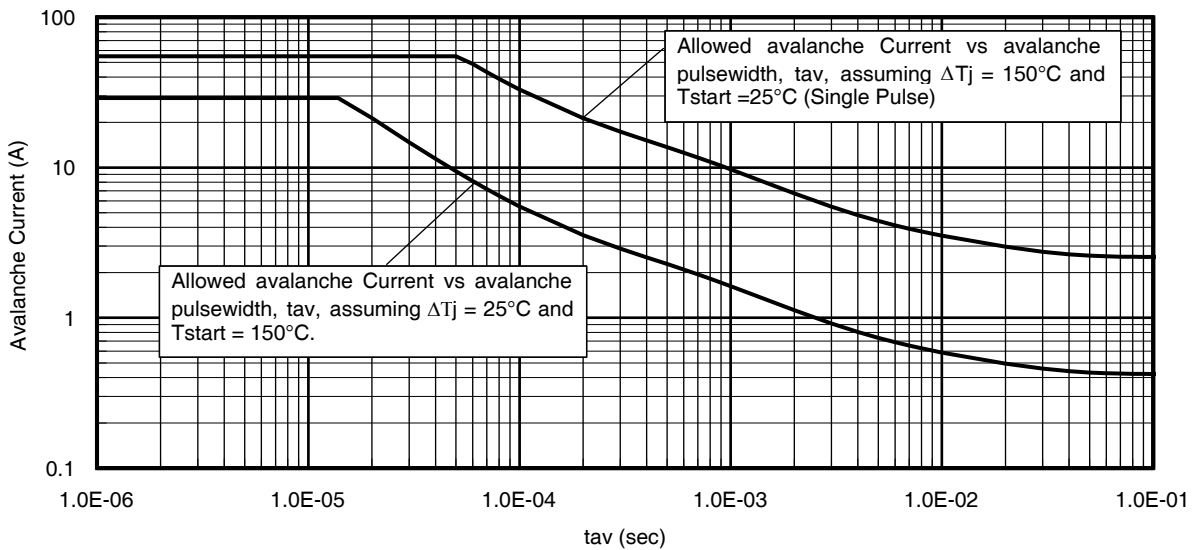


Fig 15. Avalanche Current vs. Pulse Width

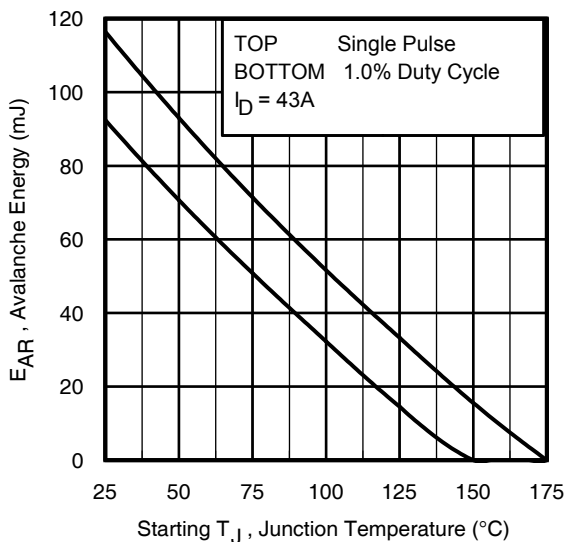


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

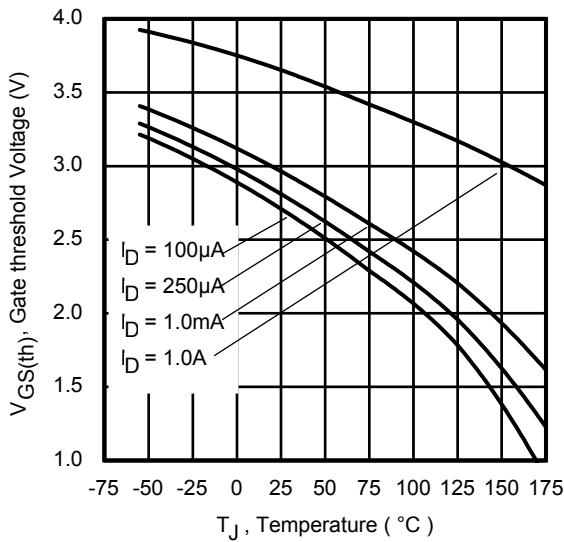


Fig 17. Threshold Voltage vs. Temperature

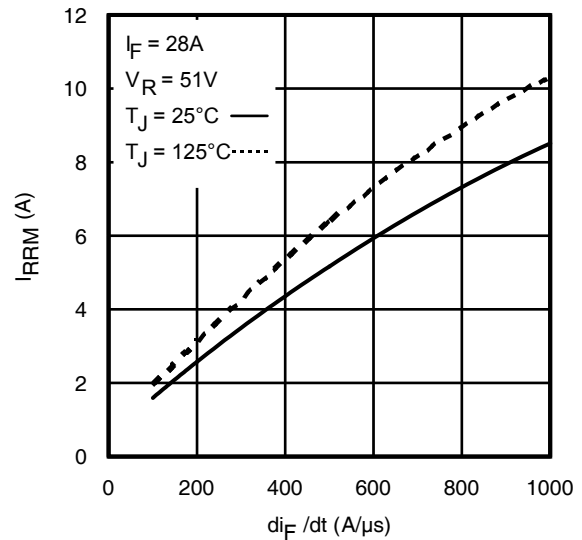


Fig 18. Typical Recovery Current vs. di_F/dt

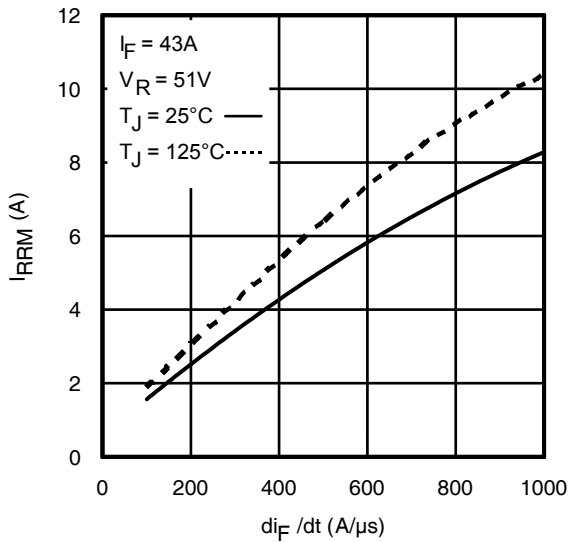


Fig 19. Typical Recovery Current vs. di_F/dt

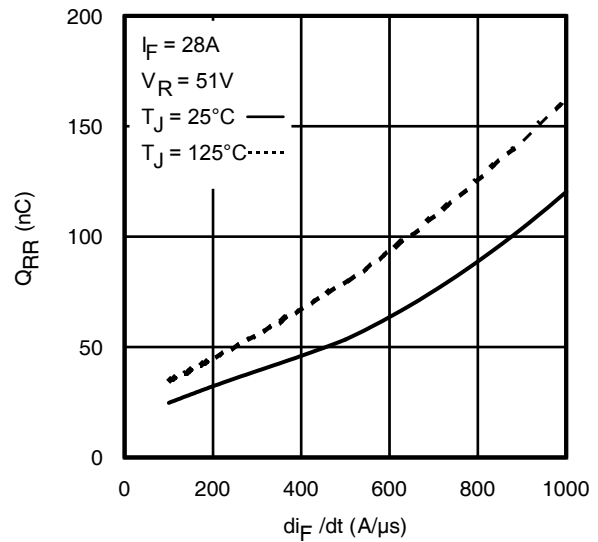


Fig 20. Typical Stored Charge vs. di_F/dt

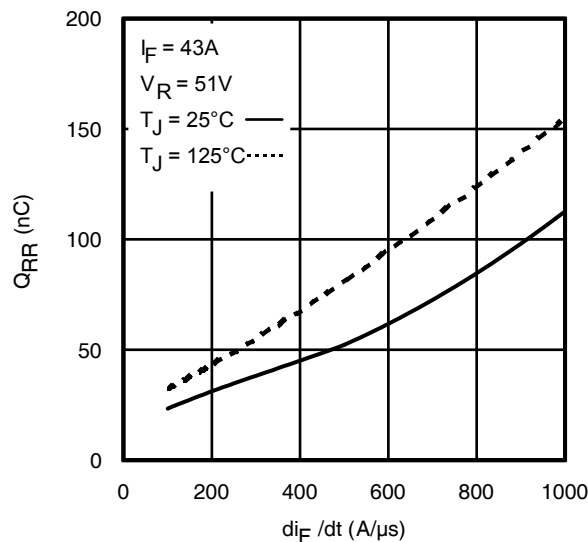


Fig 21. Typical Stored Charge vs. di_F/dt

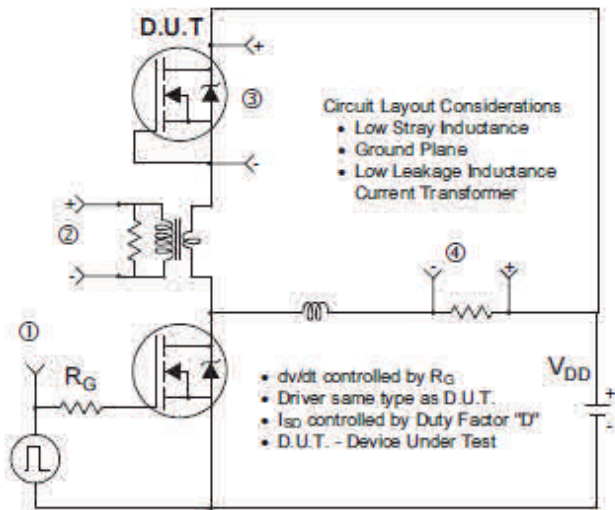


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel Power MOSFETs

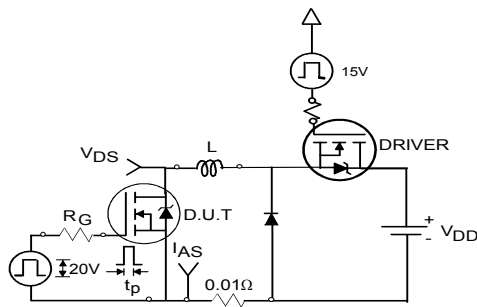
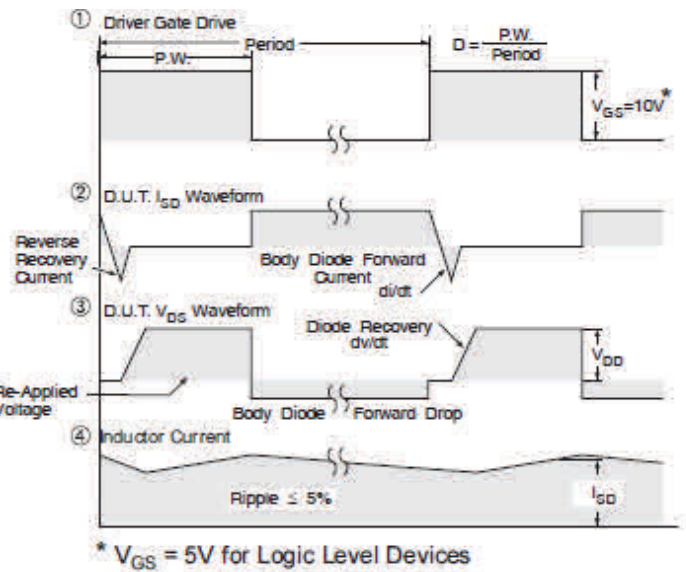


Fig 23a. Unclamped Inductive Test Circuit

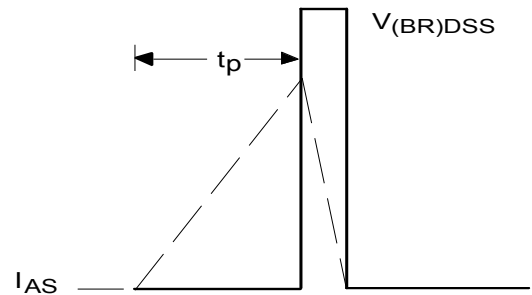


Fig 23b. Unclamped Inductive Waveforms

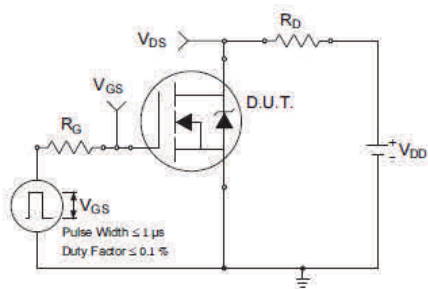


Fig 24a. Switching Time Test Circuit

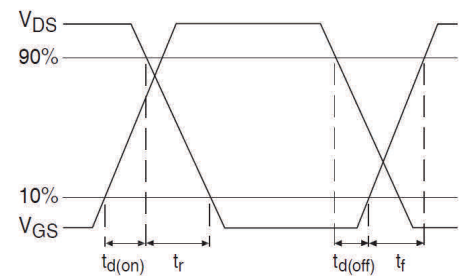


Fig 24b. Switching Time Waveforms

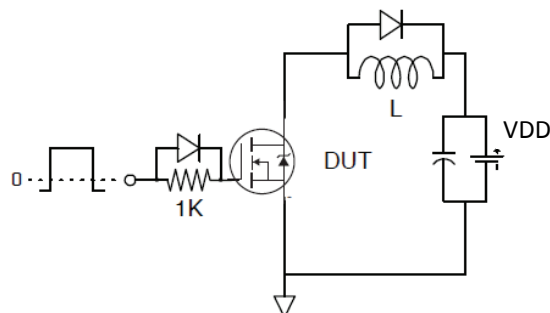


Fig 25a. Gate Charge Test Circuit

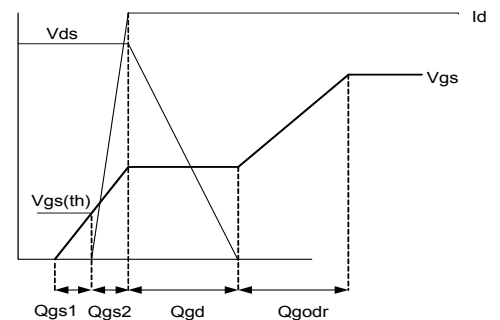
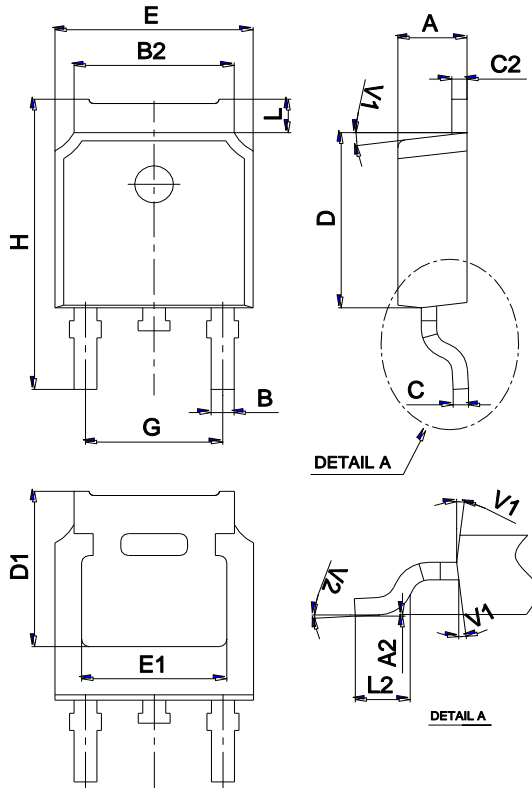


Fig 25b. Gate Charge Waveform

Package Mechanical Data TO-252

60V N-Channel MOSFET



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Ordering information

Order code	Package	Baseqty	Delivery mode
UMW IRFR7546TR	TO-252	2500	Tape and reel