Single Supply, Rail-to-Rail Low Power, FET-Input Op Amp

Data Sheet **AD824**

FEATURES

Single supply operation: 3 V to 30 V
Very low input bias current: 2 pA
Wide input voltage range
Rail-to-rail output swing
Low supply current per amplifier: 500 µA
Wide bandwidth: 2 MHz
Slew rate: 2 V/µs
No phase reversal

APPLICATIONS

Photo diode preamplifier
Battery powered instrumentation
Power supply control and protection
Medical instrumentation
Remote sensors
Low voltage strain gage amplifiers
DAC output amplifier

PIN CONFIGURATION

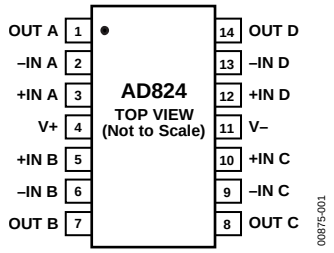

Figure 1. 14-Lead SOIC (R Suffix)

GENERAL DESCRIPTION

The AD824 is a quad, FET input, single supply amplifier, featuring rail-to-rail outputs. The combination of FET inputs and rail-to-rail outputs makes the AD824 useful in a wide variety of low voltage applications where low input current is a primary consideration.

The AD824 is guaranteed to operate from a 3 V single supply up to ±15 V dual supplies. AD824AR-3V parametric performance at 3 V is fully guaranteed.

Fabricated on Analog Devices, Inc., complementary bipolar process, the AD824 has a unique input stage that allows the input voltage to safely extend beyond the negative supply and to the positive supply without any phase inversion or latch-up. The output voltage swings to within 15 mV of the supplies. Capacitive loads to 350 pF can be handled without oscillation.

The FET input combined with laser trimming provides an input that has extremely low bias currents with guaranteed offsets below 1 mV. This enables high accuracy designs even with high source impedances. Precision is combined with low noise, making the AD824 ideal for use in battery powered medical equipment.

Applications for the AD824 include portable medical equipment, photo diode preamplifiers, and high impedance transducer amplifiers.

The ability of the output to swing rail-to-rail enables designers to build multistage filters in single supply systems and maintain high signal-to-noise ratios.

The AD824 is specified over the extended industrial (−40°C to +85°C) temperature range and is available in narrow 14-lead SOIC package.

Rev. E **Document Feedback**
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REVISION HISTORY

4/15—Rev. D to Rev. E

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5/14—Rev. C to Rev. D

Updated Format ... Universal
Removed 16-Lead SOIC Package (Throughout) ... 1
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2/03—Rev. B to Rev. C

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1/02—Rev. A to Rev. B

Edits to Electrical Specifications ... 2, 3
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

At V_S = 5.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = 25°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD824A)	V_{OS}			0.1	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		300	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		300		pA
Input Voltage Range			−0.2		+3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	80		dB
		V_{CM} = 0 V to 3 V	60	74		dB
		T_{MIN} to T_{MAX}	60			dB
Input Impedance				10^{13}||3.3		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 4.0 V				
		R_L = 2 kΩ	20	40		V/mV
		R_L = 10 kΩ	50	100		V/mV
		R_L = 100 kΩ	250	1000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	180	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	4.975	4.988		V
		T_{MIN} to T_{MAX}	4.97	4.985		V
		I_{SOURCE} = 2.5 mA	4.80	4.85		V
		T_{MIN} to T_{MAX}	4.75	4.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/source		±12		mA
		T_{MIN} to T_{MAX}		±10		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% distortion, V_O = 4 V p-p		150		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 4.5 V, to 0.01%		2.5		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	φo	No load		50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		−123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.8		fA/√Hz
Total Harmonic Distortion	THD	f = 10 kHz, R_L = ∞, A_V = +1		0.005		%

At V_S = ±15.0 V, V_{OUT} = 0 V, T_A = 25°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD824A)	V_{OS}			0.5	2.5	mV
		T_{MIN} to T_{MAX}		0.6	4.0	mV
Input Bias Current	I_B	V_{CM} = 0 V		4	35	pA
		T_{MIN} to T_{MAX}		500	4000	pA
	I_B	V_{CM} = −10 V		25		pA
Input Offset Current	I_{OS}			3	20	pA
		T_{MIN} to T_{MAX}		500		pA
Input Voltage Range			−15		+13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15 V to 13 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Input Impedance				10^{13}||3.3		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = −10 V to +10 V;				
		R_L = 2 kΩ	12	50		V/mV
		R_L = 10 kΩ	50	200		V/mV
		R_L = 100 kΩ	300	2000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	200	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	14.975	14.988		V
		T_{MIN} to T_{MAX}	14.970	14.985		V
		I_{SOURCE} = 2.5 mA	14.80	14.85		V
		T_{MIN} to T_{MAX}	14.75	14.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		−14.985	−14.975	V
		T_{MIN} to T_{MAX}		−14.98	−14.97	V
		I_{SINK} = 2.5 mA		−14.88	−14.85	V
		T_{MIN} to T_{MAX}		−14.86	−14.8	V
Short Circuit Limit	I_{SC}	Sink/source, T_{MIN} to T_{MAX}	±8	±20		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 15 V	70	80		dB
		T_{MIN} to T_{MAX}	68			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		560	625	µA
		T_{MIN} to T_{MAX}			675	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% distortion, V_O = 20 V p-p		33		kHz
Settling Time	t_S	V_{OUT} = 0 V to 10 V, to 0.01%		6		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	φo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		−123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.1		fA/√Hz
Total Harmonic Distortion	THD	f =10 kHz, V_O = 3 V rms, R_L = 10 kΩ		0.005		%

At V_S = 3.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = 25°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD824A–3 V)	V_{OS}			0.2	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		250	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		250		pA
Input Voltage Range			0		1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1 V	58	74		dB
		T_{MIN} to T_{MAX}	56			dB
Input Impedance				10^{13}||3.3		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 2.0 V;				
		R_L = 2 kΩ	10	20		V/mV
		R_L = 10 kΩ	30	65		V/mV
		R_L = 100 kΩ	180	500		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	90	250		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	2.975	2.988		V
		T_{MIN} to T_{MAX}	2.97	2.985		V
		I_{SOURCE} = 2.5 mA	2.8	2.85		V
		T_{MIN} to T_{MAX}	2.75	2.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/source		±8		mA
	I_{SC}	Sink/source, T_{MIN} to T_{MAX}		±6		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V,	70			dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	V_O = 0.2 V, T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% distortion, V_O = 2 V p-p		300		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 2.5 V, to 0.01%		2		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	φo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_n			0.8		fA/√Hz
Total Harmonic Distortion	THD	f = 10 kHz, R_L = ∞, A_V = +1		0.01		%

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Supply Voltage	±18 V
Input Voltage	$-V_S$ – 0.2 V to $+V_S$
Differential Input Voltage	±30 V
Output Short Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Absolute maximum ratings apply to packaged parts unless otherwise noted.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
14-Lead SOIC (R)	120	36	°C/W

[1] θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for device soldered in circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

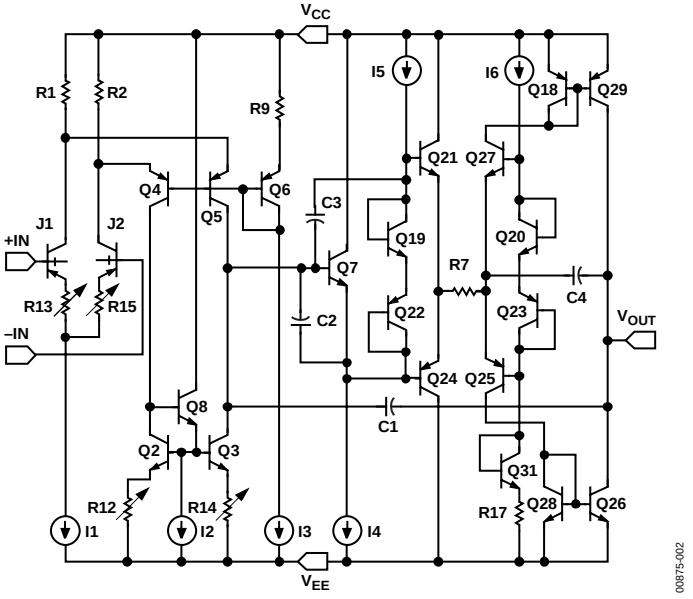
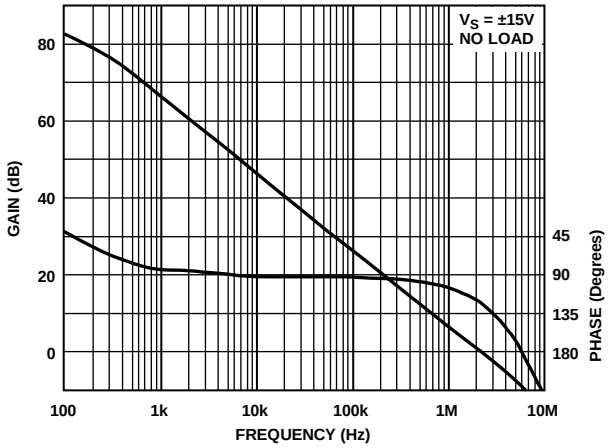


Figure 2. Simplified Schematic of 1/4 AD824

TYPICAL PERFORMANCE CHARACTERISTICS



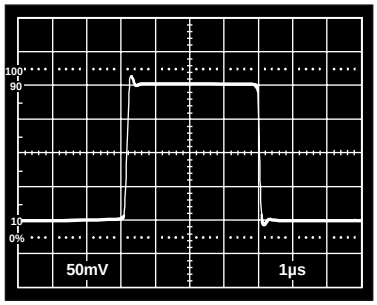
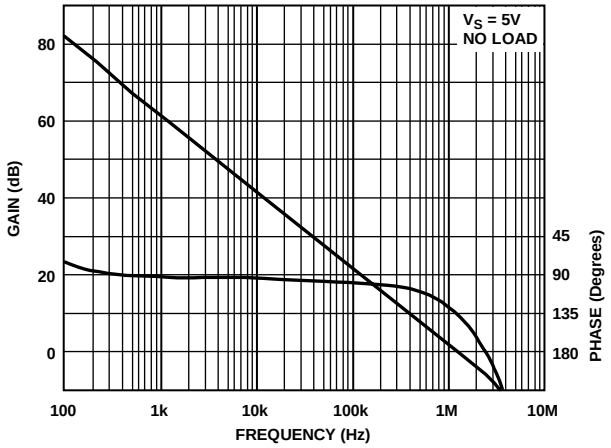


Figure 3. Open-Loop Gain/Phase and Small Signal Response, V_S = ±15 V, No Load



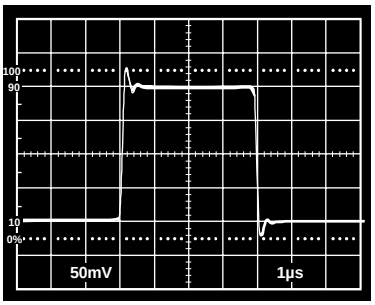
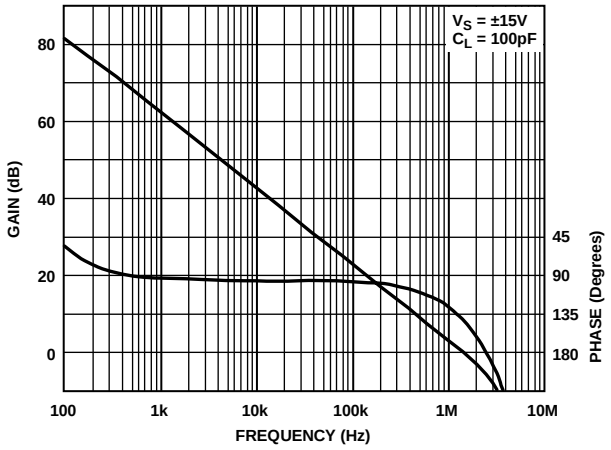


Figure 5. Open-Loop Gain/Phase and Small Signal Response, V_S = 5 V, No Load



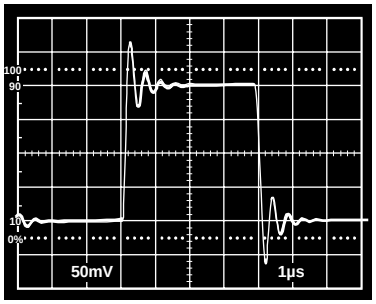
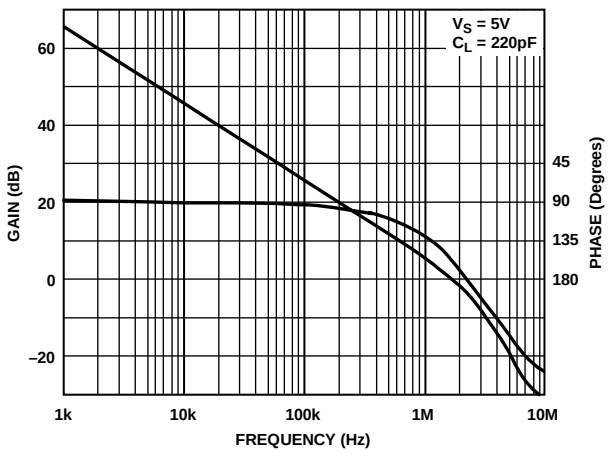


Figure 4. Open-Loop Gain/Phase and Small Signal Response, V_S = ±15 V, C_L = 100 pF



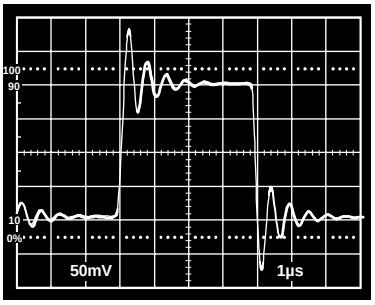
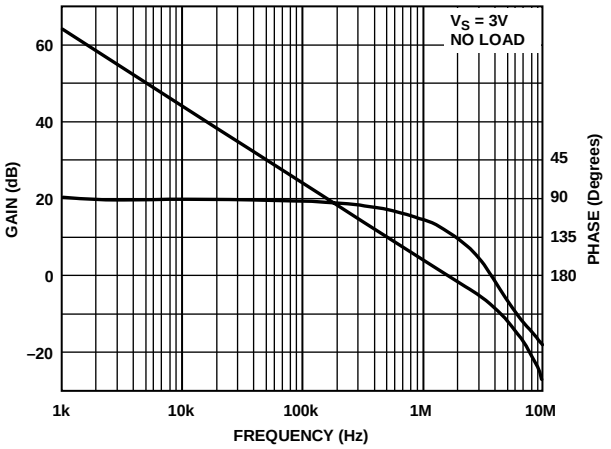


Figure 6. Open-Loop Gain/Phase and Small Signal Response, V_S = 5 V, C_L = 220 pF



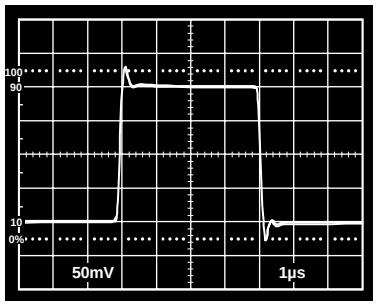
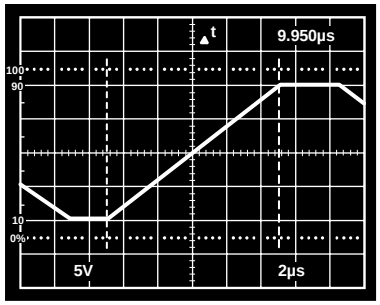


Figure 7. Open-Loop Gain/Phase and Small Signal Response, V_S = 3 V, No Load



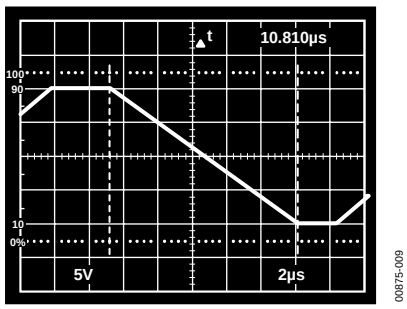
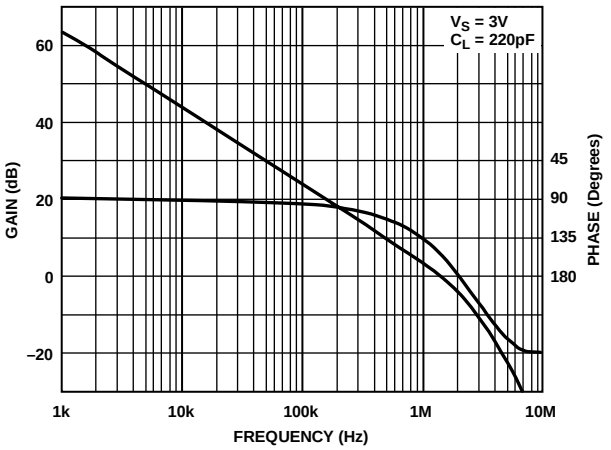


Figure 9. Slew Rate, R_L = 10 kΩ



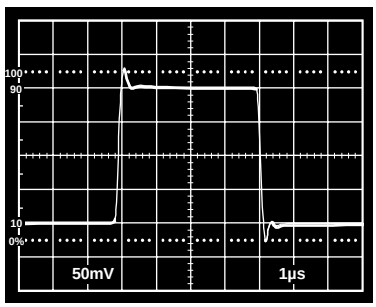


Figure 8. Open-Loop Gain/Phase and Small Signal Response, V_S = 3 V, C_L = 220 pF

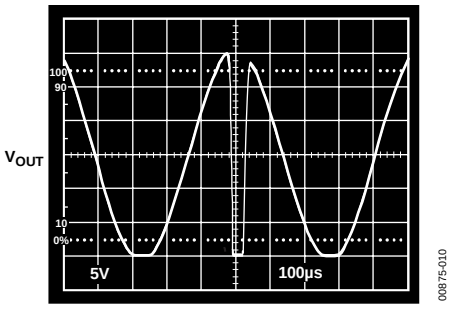


Figure 10. Phase Reversal with Inputs Exceeding Supply by 1 V

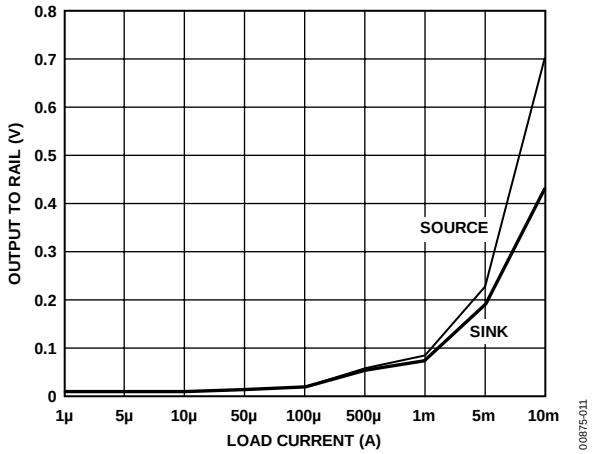


Figure 11. Output Voltage to Supply Rail vs. Sink and Source Load Currents

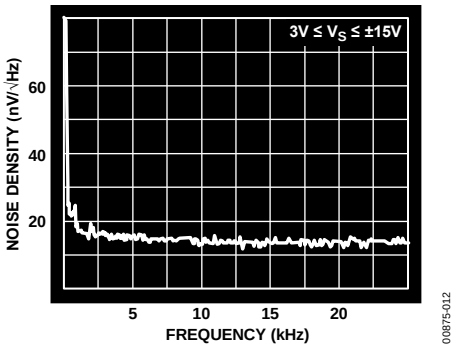


Figure 12. Voltage Noise Density

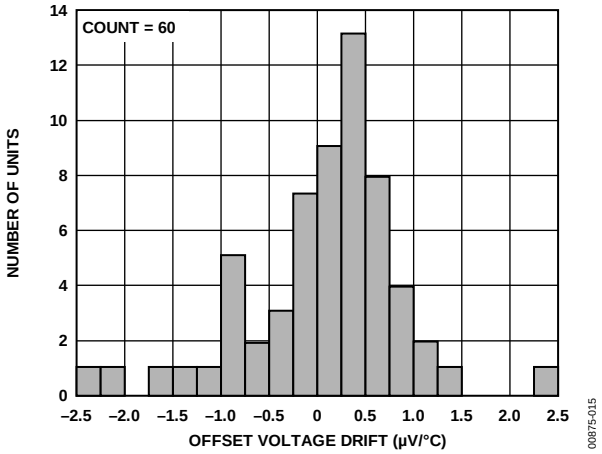


Figure 15. TC V_{OS} Distribution, −55°C to +125°C, V_S = 5 V, 0 V

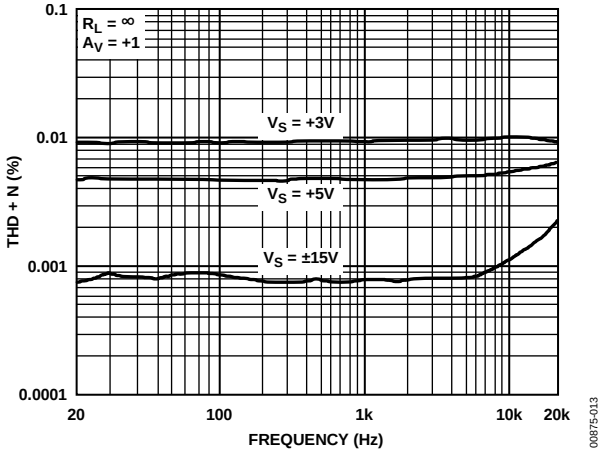


Figure 13. Total Harmonic Distortion

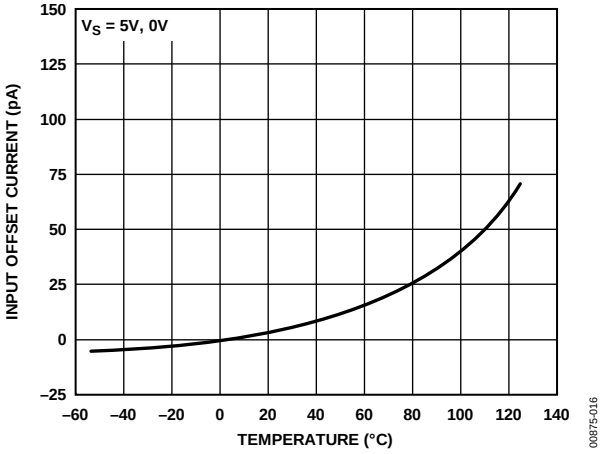


Figure 16. Input Offset Current vs. Temperature

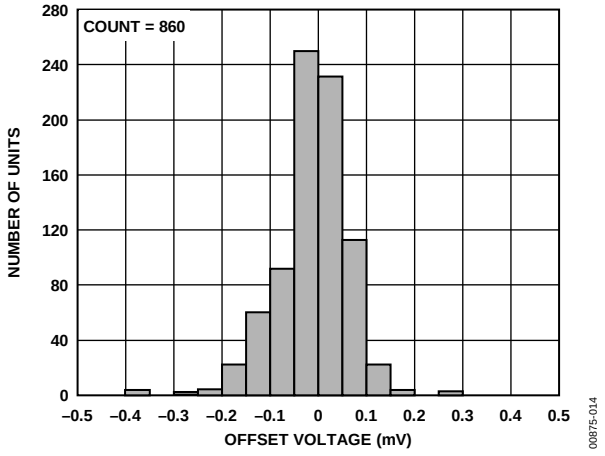


Figure 14. Input Offset Distribution, V_S = 5 V, 0 V

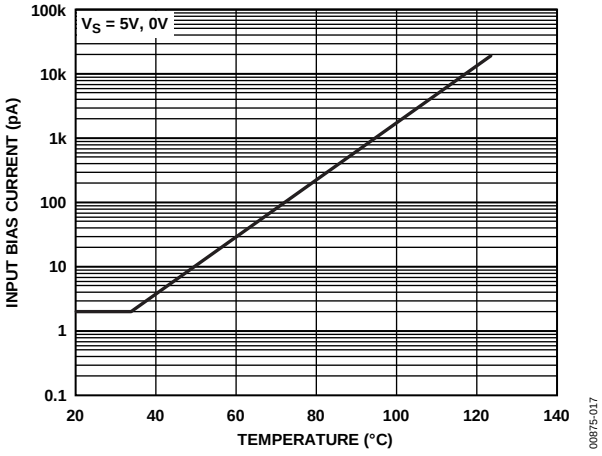


Figure 17. Input Bias Current vs. Temperature

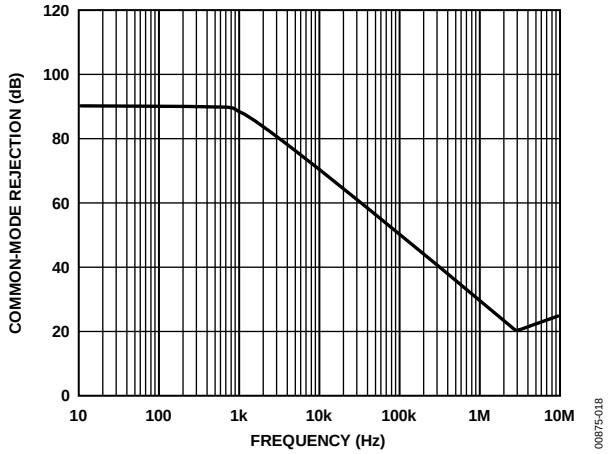


Figure 18. Common-Mode Rejection vs. Frequency

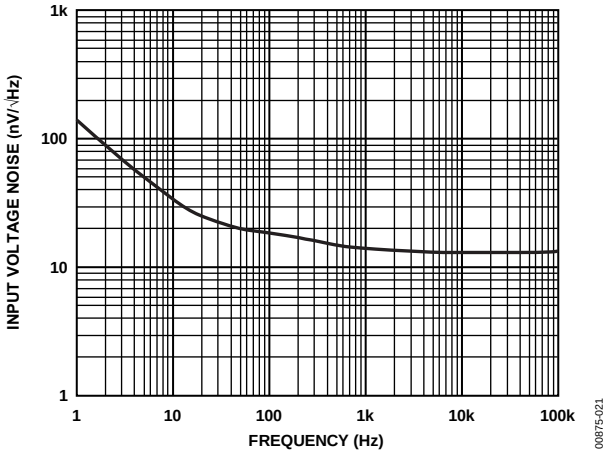


Figure 21. Input Voltage Noise Spectral Density vs. Frequency

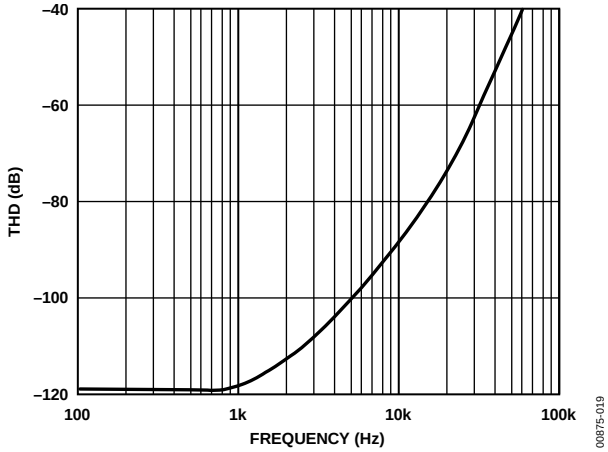


Figure 19. THD vs. Frequency, 3 V rms

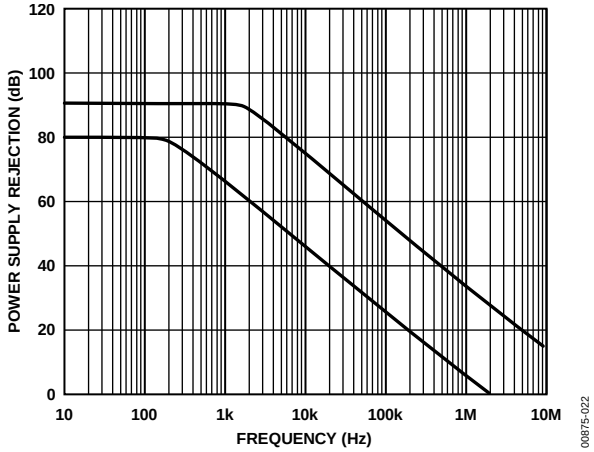


Figure 22. Power Supply Rejection vs. Frequency

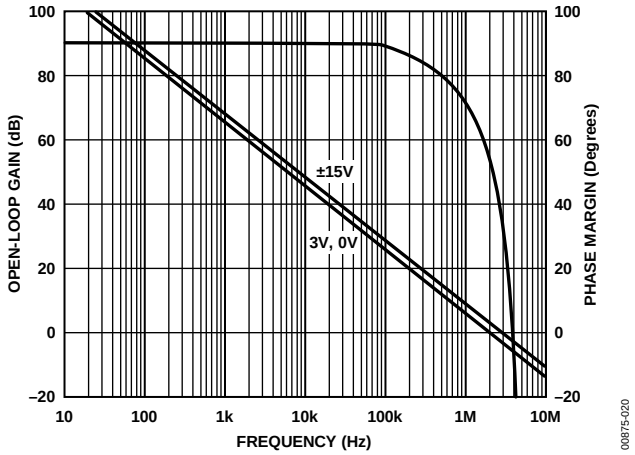


Figure 20. Open-Loop Gain and Phase vs. Frequency

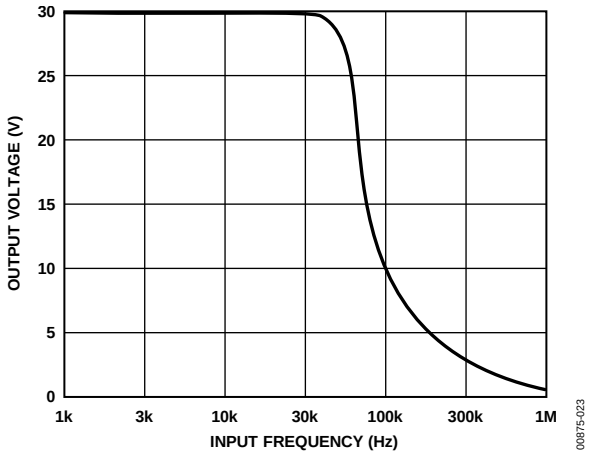


Figure 23. Large Signal Frequency Response

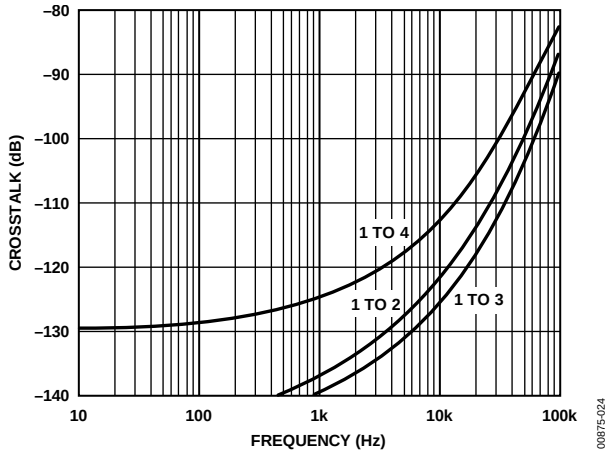


Figure 24. Crosstalk vs. Frequency

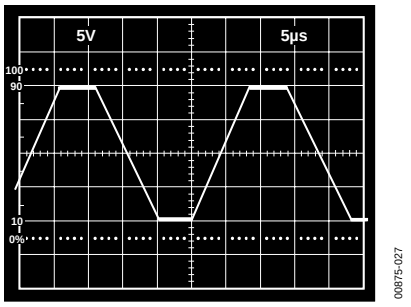


Figure 27. Large Signal Response

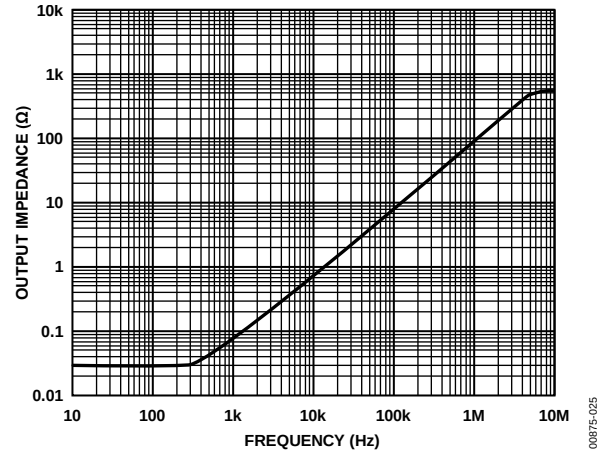


Figure 25. Output Impedance vs. Frequency, Gain = +1

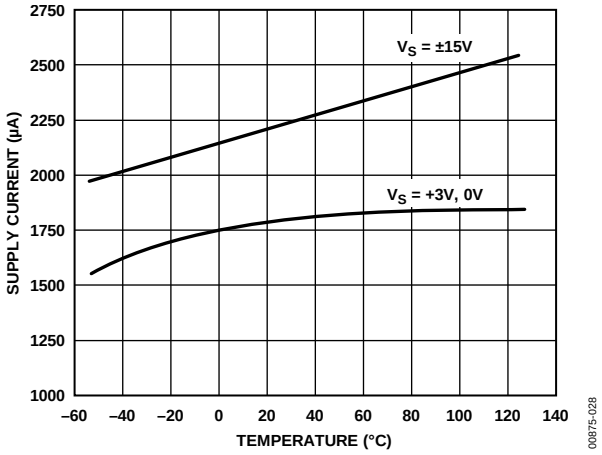


Figure 28. Supply Current vs. Temperature

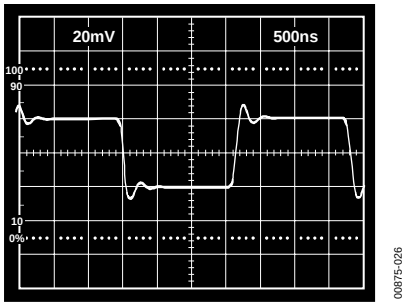


Figure 26. Small Signal Response, Unity Gain Follower, 10 kΩ||100 pF Load

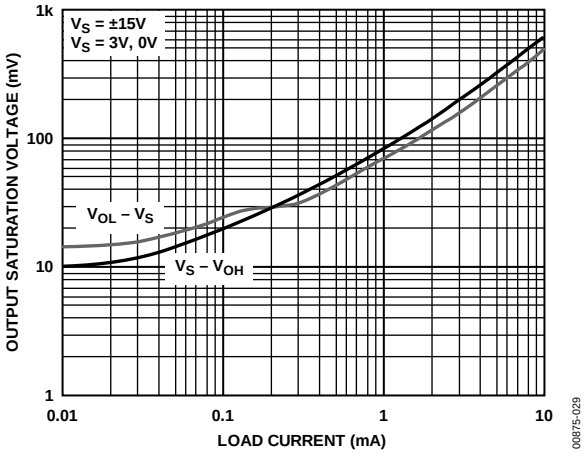


Figure 29. Output Saturation Voltage

THEORY OF OPERATION

INPUT CHARACTERISTICS

In the AD824, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail causes a loss of amplifier bandwidth.

The AD824 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 30a shows the response of an AD824 voltage follower to a 0 V to 5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output waveform. For input voltages greater than $+V_S$, a resistor in series with the noninverting input prevents phase reversal at the expense of greater input voltage noise. This is illustrated in Figure 30b.

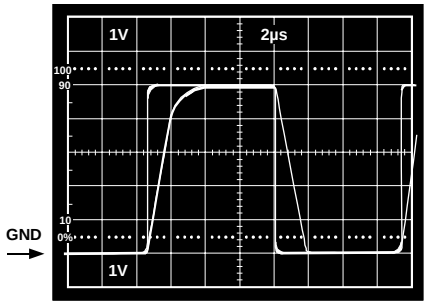


Figure 30. (a) Response with $R_P = 0$; V_{IN} from 0 V to $+V_S$; (b) $V_{IN} = -200$ V to $+V_S + 200$ mV; $V_{OUT} = 0$ V to $+V_S$; $R_P = 49.9$ kΩ

Because the input stage uses n-channel JFETs, input current during normal operation is positive; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current reverses direction as internal device junctions become forward biased. This is illustrated in Figure 10.

Use a current-limiting resistor in series with the input of the AD824 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV or if an input voltage will be applied to the AD824 when $\pm V_S = 0$ V. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 V of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 V below the $-V_S$ as long as the total voltage from the $+V_S$ to the input terminal is less than 36 V. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

OUTPUT CHARACTERISTICS

The unique bipolar rail-to-rail output stage of the AD824 swings within 15 mV of the positive and negative supply voltages. The approximate output saturation resistance of the AD824 is 100 Ω for both sourcing and sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, the saturation voltage is 0.5 V from either supply with a 5 mA current load.

For load resistances over 20 kΩ, the input error voltage of the AD824 is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the output of the AD824 is overdriven to saturate either of the output devices, the amplifier will recover within 2 µs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 6 and Figure 8 show the pulse response of the AD824 as a unity gain follower driving 220 pF. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

Figure 31 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit drives 5,000 pF with a 10% overshoot.

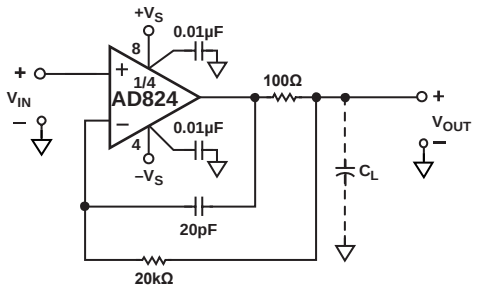


Figure 31. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

APPLICATIONS INFORMATION

SINGLE SUPPLY VOLTAGE-TO-FREQUENCY CONVERTER

The circuit shown in Figure 32 uses the AD824 to drive a low power timer, which produces a stable pulse of width, t_1. The positive going output pulse is integrated by R1 and C1 and used as one input to the AD824, which is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD824 output drives the timer trigger input, closing the overall feedback loop.

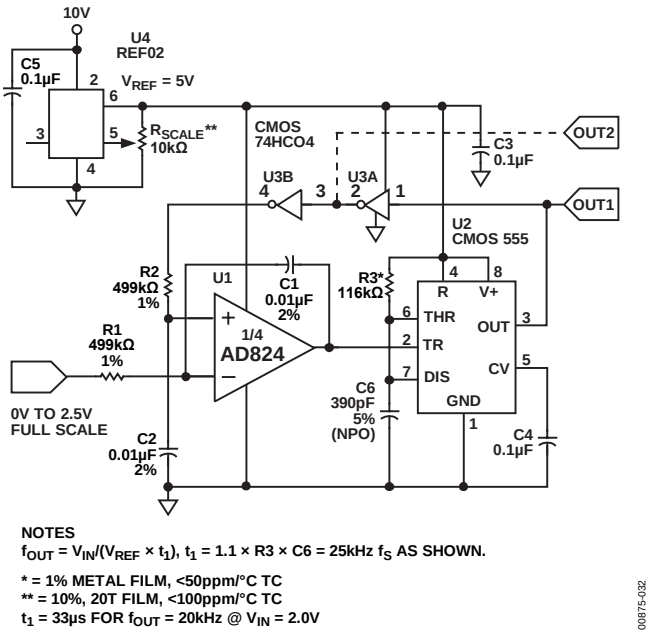


Figure 32. Single Supply Voltage-to-Frequency Converter

Typical AD824 bias currents of 2 pA allow MΩ range source impedances with negligible dc errors. Linearity errors of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 V single supply, which delivers less than 3 mA to the entire circuit.

SINGLE SUPPLY PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The AD824 can be configured as a single supply instrumentation amplifier that is able to operate from single supplies down to 5 V or dual supplies up to ±15 V. AD824 FET inputs bias currents of 2 pA minimize offset errors caused by high unbalanced source impedances.

An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser-trimmed to ratio match to 0.01% and have a maximum differential TC of 5 ppm/°C.

Table 6. AD824 In Amp Performance

Parameter	V_S = 3 V, 0 V	V_S = ±5 V
CMRR	74 dB	80 dB
Common-Mode Voltage Range	−0.2 V to +2 V	−5.2 V to +4 V
3 dB BW		
G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$		
2 V Step (V_S = 0 V, 3 V)	2 µs	
5 V (V_S = ± 5 V)		5 µs
Noise @ f = 1 kHz		
G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 µV/√Hz	2.2 µV/√Hz

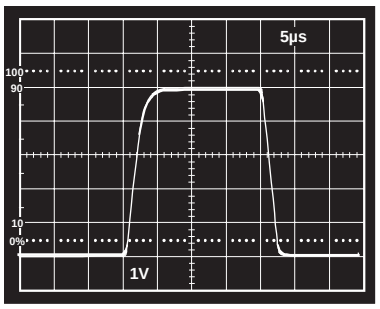


Figure 33. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = 5 V, 0 V; Gain = 10

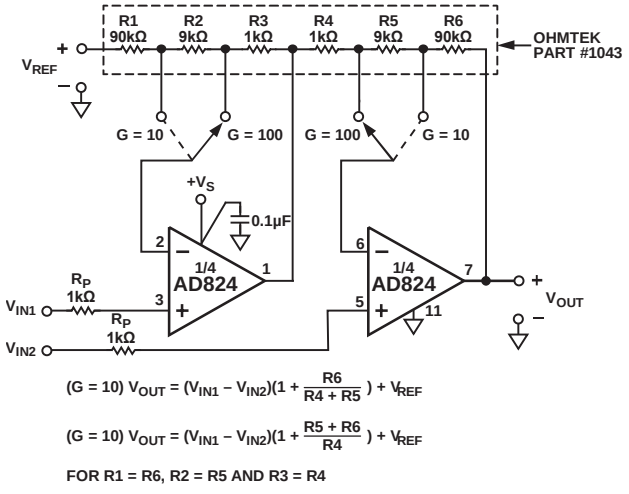


Figure 34. A Single Supply Programmable Instrumentation Amplifier

3 V, SINGLE SUPPLY STEREO HEADPHONE DRIVER

The AD824 exhibits good current drive and THD + N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD + N) equals −62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single supply op amps that consume more power and cannot run on 3 V power supplies.

In Figure 35, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (1.5 V). The gain is 1.5. Each half of the AD824 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones, which can be modeled as 32 Ω load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz to 20 kHz) are delivered to the headphones.

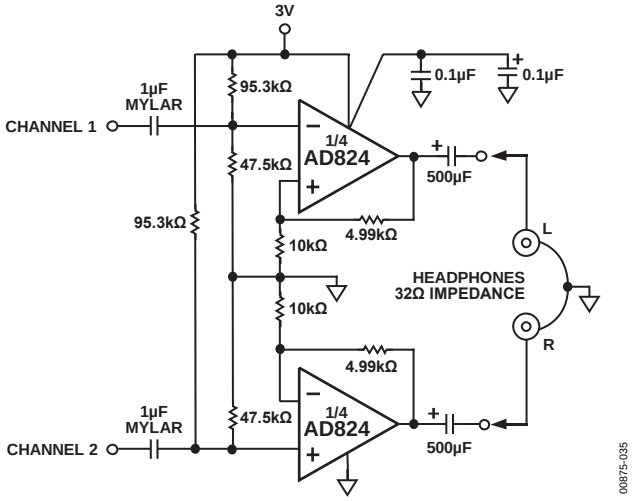


Figure 35. 3 Volt Single Supply Stereo Headphone Driver

LOW DROPOUT BIPOLAR BRIDGE DRIVER

The AD824 can be used for driving a 350 Ω Wheatstone bridge. Figure 36 shows one half of the AD824 being used to buffer the AD589—a 1.235 V low power reference. The output of 4.5 V can be used to drive an ADC front end. The other half of the AD824 is configured as a unity-gain inverter and generates the other bridge input of –4.5 V. Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor R_G and determined by:

$$G = \frac{49.4\ \text{k}\Omega}{R_G} + 1$$

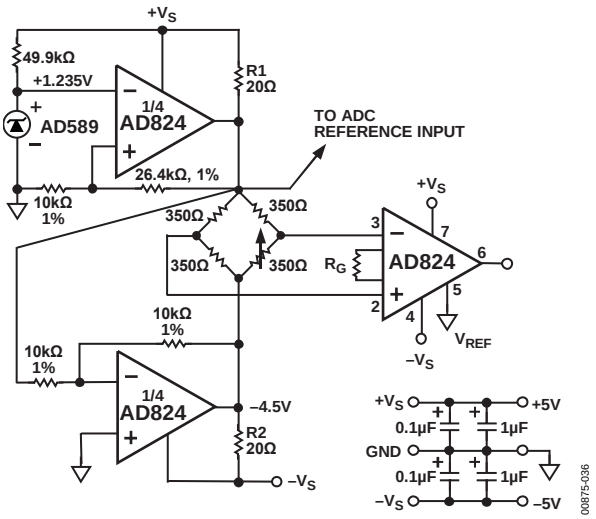


Figure 36. Low Dropout Bipolar Bridge Driver

A 3.3 V/5 V PRECISION SAMPLE-AND-HOLD AMPLIFIER

In battery-powered applications, low supply voltage operational amplifiers are required for low power consumption. Also, low supply voltage applications limit the signal range in precision analog circuitry. Circuits like the sample-and-hold circuit shown in Figure 37 illustrate techniques for designing precision analog circuitry in low supply voltage applications. To maintain high signal-to-noise ratios (SNRs) in a low supply voltage application requires the use of rail-to-rail, input/output operational amplifiers. This design highlights the ability of the AD824 to operate rail-to-rail from a single 3 V/5 V supply, with the advantages of high input impedance. The AD824, a quad JFET-input op amp, is well suited to sample-and-hold circuits due to its low input bias currents (3 pA, typical) and high input impedances (3×10^{13} Ω, typical). The AD824 also exhibits very low supply currents so the total supply current in this circuit is less than 2.5 mA.

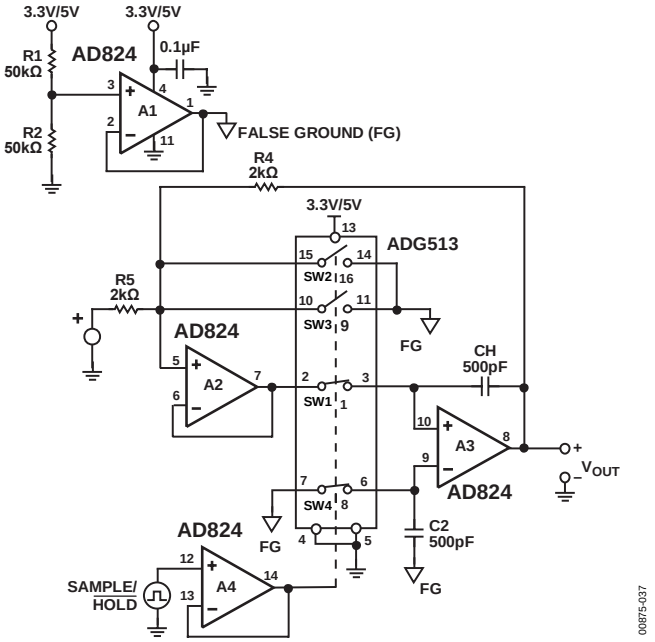


Figure 37. 3.3 V/5.5 V Precision Sample-and-Hold Circuit

In many single supply applications, the use of a false ground generator is required. In this circuit, R1 and R2 divide the supply voltage symmetrically, creating the false ground voltage at one-half the supply. Amplifier A1 then buffers this voltage creating a low impedance output drive. The sample-and-hold circuit is configured in an inverting topology centered around this false ground level.

A design consideration in sample-and-hold circuits is voltage droop at the output caused by op amp bias and switch leakage currents. By choosing an JFET op amp and a low leakage CMOS switch, this design minimizes droop rate error to better than 0.1 µV/µs in this circuit. Higher values of CH will yield a lower droop rate. For best performance, CH and C2 should be polystyrene, polypropylene or Teflon capacitors.

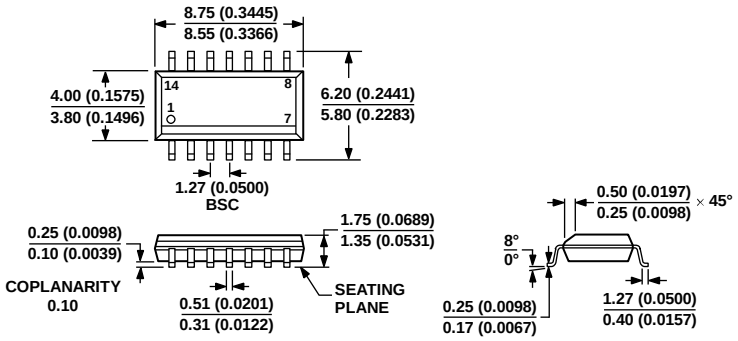
These types of capacitors exhibit low leakage and low dielectric absorption. Additionally, 1% metal film resistors were used throughout the design.

In the sample mode, SW1 and SW4 are closed, and the output is $V_{OUT} = -V_{IN}$. The purpose of SW4, which operates in parallel with SW1, is to reduce the pedestal, or hold step, error by injecting the same amount of charge into the noninverting input of A3 that SW1 injects into the inverting input of A3. This creates a common-mode voltage across the inputs of A3 and is then rejected by the CMR of A3; otherwise, the charge injection from SW1 creates a differential voltage step error that appears at V_{OUT}. The pedestal error for this circuit is less than 2 mV over the entire 0 V to 3.3 V/5 V signal range. Another method of reducing pedestal error is to reduce the pulse amplitude applied to the control pins. To control the ADG513, only 2.4 V are required for the on state and 0.8 V for the off state. If possible, use an input control signal whose amplitude ranges from 0.8 V to 2.4 V instead of a full range 0 V to 3.3 V/5 V for minimum pedestal error.

Other circuit features include an acquisition time of less than 3 µs to 1%; reducing CH and C2 will speed up the acquisition time further, but an increased pedestal error will result. Settling time is less than 300 ns to 1%, and the sample-mode signal BW is 80 kHz.

The ADG513 was chosen for its ability to work with 3 V/5 V supplies and for having normally open and normally closed precision CMOS switches on a dielectrically isolated process. SW2 is not required in this circuit; however, it was used in parallel with SW3 to provide a lower R_{ON} analog switch.

OUTLINE DIMENSIONS



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060606-A

Figure 38. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD824AR-14	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824AR-14-3V	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824AR-14-3V-REEL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824AR-14-REEL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824AR-14-REEL7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824ARZ-14	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824ARZ-14-3V	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824ARZ-14-3V-RL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824ARZ-14-REEL	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
AD824ARZ-14-REEL7	−40°C to +85°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14

[1] Z = RoHS Compliant Part.

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