ESD8106

ESD Protection Diode

Low Capacitance ESD Protection for USB 3.0 Interface

The ESD8106 surge protection is specifically designed to protect USB 3.0 interfaces by integrating two Superspeed pairs, D+ and D− lines into a single protection product. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

Features

- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.0

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

ON Semiconductor®

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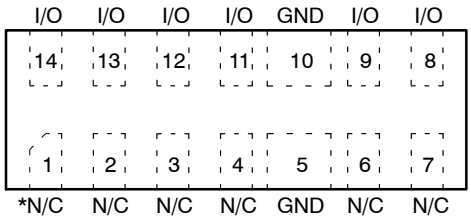
UDFN14
CASE 517CQ

MARKING DIAGRAM

6D = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONFIGURATION



*Pins 1−7 should be connected to opposite pin with PCB trace in order to maintain a flow−thru routing scheme.

ORDERING INFORMATION

Device	Package	Shipping
ESD8106MUTAG	UDFN14 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

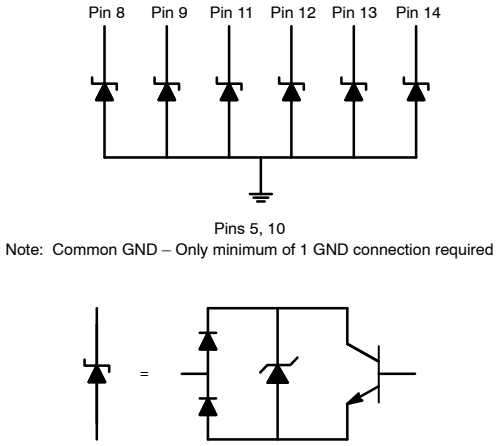


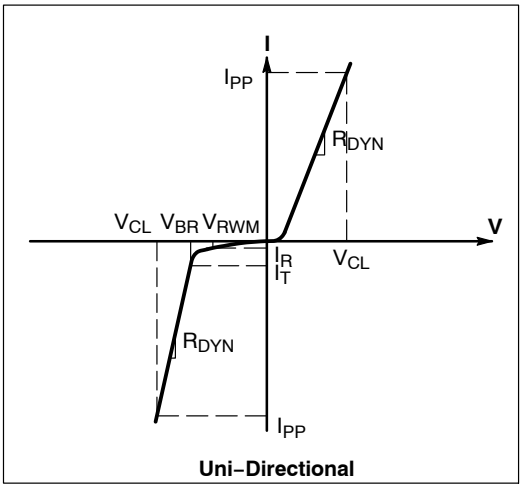
Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
R_{DYN}	Dynamic Resistance

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	4.0	5.0		V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			1.0	μA
Dynamic Resistance	R_{DYN}	(Note 1)		0.45		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND V_R = 0 V, f = 1 MHz between I/O Pins V_R = 0 V, f = 1 MHz, T_A = 65°C between I/O Pins and GND		0.30 0.10 0.37	0.35 0.20 0.47	pF

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

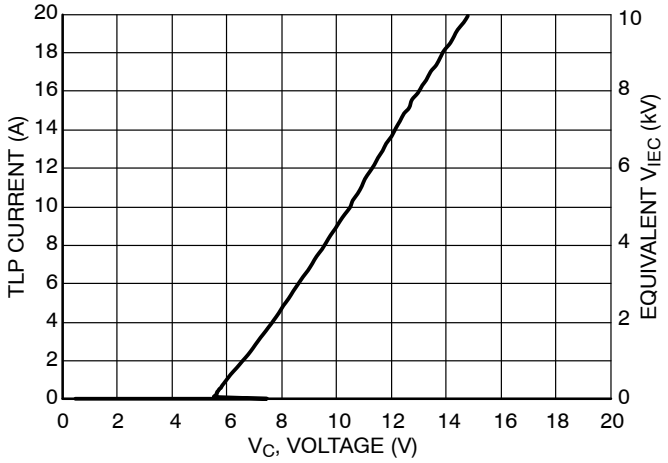


Figure 2. TLP I–V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 3. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 4 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and high to interpret them please see AND9007/D.

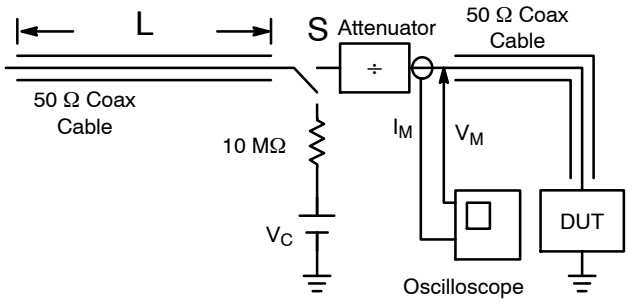


Figure 3. Simplified Schematic of a Typical TLP System

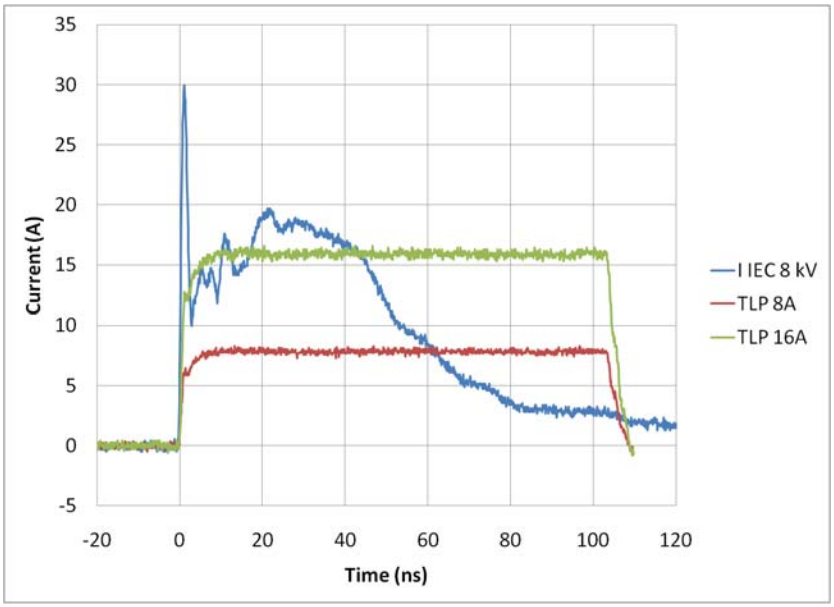


Figure 4. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

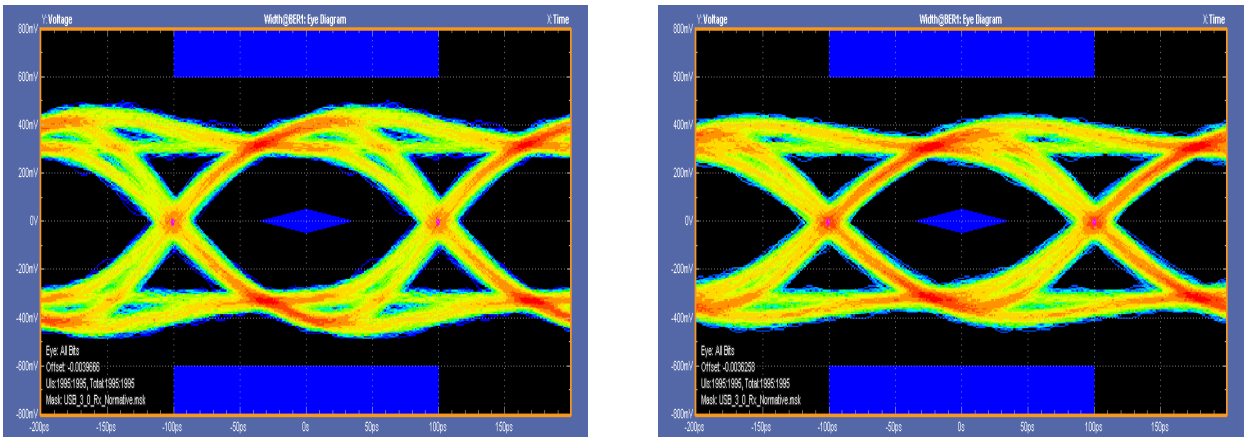
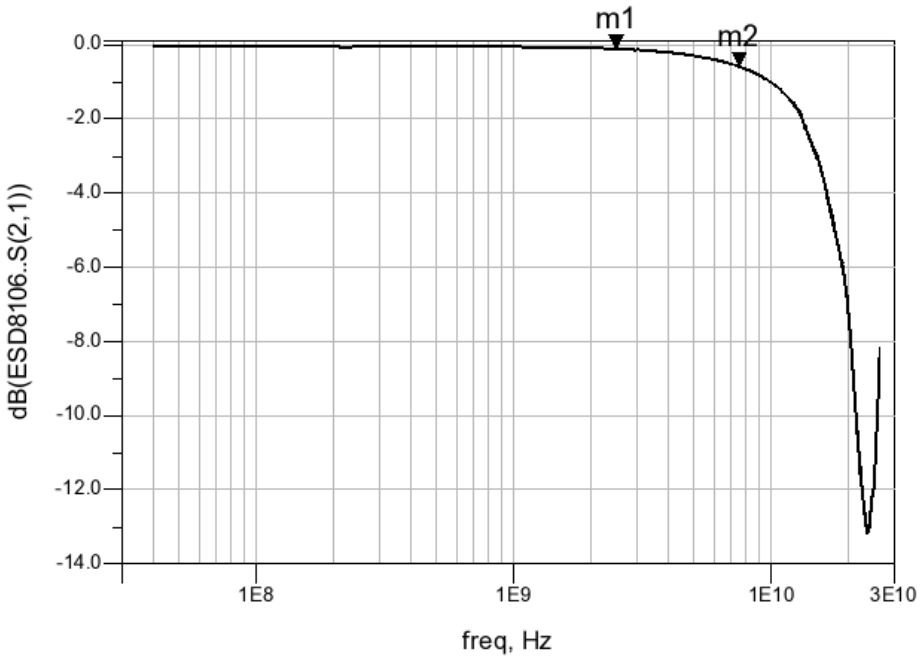


Figure 5. USB 3.0 Eye Diagram with and without ESD8106. 5.0 Gb/s, 400 mV_{PP}



Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3rd Harmonic Frequency (GHz)	ESD8106 Insertion Loss (dB)
USB 3.0	5	2.5 (m1)	7.5 (m2)	m1 = 0.100 m2 = 0.580

Figure 6. ESD8106 Insertion Loss

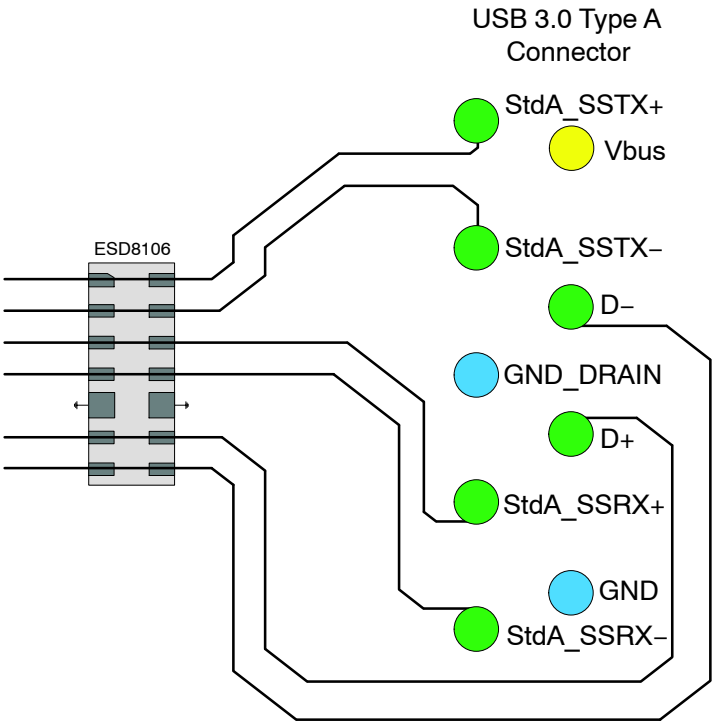


Figure 7. Recommended USB 3.0 Layout Diagram

PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
  - In USB 3.0 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in Figure 8.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - Use curved traces when possible to avoid unwanted reflections.
  - Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

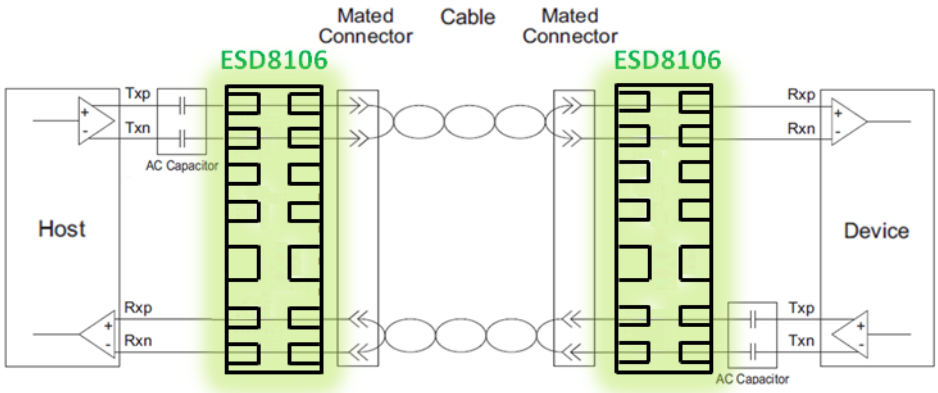


Figure 8. USB 3.0 Connection Diagram

ESD Protection Device Technology

ON Semiconductor's portfolio contains three main technologies for low capacitance ESD protection device which are highlighted below and in Figure 9.

- ESD7000 series: Zener diode based technology. This technology has a higher breakdown voltage (VBR) limiting it to protecting chipsets with larger geometries.
- ESD8000 series: Silicon controlled rectifier (SCR) type technology. The key advatange for this technology is a low holding voltage (VH) which produces a deeper snapback that results in lower voltage over high currents as shown in the TLP results in Figure 10. This technology provides optimized protection for chipsets with small geometries against thermal failures resulting in chipset damage (also known as "hard failures").
- ESD8100 series: Low voltage punch through (LVPT) technology. The key advatange for this technology is a very low turn-on voltage as shown in Figure 11. This technology provides optimized protection for chipsets with small geometries against recoverable failures due to voltage peaks (also known as "soft failures").

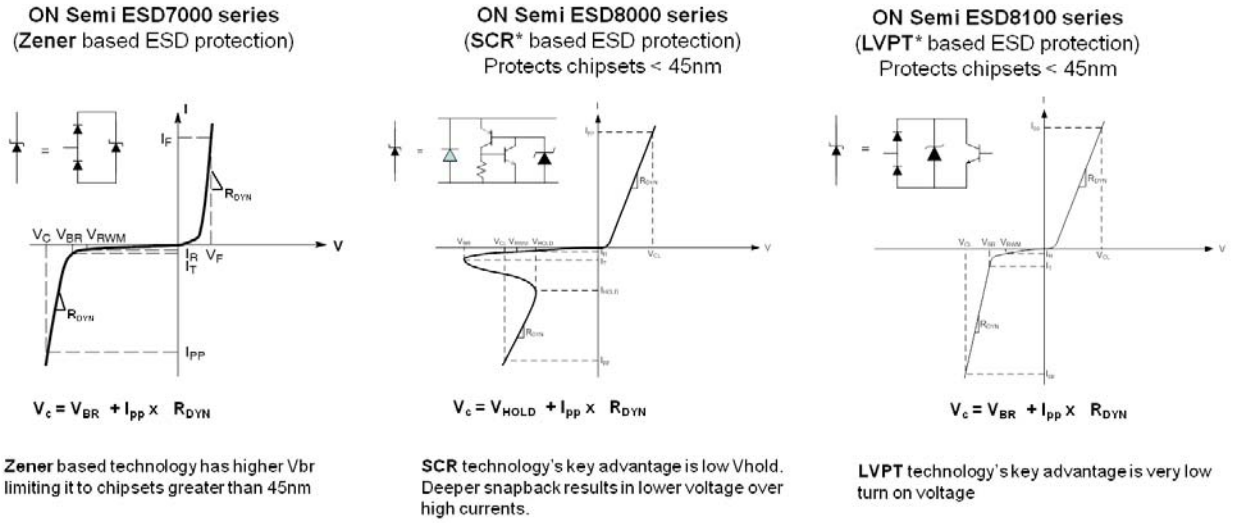


Figure 9. ON Semiconductor's Low-cap ESD Technology Portfolio

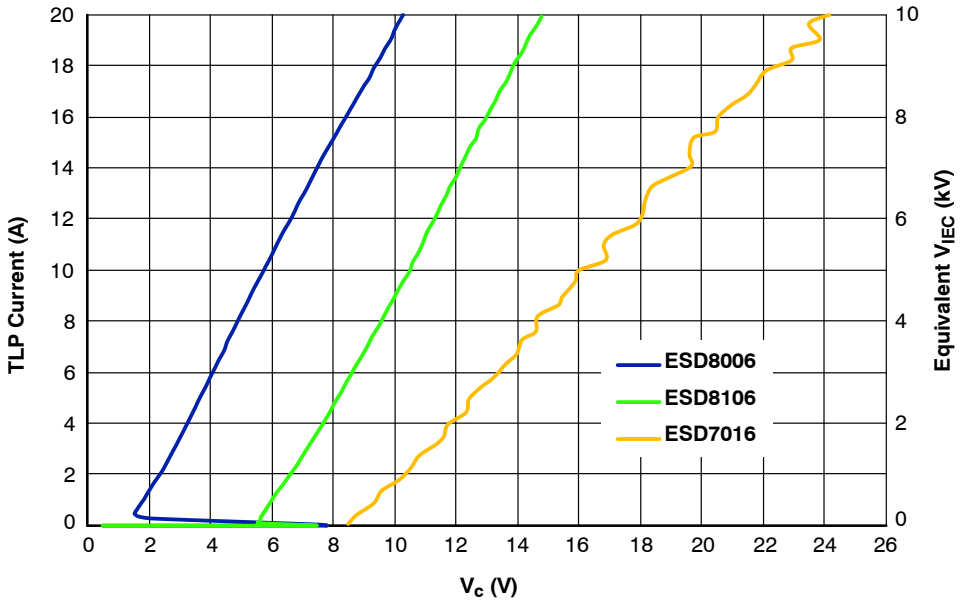


Figure 10. High Current, TLP, IV Characteristic of Each Technology

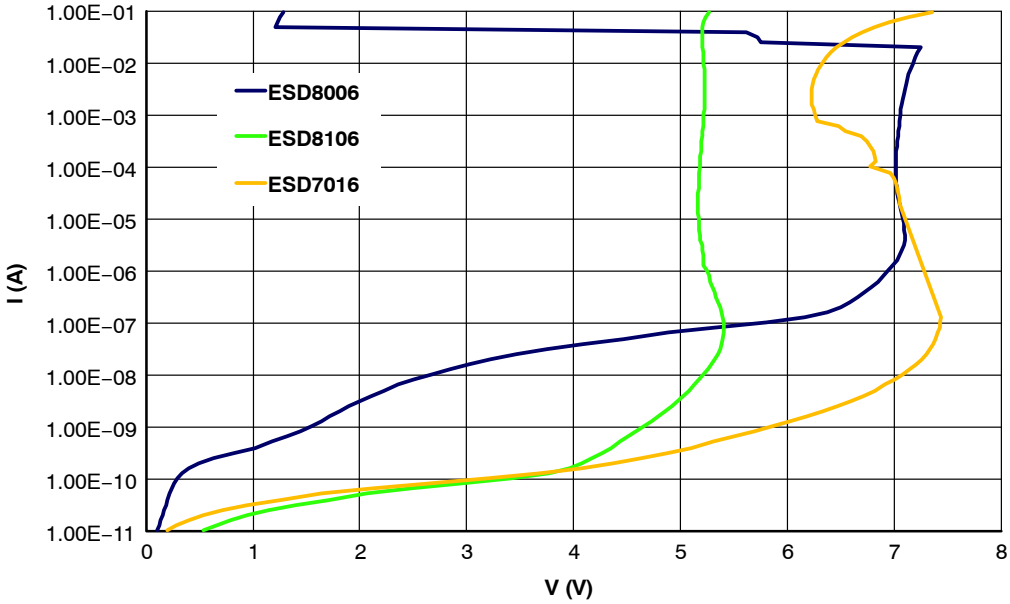


Figure 11. Low Current, DC, IV Characteristic of Each Technology

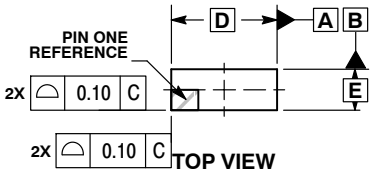
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

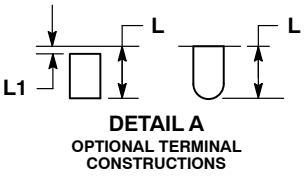
ON Semiconductor®

SCALE 2:1

UDFN14, 3.5x1.35, 0.5P
CASE 517CQ
ISSUE O

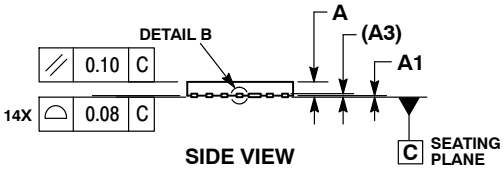
DATE 17 JAN 2013

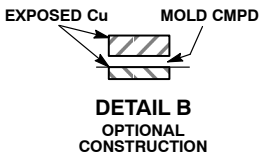


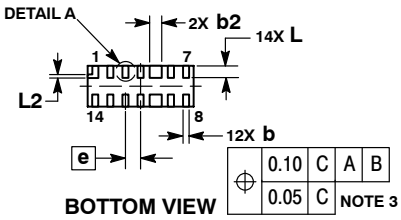


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.

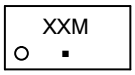
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
b2	0.35	0.45
D	3.50 BSC	
E	1.35 BSC	
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.20 REF	







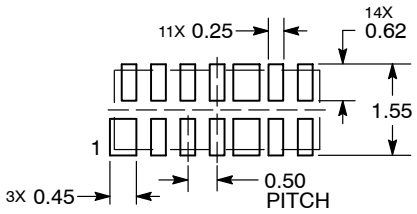
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN14, 3.5X1.35, 0.5P	PAGE 1 OF 1

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