SiT9156

LVPECL, LVDS Oscillator (XO) with 0.3 ps Jitter for 10Gb Ethernet

The Smart Timing Choice™

Features

- 0.3 ps RMS phase jitter (random) for 10GbE applications
- Frequency stability as low as ±10 PPM
- 100% drop-in replacement for quartz and SAW oscillators
- Configurable positive frequency shift, +25, +50, or +75 PPM
- Industry-standard packages: 5.0 mm x 3.2 mm and 7.0 mm x 5.0 mm
- Industrial and extended commercial temperature ranges
- Best in class 1-year and 10-year aging
- Best resilience, up to 40x better than quartz
- For other frequencies, refer to SiT9121 or 9122 datasheet

Applications

- 10Gb Ethernet, XAUI
- Telecom, networking, broadband, instrumentation, storage, Server

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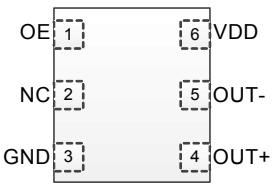
Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common AC Characteristics						
Output Frequency Range	f	156.25000, 156.253906, 156.257812, 156.261718, 161.132800			MHz	156.253906 MHz, +25 PPM from 156.250000 156.257812 MHz, +50 PPM from 156.250000 156.261718 MHz, +75 PPM from 156.250000
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations
		-25	–	+25	PPM	
		-50	–	+50	PPM	
First Year Aging		-2	–	+2	PPM	25°C
10-year Aging		-5	–	+5	PPM	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	–	10	ms	
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
LVPECL, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Maximum Output Current	I-driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	115	ns	
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications
LVDS, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Differential Output Voltage	VOD	200	350	500	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	495	600	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	115	ns	
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications

Pin Description

Pin	Map	Functionality	
1	OE	Input	H or Open: specified frequency output L: output is high impedance
2	NC	NA	Do Not Connect; Leave it floating
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Termination Diagrams

LVPECL:

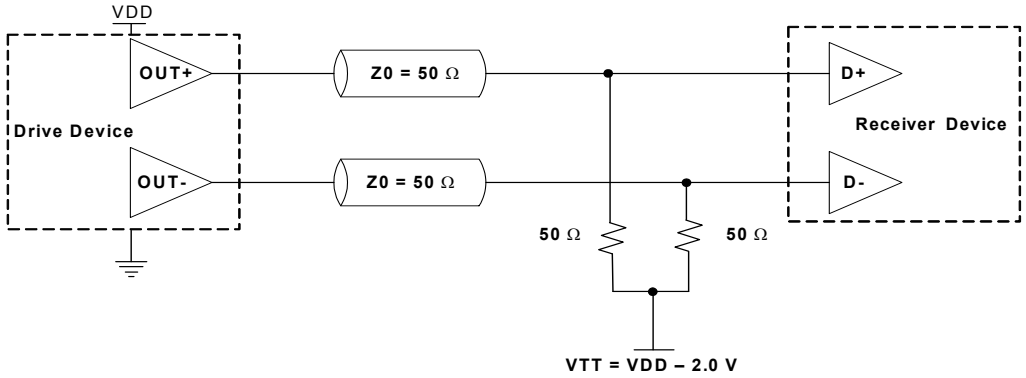


Figure 1. LVPECL Typical Termination

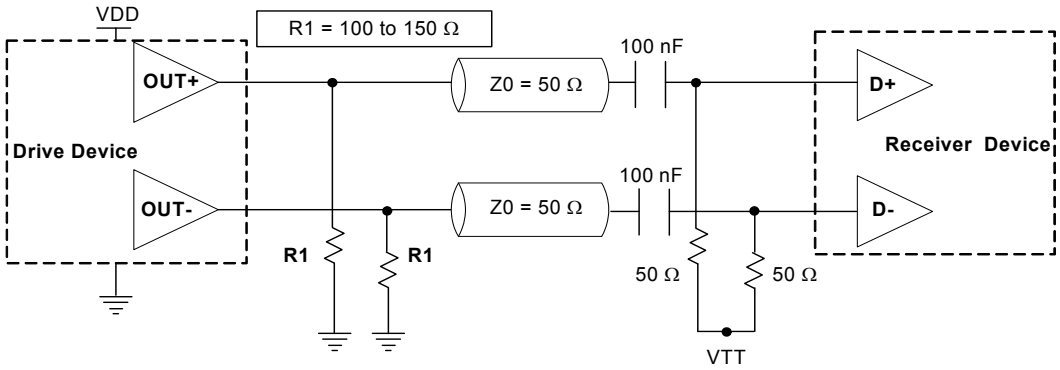


Figure 2. LVPECL AC Coupled Termination

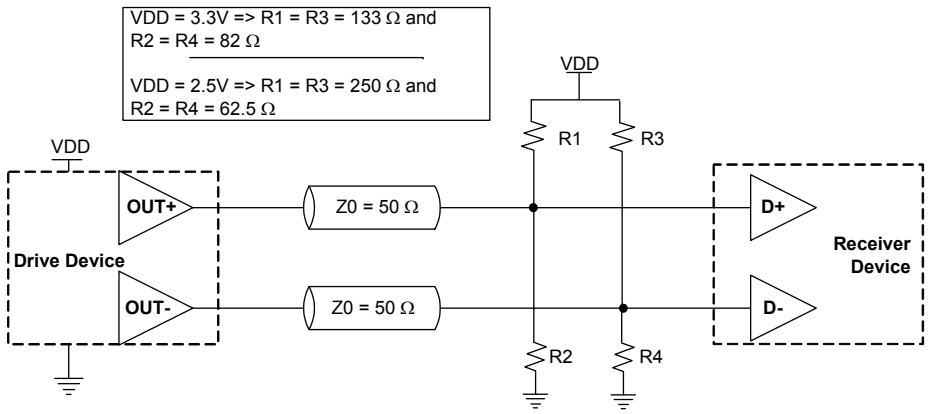


Figure 3. LVPECL with Thevenin Typical Termination

LVDS:

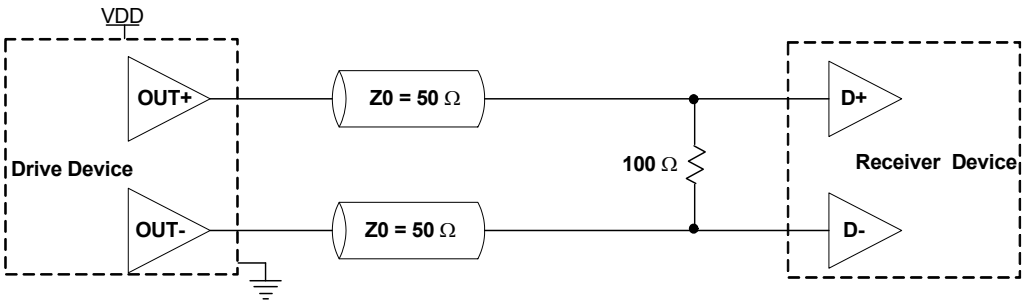
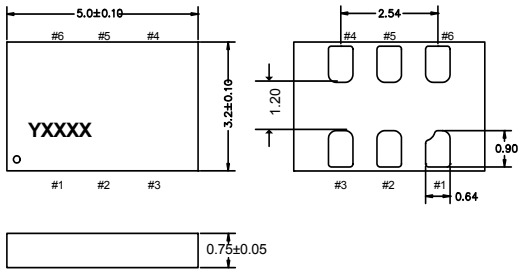
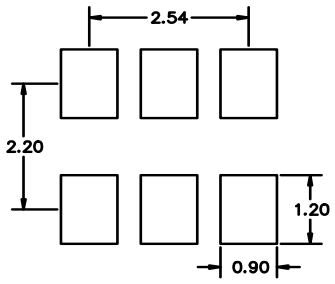
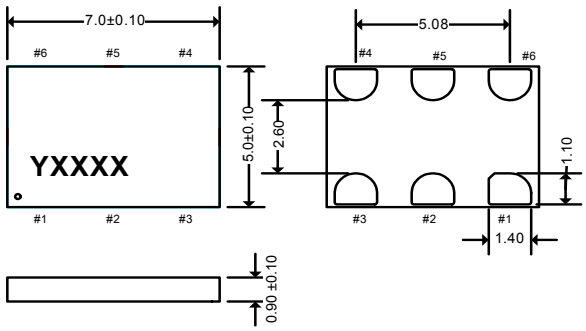
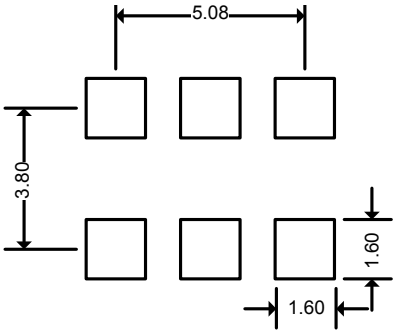


Figure 4. LVDS Single Termination (Load Terminated)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information