CN0269: 18-Bit, 1.33 MSPS, 16-Channel Data Acquisition System

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OVERVIEW FUNCTION & BENEFITS DETAILS COMMON VARIATIONS HOW TO TEST SAMPLE & BUY

OVERVIEW

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Circuit Note PDF, 11/2013 (pdf, 1177 kB)

Benefits & Features

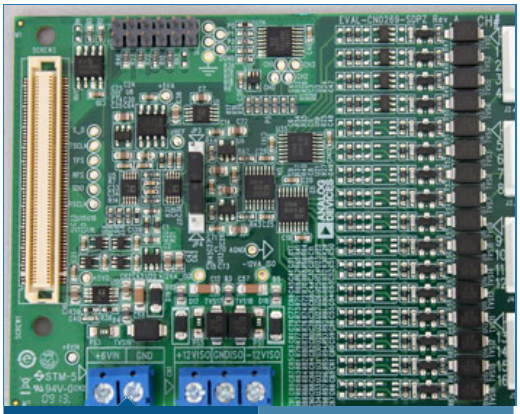
- 18-Bit, 16-Channel Data Acquisition
- 16 single-ended, 8 differential inputs
- 1.33MSPS sampling rate
- 250kHz channel switching rate

Products Used

AD7984 AD8065 AD8475
ADG5208 ADG5236 ADR444

Applications:

- Programmable Logic Controllers/ Distributed Control Systems
- Electronic Test & Measurement



HARDWARE BLOCK DIAGRAM

BETA Use in Signal Chain Designer

Design Resources

Design & Integration Files

- Schematic
- Bill of Materials
- Gerber Files
- PADS Files
- Assembly Drawing

Download Design Files (3266 kB)

Evaluation Hardware

Part numbers with "Z" indicate RoHS Compliance.
Boards checked are needed to evaluate this circuit.

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Check Inventory & Purchase

FPGA HDL

AD7984 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
BeMicro FPGA Project for AD7984 with Nios driver

Connectivity Options

This circuit supports 3rd party connectivity.

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a high performance industrial signal level multichannel data acquisition circuit that has been optimized for fast channel-to-channel switching. It can process 16-channels of single-ended inputs or 8-channels of differential inputs with up to 18-bit resolution.

A single channel can be sampled at up to 1.33 MSPS with 18-bit resolution. A channel-to-channel switching rate of 250 kHz between all input channels provides 16-bit performance.

The signal processing circuit combined with a simple 4-bit up-down binary counter provides a simple and cost effective way to realize channel-to-channel switching without an FPGA, CPLD, or high speed processor. The counter can be programmed to count up or count down for sequentially sampling multiple channels, or can be loaded with a fixed binary word for sampling a single channel.

This circuit is an ideal solution for a multichannel data acquisition card for many industrial applications including process control, and power line monitoring.

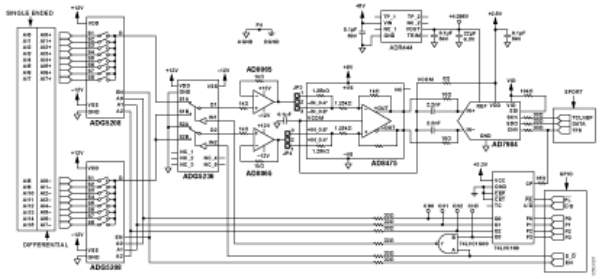

Figure 1. Multichannel Data Acquisition Circuit (Simplified Schematic: All Components, Connections, and Decoupling Not Shown)

Enlarge

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is a classic multichannel nonsynchronous data acquisition signal chain consisting of a multiplexer, amplifiers, and an ADC.

The architecture allows fast sampling of multiple channels using a single ADC, providing low cost and excellent channel-tochannel matching.

Channel-to-channel switching speed is limited by the settling time of the various components following the multiplexer in the signal chain, because the multiplexer can present a full-scale step voltage output to the downstream amplifier and ADC. The components in this circuit have been specifically chosen to minimize the settling time and maximize channel-to-channel switching speed.

Component Selection

The ADG5208 multiplexer switches one of eight inputs to a common output, as determined by the 3-bit binary address lines. The ADG5236 contains two independently selectable single-pole/double throw (SPDT) switches. Two ADG5208 switches, combined with one ADG5236, allow 16 single-ended channels or 8 true differential channels to be connected to the rest of the signal chain using a 4-bit digital control signal.

The 4-bit digital signal is generated by a 4-bit binary up/down counter triggered by the same signal used for the convert (CNV) input to the 18-bit, 1.33 MSPS AD7984 ADC.

The AD8065 JFET input op amp has a 145 MHz bandwidth and is configured as a unity-gain buffer to provide excellent settling time performance and extremely high input impedance. The AD8065 also provides very low impedance output to drive the AD8475 funnel amp attenuation stage.

The advantages of fully differential signal chain are good common-mode rejection and reduction in second-order distortion products. In order to process ±10 V industrial level signals by modern low voltage differential input ADCs, the attenuation and level shifting stage is necessary.

The AD8475, fully differential, attenuating (funnel) amplifier with integrated precision gain resistors provides precision attenuation (by 0.4× or 0.8×), common-mode level shifting, and singleended-to-differential conversion along with input overvoltage protection. Fast settling time (50 ns to 0.001%), and low noise performance (10 nV/√Hz) make the AD8475 well suited to drive 18-bit differential input ADCs at sampling rates up to 4 MSPS.

The AD7984, 18-bit, PulSAR® ADC selected in this circuit provides 18-bit resolution at 1.33 MSPS when sampling a single channel. However, the settling time of various components in the signal chain limit the overall accuracy when sequentially switching between channels. For example, 16-bit performance is achieved when switching between channels at a 250 kHz rate.

For a detailed timing and noise analysis of the circuit, please refer to the CN0269 PDF.

Histogram Test Results

Figure 16 shows the results of a 10,000 sample histogram taken by shorting the 16 single-ended channels together and connecting them to the GND of the PCB. Note that the peak-to-peak noise is approximately 12 LSBs, including the input buffer.

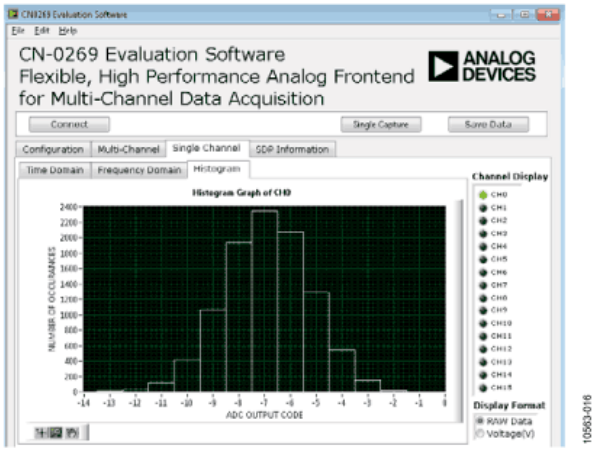

Figure 16. DC Histogram at 0 V Input, 1 MSPS Sampling Rate, 10,000 Samples

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AC Test Results

The ac performance was tested at the system level with the AD7984 sampling at 300 kSPS with 2.5 V p-p 10.675 kHz input sine wave signal provided by a Type 1051 B&K sine generator,. The circuit was sampling continuously on Channel 4, and does not include the effects of the input buffer. The FFT shows an SNR = 91.33 dBFS.

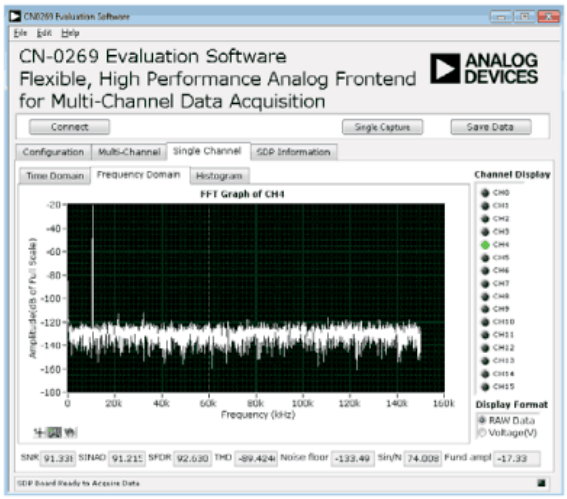

Figure 17. FFT with a Kaiser Window (Parameter = 20), 2.5 V p-p 10.675 kHz Input, 300 kSPS Sampling Rate on CH4 Without Input Buffer

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Switching Speed and Settling Time Test Results

The follow figures show the settling performance. The lab test setup is shown in Figure 18.

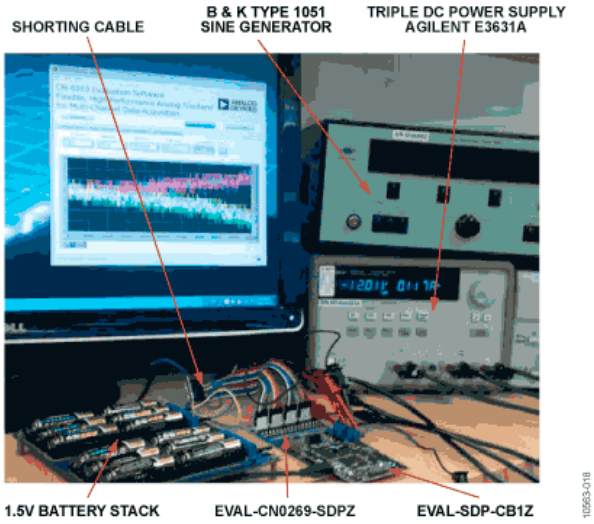

Figure 18. Switching Speed and Settling Time Lab Test Setup

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The CN-0269 evaluation board was configured in the 16-channel singled input mode, the 8 odd channels were shorted together, and the 8 even channels were shorted together.

A battery stack was used to generate the different dc input voltages for low noise and low impedance.

The odd and even channels were connected to different voltages. The LabVIEW™ software controls the EVAL-SDP-CB1Z channel-to-channel and switches continually between the input channels. The switching rate was varied from 100 Hz to 1 MHz in 1 kHz increments. There were 10 samples taken at each switching rate, and the results averaged. The average value at the lowest switching rate was used as a reference point. The error at each different switching rate was calculated by taking the difference between the 10-sample and the reference value. The test results are shown in Figure 19 to Figure 23.

In the figures, an error of 2 LSBs corresponds to 17-bit settling, and an error of 4 LSBs corresponds to 16-bit settling.

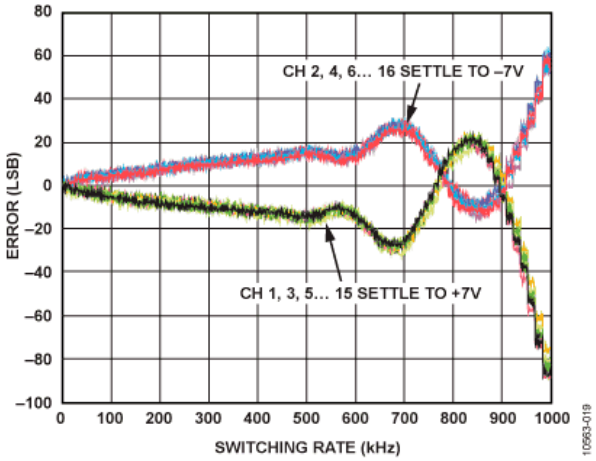

Figure 19. Errors vs. Switching Rate Without Front Buffer at 16-Channel Single-Ended, 14 V Step

Enlarge

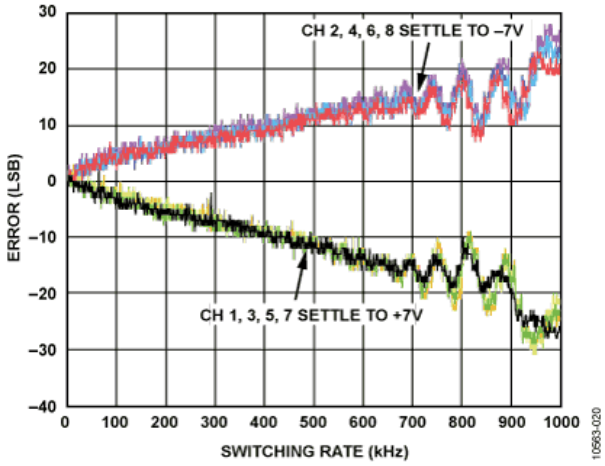

Figure 20. Errors vs. Switching Rate Without Input Buffer, 8-Channel Differential Mode, 14 V Step

Enlarge

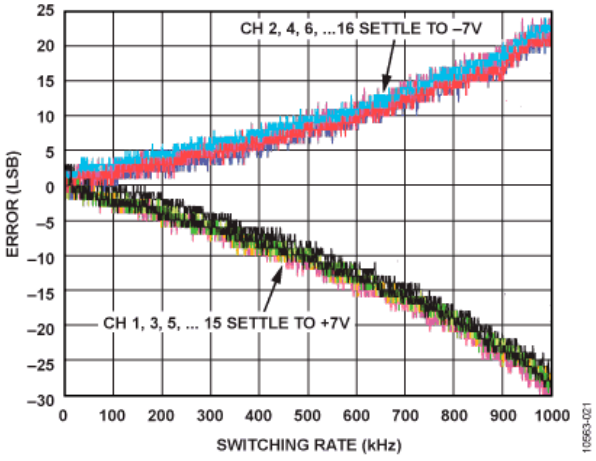

Figure 21. Errors vs. Switching Rate with Input Buffer, 16-Channel Single-Ended Mode, 14 V Step

Enlarge

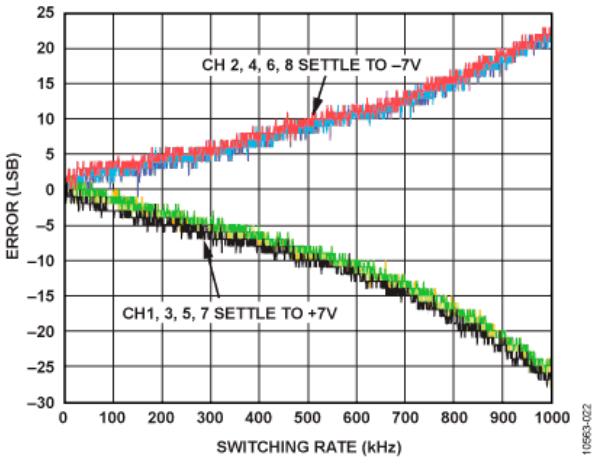

Figure 22. Errors vs. Switching Rate with Front Buffer, 8-Channel Differential Mode, 14 V Step

Enlarge

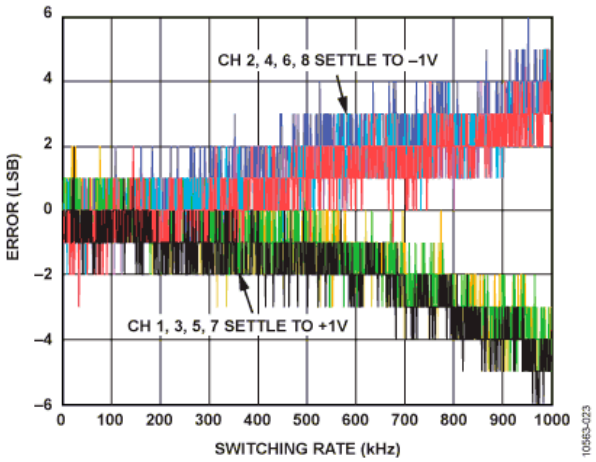

Figure 23. Errors vs. Switching Rate with Input Buffer, 8-Channel Differential Mode, 2 V Step

Enlarge

From the figures above, we can see the circuit with the input buffer has a better settling performance than the circuit without front buffer at switching rates less than 1 MHz.

Figure 21, Figure 22, and Figure 23 show that with the input buffer connected the circuit settles to 16 bits at channel-to- channel switching rates up to 250 kHz.

COMMON VARIATIONS

The 18-bit AD7984 is available in a 10-lead MSOP or a 10-lead QFN (LFCSP) package. There are a number of other PulSAR ADCs available in the same package with 14-bit, 16-bit, and 18- bit resolutions having various sampling rates.

Another possible choice for the buffer amplifiers is the AD8021. If programmable gain is required, the AD8250, AD8251, and AD8253 have 685 ns settling time to 0.001%. The ADG12xx series of multiplexers can be used if lower capacitance is required.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0269-SDPZ circuit board and the EVAL-SDP-CB1Z SDP-B System Demonstration Platform controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The EVAL-CN0269-SDPZ board contains the circuit to be evaluated, as described in this note, and the SDP-B controller board is used with the CN-0269 evaluation software to capture the data from the EVAL-CN0269-SDPZ circuit board.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP (32 bit), Windows Vista®, or Windows 7
- EVAL-CN0269-SDPZ circuit board
- EVAL-SDP-CB1Z SDP-B controller board
- CN-0269 SDP Evaluation Software

- 6 V dc (500 mA), ±12 V(300 mA) power supply
- Low distortion signal generator to provide ±10 V output with frequency from dc to 1MHz

Getting Started

Load the evaluation software by placing the CN-0269 evaluation software into the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software.

Functional Block Diagram

See Figure 1 for the circuit block diagram and the EVAL-CN0269-SDPZ-SCH-RevX.pdf file for the complete circuit schematic. This file is contained in the CN-0269 Design Support Package. A functional block diagram of the test setup is shown in Figure 24.

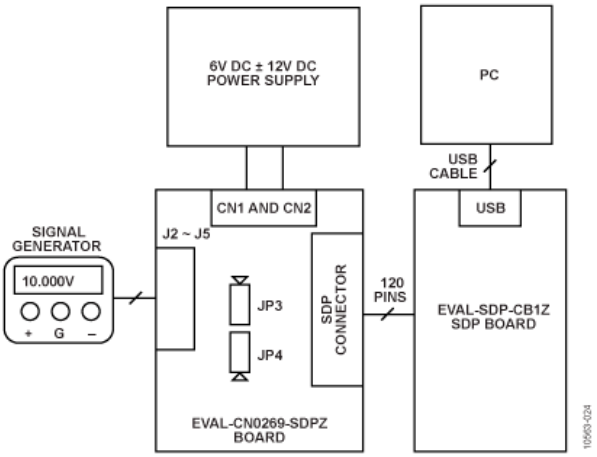

Figure 24. Test Setup Block Diagram

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Setup

Connect the 120-pin connector on the EVAL-CN0269-SDPZ circuit board to the **CON A** connector on the EVAL-SDP-CB1Z controller board (SDP-B). Use nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V and ±12 V dc power supply to the pins on CN1, CN2 marked with +6 V, ±12 V and GND on the board. If available, a 6 V wall wart can be connected to the barrel connector on the board and used in place of the 6 V power supply. Connect the USB cable supplied with the SDP-B board to the USB port on the PC. Do not connect the USB cable to the Mini-USB connector on the SDP-B board at this time. Turn on the 6 V and ±12 V power supply at the same time and then connect the USB cable to the Mini-USB connector.

Test

With the 6 V and ±12 V power supply on, launch the evaluation software. Once USB communications are established, the SDP-B board can be used to send, receive, and capture data from the EVAL-CN0269-SDPZ board and do the data analysis under time and frequency domain to evaluate the performance of the whole circuit.

Figure 25 shows a photo of the EVAL-CN0269-SDPZ evaluation board connected. Information regarding the SDP-B board can be found in the SDP-B User Guide.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0269 Software User Guide.

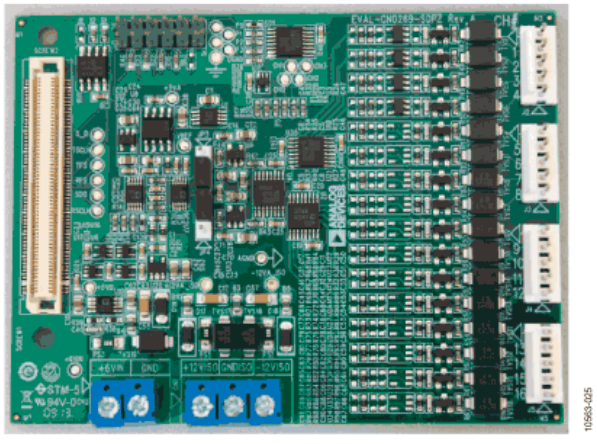

Figure 25. EVAL-CN0269-SDPZ Evaluation Board

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Connectivity for Prototype Development

The EVAL-CN0269-SDPZ evaluation board is designed to be evaluated with the EVAL-SDP-CB1Z SDP-B board based on the Black-Fin DSP through SPORT port; however, any microprocessor can be used to interface to serial port of AD7984 through the 14 pin PMOD connector. In order for another controller to be used with the EVAL-CN0269-SDPZ evaluation board, software must be developed by a third party.

There are existing interposer boards that can be used to interface to the Altera and Xilinx field programmable gate arrays (FPGAs). The BeMicro SDK board from Altera can be used with the BeMicro SDK/SDP interposer using Nios Drivers. Any Xilinx evaluation board that features the FMC connector can be used with the FMC-SDP Interposer board.

SAMPLE PRODUCTS USED IN THIS CIRCUIT

Product	Description	Available Product Models to Sample
AD7984	18-Bit, 1.33 MSPS PulSAR 10.5 mW ADC in MSOP/QFN	☐ AD7984BCPZ-RL7 ☐ AD7984BRMZ
AD8065	High Performance, 145 MHz *FastFET*™ Op Amps	☐ AD8065ARZ ☐ AD8065ARTZ-REEL7
AD8475	Precision, Selectable Gain, Fully Differential Funnel Amp	☐ AD8475ACPZ-R7 ☐ AD8475BRMZ ☐ AD8475ARMZ
ADG5208	High Voltage Latch-Up Proof, 4-/8-Channel Multiplexers	☐ ADG5208BRUZ ☐ ADG5208BCPZ-RL7
ADG5236	High Voltage Latch-Up Proof, Dual SPDT Switches	☐ ADG5236BRUZ ☐ ADG5236BCPZ-RL7
ADR444	Ultralow Noise, LDO XFET® 4.096V Voltage Reference w/Current Sink and Source	☐ ADR444ARMZ ☐ ADR444ARZ

ADD SELECTIONS TO SAMPLES CART

Evaluation Hardware

Boards checked are needed to evaluate this circuit.

Model	Description	RoHS	Check Inventory/ Purchase/Sample
EVAL-CN0269-SDPZ	18-Bit, 1.33 MSPS, 16-Channel Data Acquisition System	Yes	☒
EVAL-SDP-CB1Z	Eval Control Board	Yes	☒

Pricing displayed is based on 1-piece. The USA list pricing shown is for budgetary use only, shown in United States dollars (FOB USA per unit), and is subject to change. International prices may vary due to local duties, taxes, fees and exchange rates.

Check Inventory & Purchase