1. General description

NX20P0408 is a single chip USB data lines protection solution. D+ and D- pins in system side are protected from 28V short to VBUS, which pins are located near VBUS pins.

USB Type C allows VBUS voltage to increase up to 20V through Power delivery protocol, the concern is that these D+/D- pins can be shorted with VBUS when plugging out with mechanical twisted connector since Type C connector contact pin is 25% closer to each other than prior generation connector, micro USB which most mobile devices have been using. Another concern is that moisture or fine dust may cause short to 20V VBUS with next to pins.

NX20P0408 enables D+/D- to be robust in even abnormal conditions. NX20P0408 has 28V DC tolerant on D+/D- pin in connector side and quickly disconnects switchers if the voltage is above over voltage threshold, D+/D- in system side is protected from high voltage.

2. Features and benefits

- USB Type C D+/D- short protection to VBUS
  - CON_DP / CON_DN : $28V_{DC}$
- Low Rdson switch : 4Ω
- High switch bandwidth = 1.5GHz
- 35V surge protection on CON_DP/CON_DN
- Fast OVP turn off time : 60ns
- Post-stage clamp circuit to clamp voltage until switch is off.

3. Applications

- Smartphone
- Tablet
- Laptop

4. Ordering information

Table 1.   Ordering information

Type number	Temperature range	Name	Description	Version
NX20P0408UK	−40 °C to +85 °C	WLCSP12	Wafer level chip-size, 12 bumps; 1.27 x 1.67 x 0.525 mm (back side coating included)	NX20P0408

5. Marking

Table 2.   Marking Codes

Type number	Marking code
NX20P0408UK	N08

6. Functional Diagram
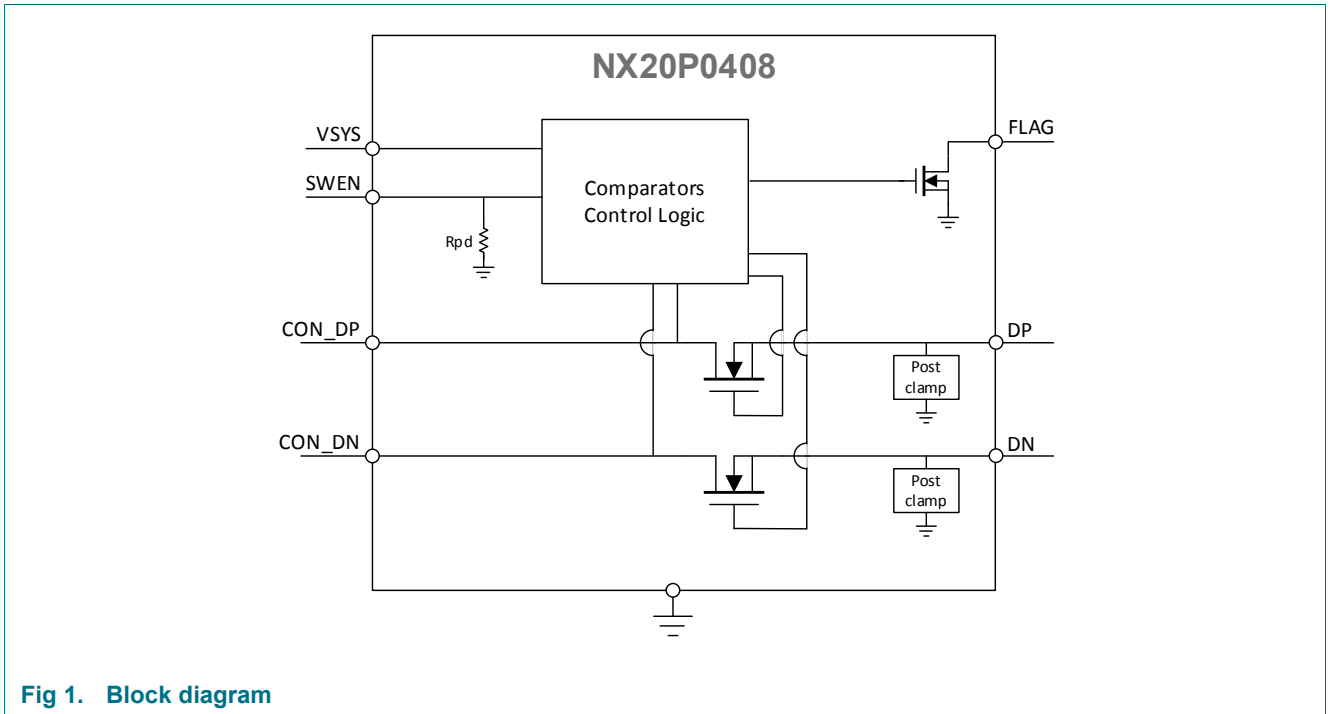
Fig 1.   Block diagram

7. Pinning information

7.1 Pinning

	1	**2**	**3**			**3**	**2**	**1**	
A	NC	NC	VSYS		**A**	VSYS	NC	NC	**A**
B	NC	NC	GND		**B**	GND	NC	NC	**B**
C	CON_DP	DP	Flag		**C**	Flag	DP	CON_DP	**C**
D	CON_DN	DN	SWEN		**D**	SWEN	DN	CON_DN	**D**

Pin Map Bump-side down   **Pin Map Bump-side Up**

Fig 2.   NX20P0408, WLCSP12
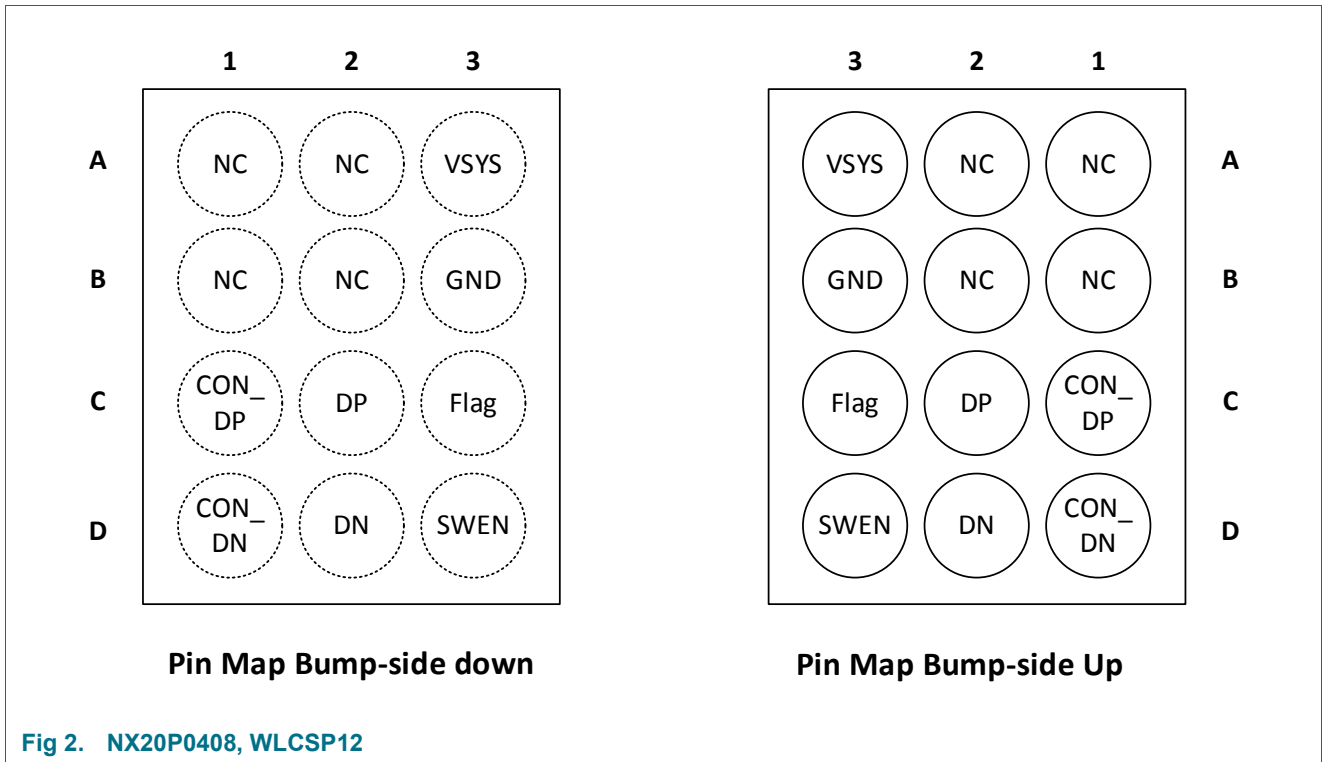
7.2 Pin description

Table 3.   Pin description

Symbol	Pin	Type	Description
CON_DP	C1	DIO	Type C connector side DP. Connect DP of Type C USB connector.
CON_DN	D1	DIO	Type C connector side DN. Connect DN of Type C USB connector.
DP	C2	DIO	System side DP.
DN	D2	DIO	System side DN.
SWEN	D3	DI	USB switch enable/disable control pin. SWEN is driven high to enable USB switch. There is internal pull-down resistor, 460Kohm.
VSYS	A3	P	Power supply input, connect System voltage and bypass 1uF capacitor to GND.
FLAG	C3	DO	Open-drain output indicating fault condition. Low when Fault condition happen. External pull-up resistor is required.
GND	B3	P	Ground
NC	A1, A2, B1, B2		No connection. Leave them open.

8. Functional description

NX20P0408 is placed in front of Type C connector and protects D+ and D- pins in System side from 20V VBUS short, ESD and Surge.
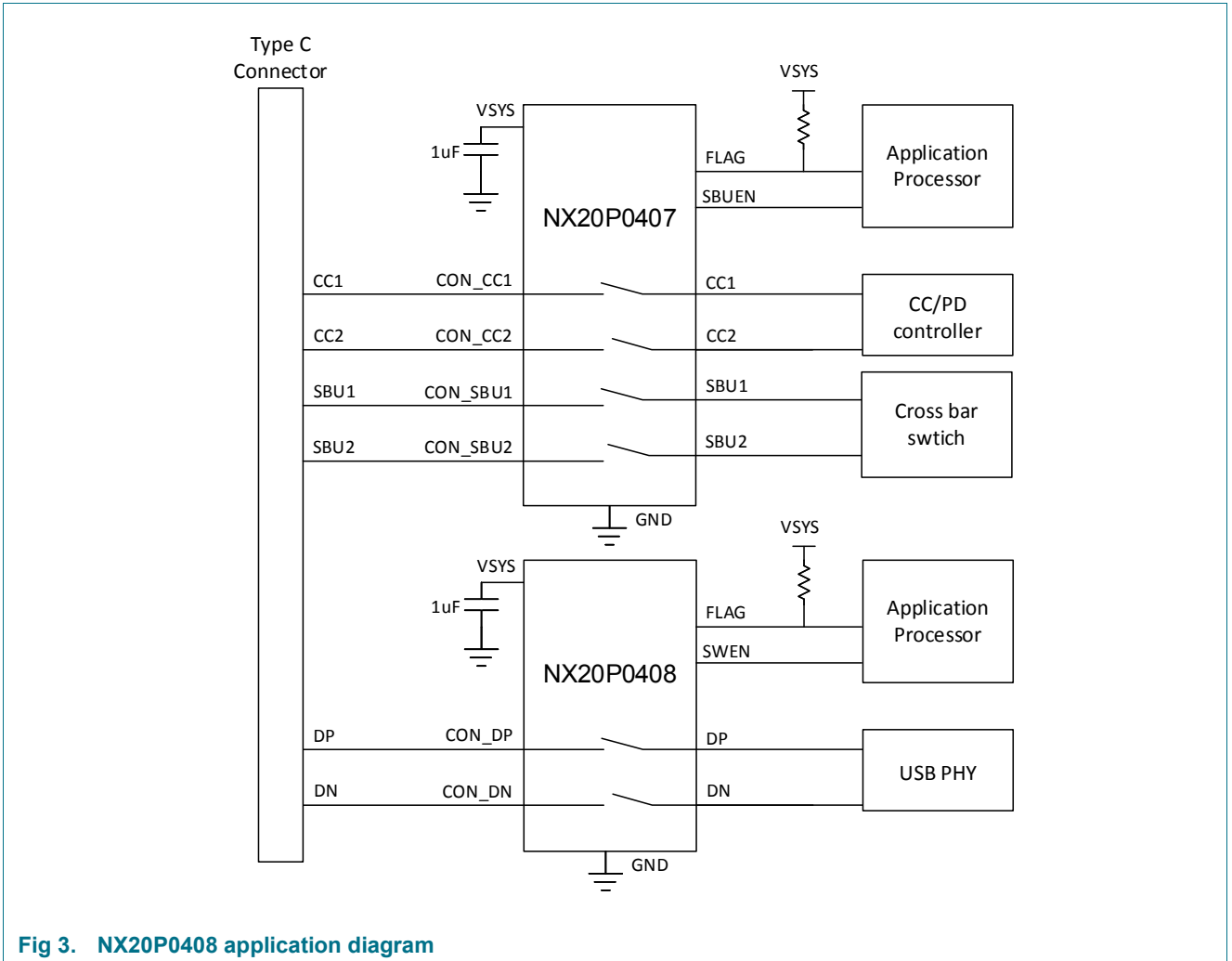

Fig 3.   NX20P0408 application diagram

8.1 Power status

When VSYS is below $V_{SYSUVLO}$, NX20P0408 stays shutdown mode, where bias, switches and all comparators are disabled.

NX20P0408 enters standby mode when VSYS exceed $V_{SYSUVLO}$. USB switch is controlled by SWEN.

Table 4.   Power state

Power state	VSYS	Flag	SWEN	USB Switch
Dead battery	< $V_{SYSUVLO}$	Hi-Z	x	OFF
Power ON_A	> $V_{SYSUVLO}$	Hi-Z	Low	OFF
Power ON_B	> $V_{SYSUVLO}$	Hi-Z	High	ON

8.2 Over voltage protection

NX20P0408 has short circuit protection of CON_DP and CON_DN up to 28V. USB switch overvoltage threshold is V_{OVP} to secure turn the switch off not to pass high voltage to USB phy in system side.

Once overvoltage on any of channels is triggered, the switch is super fast turned off within t_{OVP_res}, not to pass over the overvoltage to system side. FLAG pin goes low in t_{FLAG_RES} to inform system this fault condition. If the voltage of the channel triggered OVP come down back below overvoltage threshold for t_{OVP_Deb}, the switch is turned back on and FLAG pin get Hi-Z.

Four switches for DP and DN are each own OVP comparator and controlled by its comparator independently. If DP voltage exceed OVP threshold, the DP switch is turned off, but the other switch stays ON.
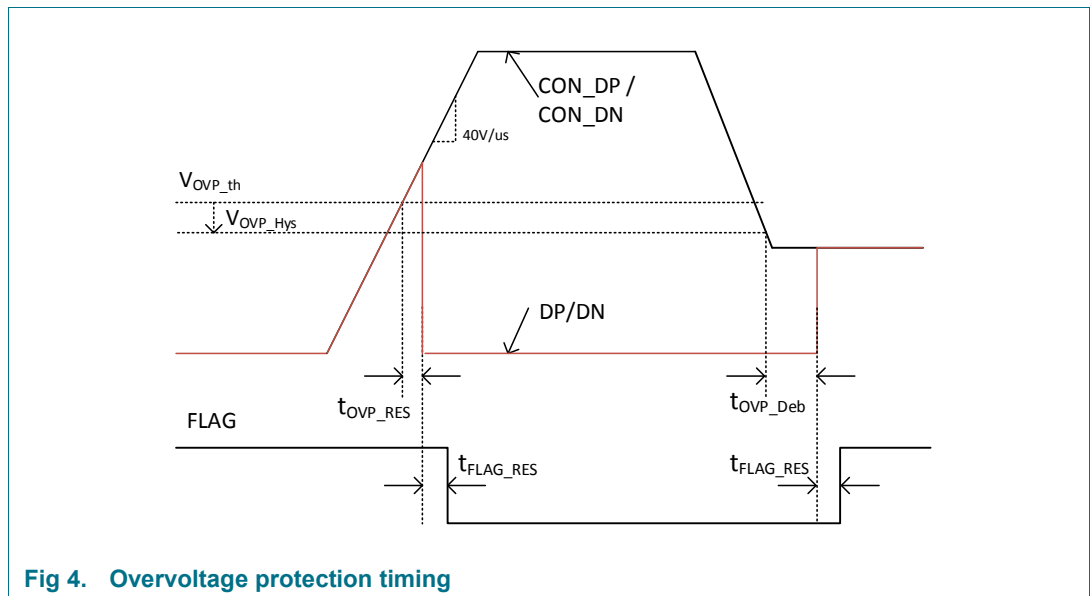

Fig 4.   Overvoltage protection timing

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8.3 Post-stage Clamp circuit

NX20P0408 has post stage clamp circuit to clamp extra voltage on DP and DN in system side. When shorting with VBUS, the voltage on CON_DP and CON_DN is rapidly increased. Even though NX20P0408 features super fast response for overvoltage condition, the over-voltage may pass through to DP/DN for the response time, 70ns. NX20P0408 post-stage clamp circuit is second protection to clamp the voltage on DP/DN in system side not to exceed Clamping voltage, 7V.

Fig 5. Post-stage clamp operation
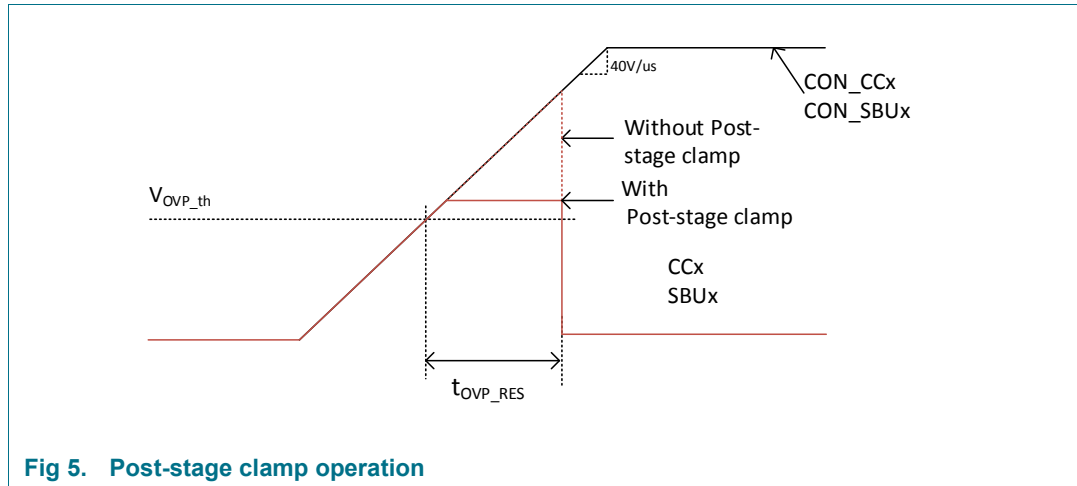
8.4 Flag

Flag pin is open drain output to indicate device fault condition to application processor. If Fault condition is detected, Flag output is latched to low until the fault condition is cleared.
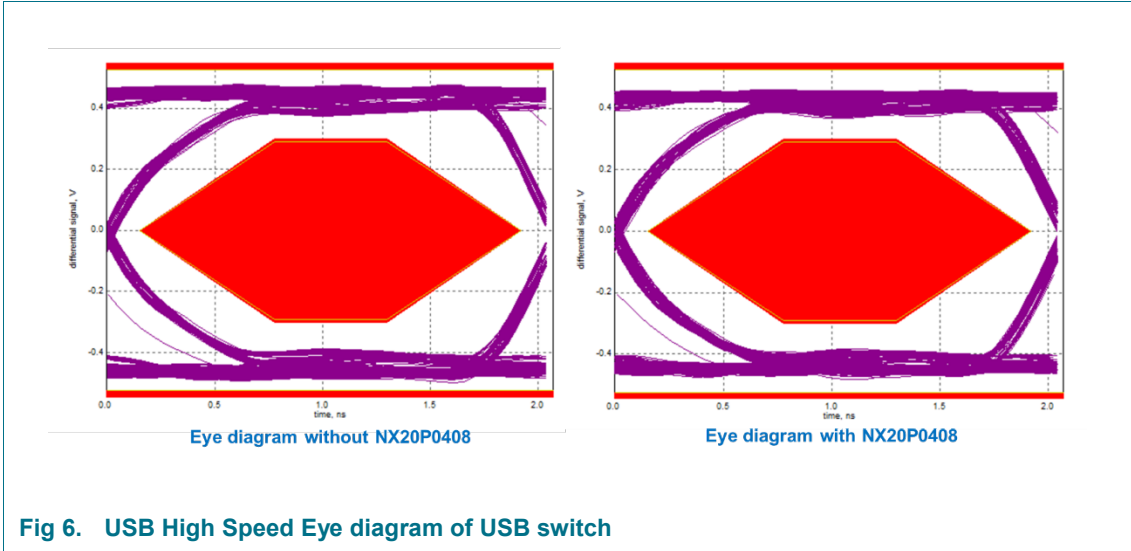
The table 5 shows NX20P0408 fault conditions and its behavior.

Table 5.   Fault conditions and behavior

Fault	Condition	SWEN	Flag	USB Switch
Thermal Warning	$T_j > T_{OTP}$	Low	Low	OFF
Thermal Warning	$T_j > T_{OTP}$	High	Low	ON
OVP	$V_{CON\_Dx} > V_{OVP}$	Low	Hi-Z	OFF
OVP	$V_{CON\_Dx} > V_{OVP}$	High	Low	OFF

8.5 Switch

NX20P0408 has a pair of switch. USB switches are controlled by SWEN when SYS power is valid. The switch bandwidth is 1.5GHz so that it can be used to protect USB D+/D- from overvoltage.

Eye diagram without NX20P0408   Eye diagram with NX20P0408

Fig 6.   USB High Speed Eye diagram of USB switch

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9.   Limiting values

Table 6.   Limiting values (Absolute Maximum Ratings)

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to GND)	CON_DP, CON_DN		-0.5	28	V
	DP, DN		-0.5	6	V
	VSYS,		-0.5	6	V
	FLAG		-0.5	6	V
Output Current	CON_DP, CON_DN, DP, DN		-100	100	mA
Junction temperature			-40	135	°C
V_{ESD} Electrostatic discharge voltage	All other pins	HBM (JESD22-001)	-2	+2	KV
		CDM (JESD22-C101E)	-500	+500	KV

10. Recommended operating conditions

Table 7.   Recommended Operating Conditions

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to GND)	VSYS		2.5	5.5	V
	SWEN		0	5.5	V
	FLAG		0	5.5	V
	DP, DN, CON_DP, CON_DN		0	4.5	V
Ambient temperature			-40	85	°C

11. Thermal characteristics

Table 8.   Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	110	°C/W

[1]   The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply.Try not to use any solder-stop varnish under the chip

[2]   This Rth(j-a) is calculated based on JEDEX2S2P board. The actual Rth(j-a) value may vary in applications using different layer stacks and layouts.

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12. Electrical Characteristics

12.1 Static Characteristics

Table 9.   Static Characteristics (-40C~85C)

At recommended input voltages and Tamb = -40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply current / Leakage current						
$V_{SYSUVLO}$	VSYS Under Voltage Lockout	Falling, 100mV hysteresis	2.14	2.27	2.40	V
I_{SYS}	Standby current	V_{SYS} = 3.6V, SWEN = 0V		32	55.5	µA
		V_{SYS} = 3.6V, SWEN = 3.6V		105	170	µA
I_{Leak}	Leakage current for DP/DN pins	V_{SYS} = 3.6V, $V_{DP/DN}$ = 3.6V, CON_DP/DN floating			1	µA
USB switcher						
R_{on}	On resistance	V_{SYS} = 3.6V, SWEN = High, DP/DN= 3.6V	-	3.6	5.4	Ω
R_{on_Flat}	On resistance flatness	Sweep DP/DN voltage between 0V and 3.6V		30	150	mΩ
V_{OVP}	OVP threshold on CON_DP/DN	V_{SYS} = 3.6V, SWEN = High, rising	4.6	4.8	5.0	V
V_{OVP_hys}	OVP threshold hysteresis			100		mV
C_{on}	Equivalent on capacitance	Capacitance between Dx /CON_Dx and GND when Powered up. $V_{DP/DN}$ = 0V to 1.2V, f = 240MHz		4.5		pF
BW	3dB Bandwidth	Single ended, 50ohm termination, $V_{DP/DN}$ = 0.1V to 1.2V		1500		MHz
XTALK	Crosstalk	Swing 1Vpp at 10MHz, measure the other channels with 50mohm termination		-84		dB
V_{CLAMP}	Clamp voltage on system side	Hot plug voltage CON_Dx = 22V. load 150nF cap and 40ohm in series to GND on DP/DN		7		V
FLAG						
V_{OL}	Output low voltage	I_{OL} = 5mA			0.3	V
I_{OH}	High level leakage current	V_{FLAG} = 5.5V			1	µA
SWEN						

Symbol	Parameter		Typ		Max	Unit
V_{IH}	Valid input high		1.5			V
V_{IL}	Valid input low				0.4	V
R_{PD}	Pull down resistor		350	450	600	kΩ
Over Temperature flag						
T_{OTP}	Over temperature Flag			125		°C
T_{OTP_hys}	Over temperature Flag hysteresis		-	10	-	°C

12.2 Dynamic Characteristics

Table 10. Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Switch Dynamic Characteristics						
t_{pwrup}	Power up time from Valid power source of VSYS			2.5	5	ms
t_{OVP_res}	OVP response time	Time from OVP trip voltage asserted to OVP FET turn-off	-	60		ns
t_{OVP_deb}	Minimum time to exit OVP shutdown, CON_DP or CON_DN		-	20		ms
t_{ON}	USB switch enable time from SWEN to high			40	80	us
t_{OTP_deb}	Minimum time to exit Over Temperature flag	Note 1	-	20		ms
t_{FLAG_RES}	Time to FLAG assertion from OVP detected.			5		us
t_{OTP_flag}	Time to Flag from over temperature	Note 1		20		us

Note 1 : Guaranteed by Design

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13. Package outline

WLCSP12; wafer level chip-scale package, 12 bumps, 1.67 x 1.27 x 0.525 mm (Backside coating included)

DIMENSIONS (mm are the original dimensions)
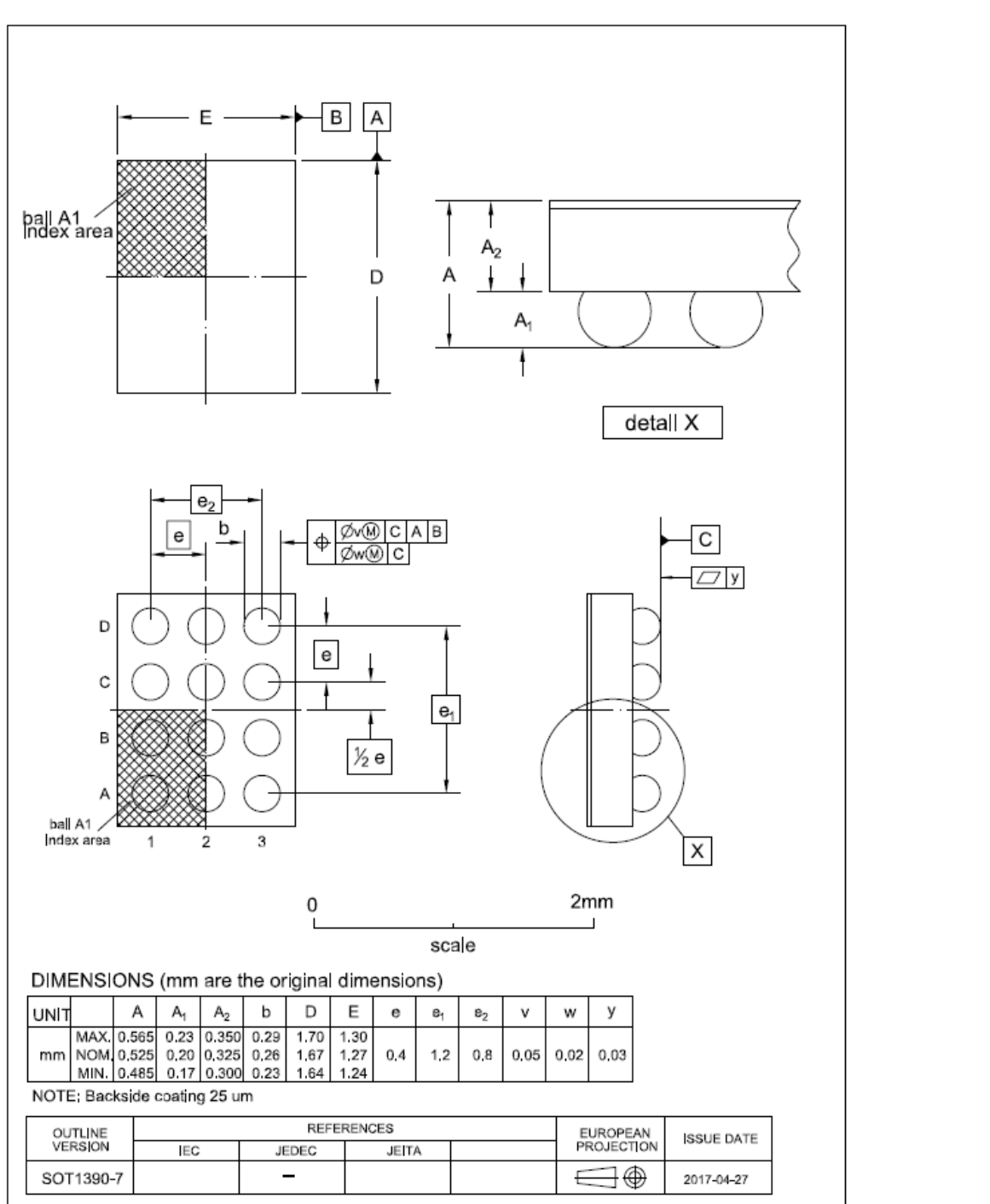
UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.565	0.23	0.350	0.29	1.70	1.30	0.4	1.2	0.8	0.05	0.02	0.03
	NOM.	0.525	0.20	0.325	0.26	1.67	1.27						
	MIN.	0.485	0.17	0.300	0.23	1.64	1.24						

NOTE: Backside coating 25 um

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1390-7		—			⊟⊕	2017-04-27

Fig 7. Package outline WLCSP12

14. Legal information

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[2] The term 'short data sheet' is explained in section "Definitions".

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16. List of figures

17. List of tables

18. Contents

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