AT45DB021E

2-Mbit DataFlash (with Extra 64 kbits)
1.65 V Minimum SPI Serial Flash Memory

Features

- Single 1.65 V - 3.6 V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports RapidS™ operation
- Continuous read capability through entire array
  - Up to 85 MHz
  - Low-power read option up to 15 MHz
  - Clock-to-output time (t_V) of 6 ns maximum
- User-configurable page size
  - 256 bytes per page
  - 264 bytes per page (default)
  - Page size can be factory pre-configured for 256 bytes
- One SRAM data buffer (256/264 bytes)
- Flexible programming options
  - Byte/Page Program (1 to 256/264 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase (256/264 bytes)
  - Block Erase (2 kB)
  - Sector Erase (32 kB)
  - Chip Erase (2 Mbits)
- Program and Erase Suspend/Resume
- Advanced hardware and software data protection features
  - Individual sector protection
  - Individual sector lockdown to make any sector permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low power dissipation
  - 200 nA Ultra-Deep Power-Down current (typical)
  - 3 µA Deep Power-Down current (typical)
  - 25 µA Standby current (typical @ 20 MHz)
  - 4.5 mA Active Read current (typical))
- Endurance: 100,000 program/erase cycles per page minimum
- Data retention: 20 years
- Complies with full industrial temperature range
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.150" wide and 0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)
  - 8-ball (6 x 4 Array) Wafer Level Chip Scale Package
  - Die in Wafer Form

Adesto™

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1 Description

The Adesto® AT45DB021E is a 1.65 V minimum, serial-interface, sequential access Flash memory. It is ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT45DB021E also supports the RapidS serial interface for applications requiring very high speed operation. Its 2,162,688 bits of memory are organized as 1,024 pages of 256 bytes or 264 bytes each. In addition to the main memory, AT45DB021E also contains one SRAM buffer of 256/264 bytes. The Buffer can be used as additional system scratch memory, and E^2PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation.

Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the Adesto DataFlash® uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, AT45DB021E does not require high input voltages for programming. The device operates from a single 1.65 V to 3.6 V power supply for the erase and program and read operations. The AT45DB021E is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2 Pin Configurations and Pinouts

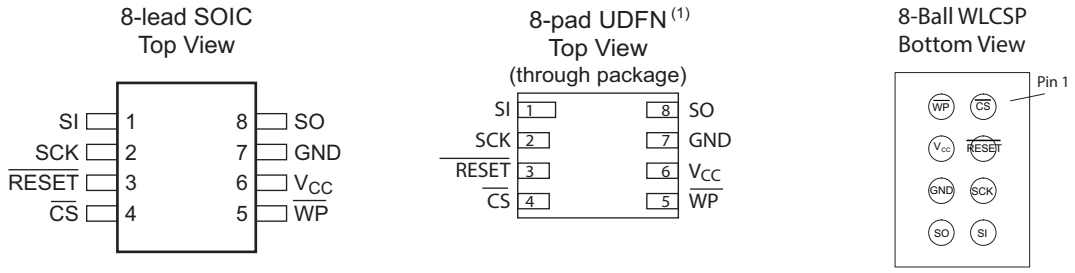


Figure 2-1. Pinouts

Note: 1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

Table 2-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device is deselected and normally placed in the standby mode (not Deep Power-Down mode) and the output pin (SO) is in a high-impedance state. When the device is deselected, data are not accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device does not enter the standby mode until the operation is done.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to, and from, the device. Command, address, and input data present on the SI pin is latched on the rising edge of SCK, while output data on the SO pin is clocked out on the falling edge of SCK.	—	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input, including command and address sequences. Data on the SI pin is latched on the rising edge of SCK. Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin are clocked out on the falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Output

Table 2-1. Pin Configurations *(continued)*

Symbol	Name and Function	Asserted State	Type
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register are protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the contents of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device ignores the command and perform no operation. The device returns to the idle state once the $\overline{CS}$ pin has been deasserted. The Enable Sector Protection command and the Sector Lockdown command are recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled-high and can be left floating if hardware-controlled protection is not used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{RESET}$	**Reset:** A low state on the reset pin ($\overline{RESET}$) terminates the operation in progress and reset the internal state machine to an idle state. The device remains in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin/feature is not used, drive the $\overline{RESET}$ pin high externally.	Low	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages can produce spurious results; do not attempt this.	—	Power
GND	**Ground:** The ground reference for the power supply. Connect GND to the system ground.	—	Ground

3 Block Diagram

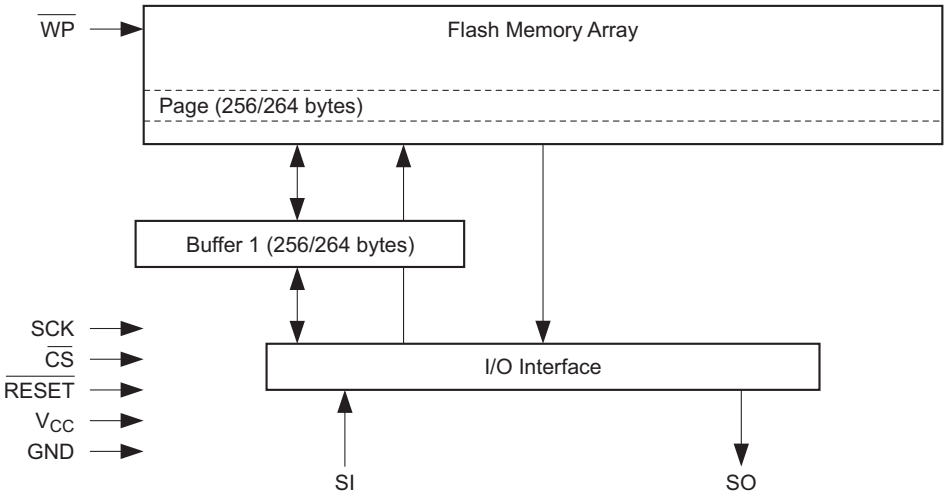


Figure 3-1. Block Diagram

4 Memory Array

To provide optimal flexibility, the AT45DB021E memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. Figure 4-1 illustrates the breakdown of each level and details the number of pages per sector and block. Program operations to the DataFlash can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip, sector, block, or page level.

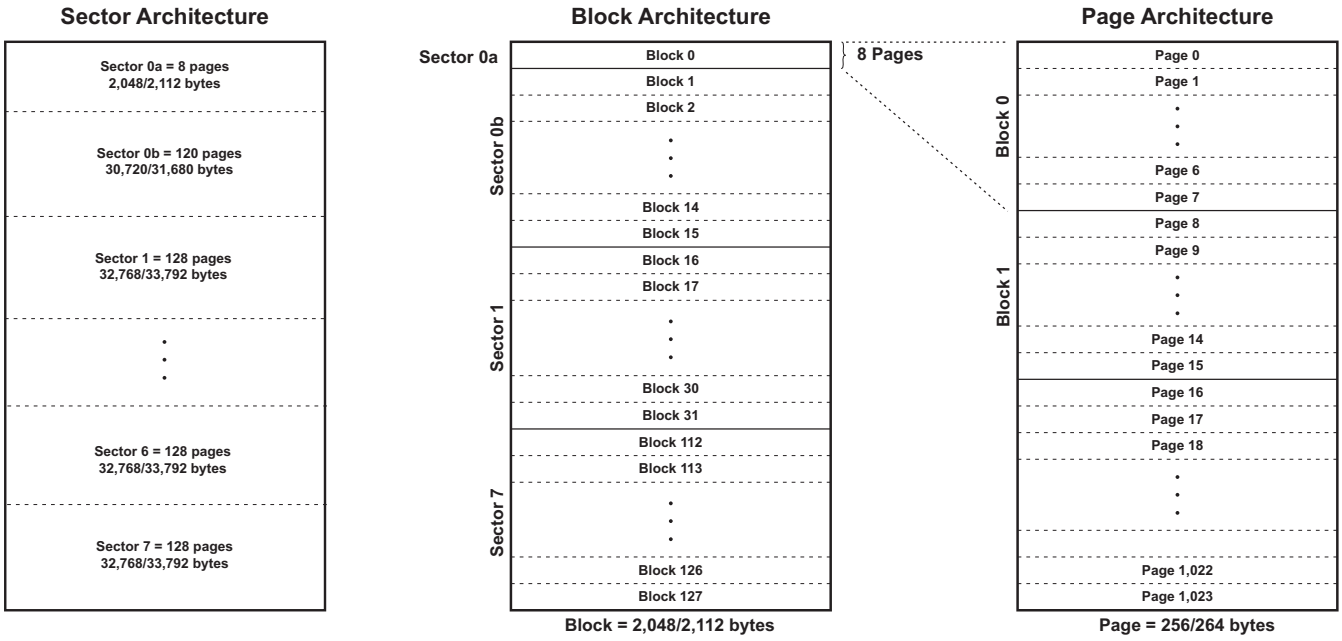


Figure 4-1. Memory Architecture Diagram

5 Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Table 16-1, on page 43, through Table 16-4, on page 44. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the Buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the Buffer or main memory address location through the SI (Serial Input) pin. All instructions, addresses, and data are transferred with the Most Significant Bit (MSB) first.

Three address bytes are used to address memory locations in either the main memory array or in the Buffer. The three address bytes are comprised of a number of dummy bits and a number of actual device address bits, with the number of dummy bits varying depending on the operation being performed and the selected device page size. Buffer addressing for the standard DataFlash page size (264 bytes) is referenced in the datasheet using the terminology BFA8 - BFA0 to denote the nine address bits required to designate a byte address within the Buffer. The main memory addressing is referenced using the terminology PA9 - PA0 and BA8 - BA0, where PA9 - PA0 denotes the 10 address bits required to designate a page address, and BA8 - BA0 denotes the nine address bits required to designate a byte address within the page. Therefore, when using the standard DataFlash page size, a total of 22 address bits are used.

For the “power of 2” binary page size (256 bytes), the Buffer addressing is referenced in the datasheet using the conventional terminology BFA7 - BFA0 to denote the eight address bits required to designate a byte address within the Buffer. Main memory addressing is referenced using the terminology A17 - A0, where A17 - A8 denotes the 10 address bits required to designate a page address, and A7 - A0 denotes the eight address bits required to designate a byte address within a page. Therefore, when using the binary page size, a total of 21 address bits are used.

6 Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from the data buffer. The DataFlash supports RapidS protocols for Mode 0 and Mode 3. See Section 26, Detailed Bit-Level Read Waveforms: RapidS Mode 0/Mode 3, on page 60 for diagrams detailing the clock cycle sequences for each mode.

6.1 Continuous Array Read (Legacy Command: E8h)

By supplying an initial starting address for the main memory array, the Continuous Array Read command can be used to sequentially read a continuous stream of data from the device by providing a clock signal; no additional addressing information or control signals is required. The DataFlash incorporates an internal address counter that automatically increments on every clock cycle, allowing one continuous read from memory to be performed without the need for additional address sequences. To perform a Continuous Array Read using the standard DataFlash page size (264-bytes), an opcode of E8h must be clocked into the device followed by three address bytes (which comprise the 19-bit page and byte address sequence) and four dummy bytes. The first 10 bits (PA9 - PA0) of the 19-bit address sequence specify which page of the main memory array to read and the last nine bits (BA8 - BA0) of the 19-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode E8h must be clocked into the device followed by three address bytes (A17 - A0) and four dummy bytes. The dummy bytes that follow the address bytes are needed to initialize the read operation. Following the dummy bytes, additional clock pulses on the SCK pin result in data being output on the SO (Serial Output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses the data buffer and leaves the contents of the Buffer unchanged.

Note: This command is not recommended for new designs.

6.2 Continuous Array Read (High Frequency Mode: 0Bh Opcode)

This command can be used to read the main memory array sequentially at the highest possible operating clock frequency up to the maximum specified by f_{CAR1}. To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 0Bh must be clocked into the device followed by three address bytes and one dummy byte. The first 10 bits (PA9 - PA0) of the 19-bit address sequence specify which page of the main memory array to read and the last nine bits (BA8 - BA0) of the 19-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 0Bh must be clocked into the device followed by three address bytes (A17 - A0) and one dummy byte. Following the dummy byte, additional clock pulses on the SCK pin result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy byte, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR1} specification. The Continuous Array Read bypasses the data buffer and leaves the contents of the Buffer unchanged.

6.3 Continuous Array Read (Low Frequency Mode: 03h Opcode)

This command can be used to read the main memory array sequentially at lower clock frequencies up to maximum specified by f_{CAR2}. Unlike the previously described read commands, this Continuous Array Read command for lower clock frequencies does not require the clocking in of dummy bytes after the address byte sequence. To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 03h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence). The first 10 bits (PA9 - PA0) of the 19-bit address sequence specify which page of the main memory array to read, and the last nine bits (BA8 - BA0) of the 19-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 03h must be clocked into the device followed by three address bytes (A17 - A0). Following the address bytes, additional clock pulses on the SCK pin result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR2} specification. The Continuous Array Read bypasses the data buffer and leaves the contents of the Buffer unchanged.

6.4 Continuous Array Read (Low Power Mode: 01h Opcode)

This command is ideal for applications that want to minimize power consumption and do not need to read the memory array at high frequencies. Like the 03h opcode, this Continuous Array Read command allows reading the main memory array sequentially without the need for dummy bytes to be clocked in after the address byte sequence. The memory can be read at clock frequencies up to maximum specified by f_{CAR3}. To perform a Continuous Array Read using the standard DataFlash page size (264 bytes), the $\overline{CS}$ pin must first be asserted, and then an opcode of 01h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence). The first 10 bits (PA9 - PA0) of the 19-bit address sequence specify which page of the main memory array to read and the last nine bits (BA8 - BA0) of the 19-bit address sequence specify the starting byte address within the page. To perform a Continuous Array Read using the binary page size (256 bytes), the opcode 01h must be clocked into the device followed by three address bytes (A17 - A0). Following the address bytes, additional clock pulses on the SCK pin result in data being output on the SO pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the f_{CAR3} specification. The Continuous Array Read bypasses the data buffer and leaves the contents of the Buffer unchanged.

6.5 Main Memory Page Read

A Main Memory Page Read allows the user to read data directly from any one of the 1,024 pages in the main memory, bypassing the data buffer and leaving the contents of the Buffer unchanged. To start a Main Memory Page Read using the standard DataFlash page size (264 bytes), the $\overline{CS}$ pin must first be asserted then an opcode of D2h must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and four dummy bytes. The first 10 bits (PA9 - PA0) of the 19-bit address sequence specify which page of the main memory array to read, and the last nine bits (BA8 - BA0) of the 19-bit address sequence specify the starting byte address within the page. To perform a Main Memory Page Read with the binary page size (256 bytes), the opcode D2h must be clocked into the device followed by three address bytes (A17 - A0) and four dummy bytes. The first 10 bits (A17 - A8) of the 18-bit address sequence specify which page of the main memory array to read, and the last eight bits (A7 - A0) of the 18-bit address sequence specify the starting byte address within that page. The dummy bytes that follow the address bytes are sent to initialize the read operation. Following the dummy bytes, the additional pulses on SCK result in data being output on the SO (Serial Output) pin.

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes, and the reading of data. Unlike the Continuous Array Read command, when the end of a page in main memory is reached, the device continues reading back at the beginning of the same page rather than the beginning of the next page.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification. The Main Memory Page Read bypasses the data buffer and leaves the contents of the Buffer unchanged.

6.6 Buffer Read

The data buffer can be accessed independently from the main memory array, and using the Buffer Read command allows data to be sequentially read directly from the Buffer. Two opcodes, D4h or D1h, can be used for the Buffer Read command. The use of each opcode depends on the maximum SCK frequency that is used to read data from the Buffer. The D4h opcode can be used at any SCK frequency up to the maximum specified by f_{CAR} while the D1h opcode can be used for lower frequency read operations up to the maximum specified by f_{CAR2}.

To perform a Buffer Read using the standard DataFlash buffer size (264 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 15 dummy bits and nine buffer address bits (BFA8 - BFA0). To perform a Buffer Read using the binary buffer size (256 bytes), the opcode must be clocked into the device followed by three address bytes comprised of 16 dummy bits and eight address bits (A7 - A0). Following the address bytes, one dummy byte must be clocked into the device to initialize the read operation if using opcode D4h. The $\overline{CS}$ must remain low during the loading of the opcode, the address bytes, the dummy byte (for opcode D4h only), and the reading of data. When the end of a buffer is reached, the device continues reading back at the beginning of the Buffer. A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO).

7 Program and Erase Commands

7.1 Buffer Write

Using the Buffer Write command allows data clocked in from the SI pin to be written directly into the data buffer.

To load data into the Buffer using the standard DataFlash buffer size (264 bytes), an opcode of 84h must be clocked into the device followed by three address bytes comprised of 15 dummy bits and nine buffer address bits (BFA8 - BFA0). The nine buffer address bits specify the first byte in the Buffer to be written.

To load data into the Buffer using the binary buffer size (256 bytes), an opcode of 84h must be clocked into the device followed by 16 dummy bits and eight address bits (A7 - A0). The eight address bits specify the first byte in the Buffer to be written.

After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device wraps around back to the beginning of the Buffer. Data continue to be loaded into the Buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

7.2 Buffer to Main Memory Page Program with Built-In Erase

The Buffer to Main Memory Page Program with Built-In Erase command allows data that is stored in the Buffer to be written into an erased or programmed page in the main memory array. It is not necessary to pre-erase the page in main memory to be written because this command automatically erases the selected page prior to the program cycle.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the standard DataFlash page size (264 bytes), an opcode of 83h must be clocked into the device followed by three address bytes comprised of five dummy bits,10 page address bits (PA9 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program with Built-In Erase using the binary page size (256 bytes), an opcode of 83h must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device first erases the selected page in main memory (the erased state is a logic 1) and then programs the data stored in the Buffer into that same page in main memory. Both erasing and programming of the page are internally self-timed and take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates intelligent erase and program algorithms that can detect when a byte location fails to erase or program properly. If an erase or programming error arises, it is indicated by the EPE bit in the Status Register.

7.3 Buffer to Main Memory Page Program without Built-In Erase

The Buffer to Main Memory Page Program without Built-In Erase command allows data that is stored in the Buffer to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors.

To perform a Buffer to Main Memory Page Program without Built-In Erase using the standard DataFlash page size (264 bytes), an opcode of 88h must be clocked into the device followed by three address bytes comprised of five dummy bits,10 page address bits (PA9 - PA0) that specify the page in the main memory to be written, and nine dummy bits.

To perform a Buffer to Main Memory Page Program using the binary page size (256 bytes), an opcode 88h must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory to be written, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device programs the data stored in the Buffer into the specified page in the main memory. The page in main memory that is being programmed *must* have been previously erased using one of the erase commands (Page Erase, Block Erase, Sector Erase, or Chip Erase). Programming the page is internally self-timed and takes place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

7.4 Main Memory Page Program through Buffer with Built-In Erase

The Main Memory Page Program through Buffer with Built-In Erase command combines the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations into a single operation to help simplify application firmware development. With the Main Memory Page Program through Buffer with Built-In Erase command, data is first clocked into the Buffer, the addressed page in memory is then automatically erased, and then the contents of the Buffer are programmed into the just-erased main memory page.

To perform a Main Memory Page Program through Buffer using the standard DataFlash page size (264 bytes), an opcode of 82h must first be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the Buffer to be written.

To perform a Main Memory Page Program through Buffer using the binary page size (256 bytes), an opcode of 82h must first be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory to be written, and eight address bits (A7 - A0) that selects the first byte in the Buffer to be written.

After all address bytes have been clocked in, the device takes data from the input pin (SI) and stores it in the Buffer. If the end of the Buffer is reached, the device wraps around back to the beginning of the Buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the device first erases the selected page in main memory (the erased state is a logic 1) and then programs the data stored in the Buffer into that main memory page. Both erasing and programming of the page are internally self-timed and take place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates intelligent erase and programming algorithms that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it is indicated by the EPE bit in the Status Register.

7.5 Main Memory Byte/Page Program through Buffer without Built-In Erase

The Main Memory Byte/Page Program through the Buffer without Built-In Erase combines both the Buffer Write and Buffer to Main Memory Program without Built-In Erase operations to allow any number of bytes (1 to 256/264 bytes) to be programmed directly into previously erased locations in the main memory array. With the Main Memory Byte/Page Program through Buffer without Built-In Erase command, data is first clocked into Buffer, and then only the bytes clocked into the Buffer are programmed into the pre-erased byte locations in main memory. Multiple bytes up to the page size can be entered with one command sequence.

To perform a Main Memory Byte/Page Program through the Buffer using the standard DataFlash page size (264 bytes), an opcode of 02h must first be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) that specify the page in the main memory to be written, and nine buffer address bits (BFA8 - BFA0) that select the first byte in the Buffer to be written. After all address bytes are clocked in, the device takes data from the input pin (SI) and stores it in the Buffer. Any number of bytes (1 to 264) can be entered. If the end of the Buffer is reached, then the device wraps around back to the beginning of the Buffer.

To perform a Main Memory Byte/Page Program through the Buffer using the binary page size (256 bytes), an opcode of 02h must first be clocked into the device followed by three address bytes comprised of six dummy bits,

10 page address bits (PA9 - PA0) that specify the page in the main memory to be written, and eight address bits (A7 - A0) that selects the first byte in the Buffer to be written. After all address bytes are clocked in, the device takes data from the input pin (SI) and stores it in the Buffer. Any number of bytes (1 to 256) can be entered. If the end of the Buffer is reached, then the device wraps around back to the beginning of the Buffer. When using the binary page size, the page and buffer address bits correspond to an 18-bit logical address (A17-A0) in the main memory.

After all data bytes have been clocked into the device, a low-to-high transition on the $\overline{CS}$ pin starts the program operation in which the device programs the data stored in the Buffer into the main memory array. Only the data bytes that were clocked into the device are programmed into the main memory.

Example: If only two data bytes were clocked into the device, then only two bytes are programmed into main memory, and the remaining bytes in the memory page remain in their previous state.

The $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data are programmed. Programming data bytes is internally self-timed and takes place in a maximum time of t_P (the program time is a multiple of the t_{BP} time depending on the number of bytes being programmed). During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

7.6 Page Erase

The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command or the Main Memory Byte/Page Program through Buffer command to be used later.

To perform a Page Erase with the standard DataFlash page size (264 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) that specify the page in the main memory to be erased, and nine dummy bits.

To perform a Page Erase with the binary page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory to be erased, and eight dummy bits.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device erases the selected page (the erased state is a logic 1). The erase operation is internally self-timed and takes place in a maximum time of t_{PE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

7.7 Block Erase

The Block Erase command can be used to erase a block of eight pages at one time. This command is useful when needing to pre-erase larger amounts of memory and is more efficient than issuing eight separate Page Erase commands.

To perform a Block Erase with the standard DataFlash page size (264 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of five dummy bits, seven page address bits (PA9 - PA3), and 12 dummy bits. The seven page address bits are used to specify which block of eight pages is to be erased.

To perform a Block Erase with the binary page size (256 bytes), an opcode of 50h must be clocked into the device followed by three address bytes comprised of six dummy bits, seven page address bits (A17 - A11), and 11 dummy bits. The seven page address bits are used to specify which block of eight pages is to be erased.

When a low-to-high transition occurs on the $\overline{CS}$ pin, the device erases the selected block of eight pages. The erase operation is internally self-timed and takes place in a maximum time of t_{BE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

Table 7-1. Block Erase Addressing

PA9/A17	PA8/A16	PA7/A15	PA6/A14	PA5/A13	PA4/A12	PA3/A11	PA2/A10	PA1/A9	PA0/A8	Block
0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	0	0	X	X	X	124
1	1	1	1	1	0	1	X	X	X	125
1	1	1	1	1	1	0	X	X	X	126
1	1	1	1	1	1	1	X	X	X	127

7.8 Sector Erase

The Sector Erase command can be used to individually erase any sector in the main memory.

The main memory array is comprised of nine sectors, and only one sector can be erased at a time. To perform an erase of Sector 0a or Sector 0b with the standard DataFlash page size (264 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of five dummy bits, seven page address bits (PA9 - PA3), and 12 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of five dummy bits, three page address bits (PA9 - PA7), and 16 dummy bits.

To perform a Sector 0a or Sector 0b erase with the binary page size (256 bytes), an opcode of 7Ch must be clocked into the device followed by three address bytes comprised of six dummy bits, seven page address bits (A17 - A11), and 11 dummy bits. To perform a Sector 1-7 erase, an opcode of 7Ch must be clocked into the device followed by six dummy bits, three page address bits (A17 - A15), and 15 dummy bits.

The page address bits are used to specify any valid address location within the sector is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the device erases the selected sector. The erase operation is internally self-timed and takes place in a maximum time of t_{SE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

Table 7-2. Sector Erase Addressing

PA9/A17	PA8/A16	PA7/A15	PA6/A14	PA5/A13	PA4/A12	PA3/A11	PA2/A10	PA1/A9	PA0/A8	Sector
0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	1	X	X	X	0b
0	0	1	X	X	X	X	X	X	X	1
● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●	● ● ●
1	0	1	X	X	X	X	X	X	X	5
1	1	0	X	X	X	X	X	X	X	6
1	1	1	X	X	X	X	X	X	X	7

7.9 Chip Erase

The Chip Erase command allows the entire main memory array to be erased at one time.

To execute the Chip Erase command, a four-byte command sequence of C7h, 94h, 80h, and 9Ah must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode are ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to start the erase process. The erase operation is internally self-timed and takes place in a time of t_{CE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The Chip Erase command does not affect sectors that are protected or locked down; the contents of those sectors remain unchanged. Only those sectors that are not protected or locked down are erased.

The $\overline{WP}$ pin can be asserted while the device is erasing, but protection is not activated until the internal erase cycle completes.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

Table 7-3. Chip Erase Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7h	94h	80h	9Ah

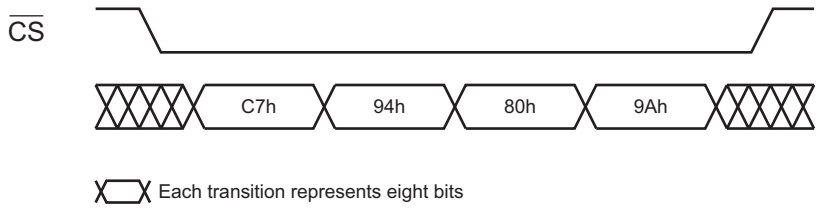


Figure 7-1. Chip Erase Timing

7.10 Read-Modify-Write

A completely self-contained read-modify-write operation can be performed to reprogram any number of sequential bytes in a page in the main memory array without affecting the rest of the bytes in the same page. This command allows the device to easily emulate an EEPROM by providing a method to modify a single byte or more in the main memory in a single operation, without the need for pre-erasing the memory or the need for any external RAM buffers. The Read-Modify-Write command is essentially a combination of the Main Memory Page to Buffer Transfer, Buffer Write, and Buffer to Main Memory Page Program with Built-in Erase commands.

To perform a Read-Modify-Write using the standard DataFlash page size (264 bytes), an opcode of 58h for Buffer 1 must be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) that specify the page in the main memory to be written and nine byte address bits (BA8-BA0) that designate the starting byte address within the page to reprogram.

To perform a Read-Modify-Write using the binary page size (256 bytes), an opcode of 58h for Buffer 1 must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory to be written and eight byte address bits (A7-A0) that designate the starting byte address within the page to reprogram.

After the address bytes have been clocked in, any number of sequential data bytes from one to 256/264 bytes can be clocked into the device. If the end of the buffer is reached when clocking in the data, then the device wraps around back to the beginning of the buffer. After all data bytes have been clocked into the device, a low-to-high transition on the CS pin starts the self-contained, internal read-modify-write operation. Only the data bytes that were clocked into the device are reprogrammed in the main memory.

Example: If only one data byte was clocked into the device, then only one byte in main memory is reprogrammed, and the remaining bytes in the main memory page remain in their previous state.

The $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data are programmed. The reprogramming of the data bytes is internally self-timed and takes place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy.

The device also incorporates an intelligent erase and programming algorithm that can detect when a byte location fails to erase or program properly. If an erase or program error arises, it is indicated by the EPE bit in the Status Register.

Note: The Read-Modify-Write command uses the same opcodes as the Auto Page Rewrite command. If no data bytes are clocked into the device, then the device performs an Auto Page Rewrite operation. See the Auto Page Rewrite command description on page 30 for more details.

8 Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{WP}$) pin. The selection of which sectors that are to be protected or unprotected against program and erase operations is specified in the nonvolatile Sector Protection Register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

8.1 Software Sector Protection

Software controlled protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin can be left floating (the $\overline{WP}$ pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

If the device is power cycled, then the software controlled protection is disabled. Once the device is powered up, the Enable Sector Protection command must be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used.

8.1.1 Enable Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and A9h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to enable the Sector Protection.

Table 8-1. Enable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3Dh	2Ah	7Fh	A9h

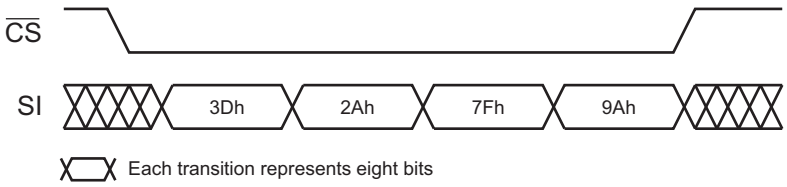


Figure 8-1. Enable Sector Protection Timing

8.1.2 Disable Sector Protection

To disable the sector protection, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and 9Ah must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to disable the sector protection.

Table 8-2. Disable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3Dh	2Ah	7Fh	9Ah

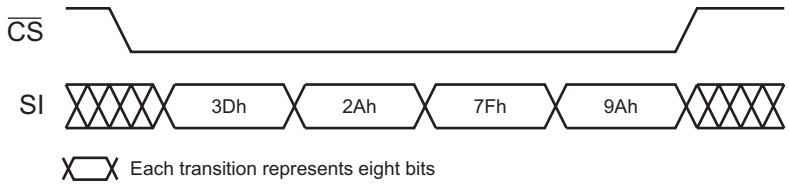


Figure 8-2. Disable Sector Protection Timing

8.2 Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or programmed as long as the $\overline{WP}$ pin is asserted. In order to modify the Sector Protection Register, the $\overline{WP}$ pin must be deasserted. If the $\overline{WP}$ pin is permanently connected to GND, then the contents of the Sector Protection Register cannot be changed. If the $\overline{WP}$ pin is deasserted or permanently connected to V_{CC}, then the contents of the Sector Protection Register can be modified.

The $\overline{WP}$ pin overrides the software controlled protection method, but only for protecting the sectors.

Example: If the sectors are not previously protected by the Enable Sector Protection command, then asserting the $\overline{WP}$ pin enables the sector protection within the maximum specified t_{WPE} time. When the $\overline{WP}$ pin is deasserted, however, the sector protection is no longer enabled (after the maximum specified t_{WPD} time) as long as the Enable Sector Protection command was not issued while the $\overline{WP}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{WP}$ pin was asserted, then deasserting the $\overline{WP}$ pin does not disable the sector protection. In this case, the Disable Sector Protection command must be issued while the $\overline{WP}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that my inadvertently assert or deassert the $\overline{WP}$ pin.

Figure 8-3 and Table 8-3 detail the sector protection status for various scenarios of the $\overline{WP}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.

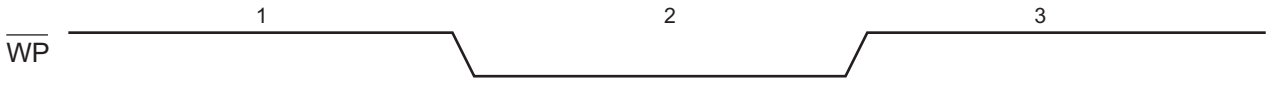


Figure 8-3. $\overline{WP}$ Pin and Protection Status Timing

Table 8-3. $\overline{WP}$ Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously	X	Disabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write
2	Low	X	X	Enabled	Read
3	High	Command Issued During Period 1 or 2	Not Issued Yet	Enabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write

8.3 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains eight bytes of data, of which byte locations 0 through 7 contain values that specify whether Sectors 0 through 7 are protected or unprotected. The Sector Protection Register is user modifiable and must be erased before it can be reprogrammed. Table 8-4 illustrates the format of the Sector Protection Register.

Table 8-4. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 7
Protected	See Table 8-5	FFh
Unprotected		00h

Note: The default values for bytes 0 through 7 are 00h when shipped from Adesto.

Table 8-5. Sector 0 (0a, 0b) Sector Protection Register Byte Value

Sector Protect/Unprotect	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-127)	N/A	N/A	
Sectors 0a and 0b Unprotected	00	00	XX	XX	0Xh
Protect Sector 0a	11	00	XX	XX	CXh
Protect Sector 0b	00	11	XX	XX	3Xh
Protect Sectors 0a and 0b	11	11	XX	XX	FXh

Note: X = Don’t care.

8.3.1 Erase Sector Protection Register

In order to modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

To erase the Sector Protection Register, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and CFh must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the Sector Protection Register takes place in a maximum time of t_{PE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the erase cycle is done, then the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with sector protection enabled or disabled. Since the erased state (FFh) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, then the erroneous program or erase command is not processed, because all sectors are protected.

Table 8-6. Erase Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3Dh	2Ah	7Fh	CFh

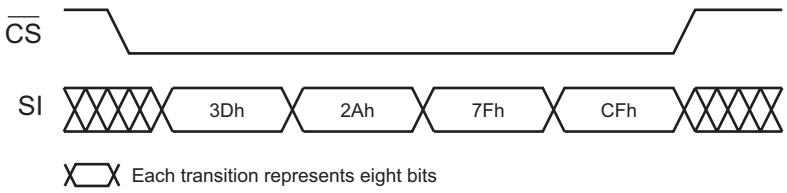


Figure 8-4. Erase Sector Protection Register Timing

8.3.2 Program Sector Protection Register

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and FCh must be clocked into the device followed by eight bytes of data corresponding to Sectors 0 through 7. After the last bit of the opcode sequence and data have been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. Programming the Sector Protection Register takes place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the erase cycle is done, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete eight bytes, then the protection status of the last six sectors cannot be guaranteed. Furthermore, if more than eight bytes of data is clocked into the device, the data wraps back around to the beginning of the register. For instance, if nine bytes of data are clocked in, then the ninth byte is stored at byte location 0 of the Sector Protection Register.

The data bytes clocked into the Sector Protection Register must be valid values (0Xh, 3Xh, CXh, and FXh for Sector 0a or Sector 0b, and 00h or FFh for other sectors) in order for the protection to function correctly. If a non-valid value is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed.

Example: If a value of 17h is clocked into byte location 2 of the Sector Protection Register, then the protection status of Sector 2 cannot be guaranteed.

The Sector Protection Register can be reprogrammed while the sector protection is enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command uses the internal buffer for processing. Therefore, the contents of the Buffer are altered from its previous state when this command is issued.

Table 8-7. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3Dh	2Ah	7Fh	FCh

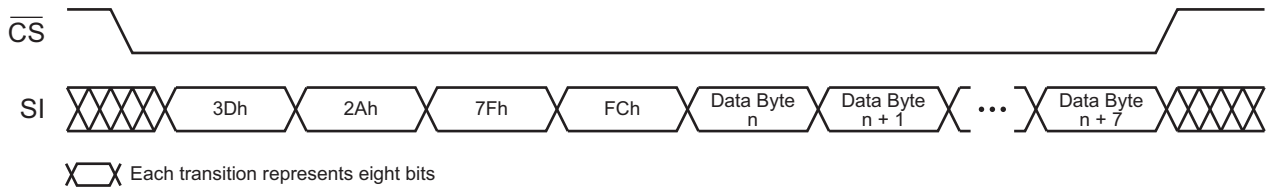


Figure 8-5. Program Sector Protection Register Timing

8.3.3 Read Sector Protection Register

To read the Sector Protection Register, an opcode of 32h and three dummy bytes must be clocked into the device. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pin result in the Sector Protection Register contents being output on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 7) corresponds to Sector 7. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses result in undefined data being output on the SO pin. The $\overline{CS}$ pin must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Table 8-8. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32h	XXh	XXh	XXh

Note: XX = Dummy byte.

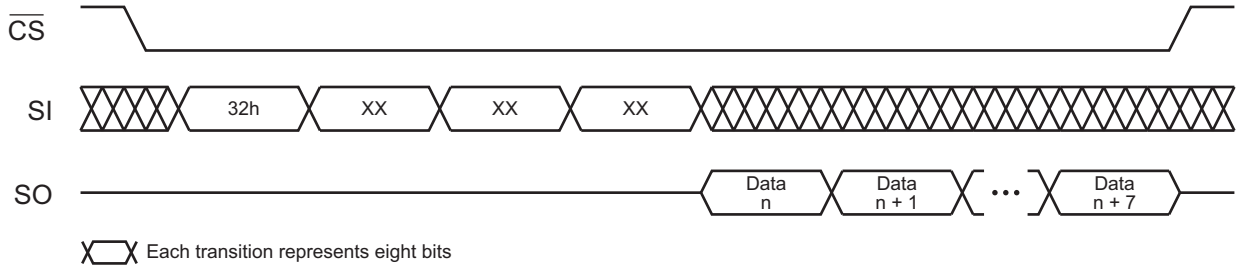


Figure 8-6. Read Sector Protection Register Timing

8.3.4 About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register is modified during the course of the application's life cycle. If the application requires that the Security Protection Register be modified more than the specified limit of 10,000 cycles because the application must temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application must limit this practice. Instead, a combination of temporarily unprotecting individual sectors, along with disabling sector protection completely, must be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

9 Security Features

9.1 Sector Lockdown

The device incorporates a sector lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read-only (ROM). This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information.

Warning: Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.

To issue the sector lockdown command, a four-byte command sequence of 3Dh, 2Ah, 7Fh, and 30h must be clocked into the device followed by three address bytes specifying any address within the sector to be locked down. After the last address bit has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed lockdown sequence. The lockdown sequence takes place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the lockdown sequence is done, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or bytes and re-issue the Sector Lockdown command if necessary.

Table 9-1. Sector Lockdown Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector Lockdown	3Dh	2Ah	7Fh	30h

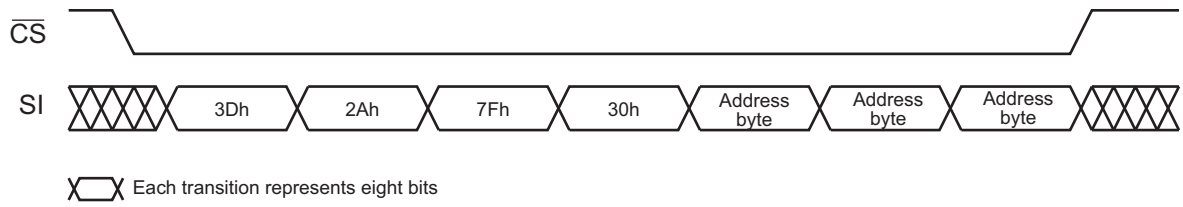


Figure 9-1. Sector Lockdown Timing

9.1.1 Read Sector Lockdown Register

The nonvolatile Sector Lockdown Register specifies which sectors in the main memory are currently unlocked or have been permanently locked down. The Sector Lockdown Register is a read-only register and contains eight bytes of data which correspond to Sectors 0 through 7. To read the Sector Lockdown Register, an opcode of 35h must be clocked into the device followed by three dummy bytes. After the last bit of the opcode and dummy bytes have been clocked in, the data for the contents of the Sector Lockdown Register are clocked out on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 7) corresponds to Sector 7. After the last byte of the Sector Lockdown Register has been read, additional pulses on the SCK pin result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin terminates the Read Sector Lockdown Register operation and put the SO pin into a high-impedance state. Table 9-2 details the format the Sector Lockdown Register.

Table 9-2. Sector Lockdown Register

Sector Number	0 (0a, 0b)	1 to 7
Locked	See Table 9-3	FFh
Unlocked		00h

Table 9-3. Sector 0 (0a and 0b) Sector Lockdown Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	
	Sector 0a (Page 0-7)	Sector 0b (Page 8-127)	N/A	N/A	Data Value
Sectors 0a and 0b Unlocked	00	00	00	00	00h
Sector 0a Locked	11	00	00	00	C0h
Sector 0b Locked	00	11	00	00	30h
Sectors 0a and 0b Locked	11	11	00	00	F0h

Table 9-4. Read Sector Lockdown Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Lockdown Register	35h	XXh	XXh	XXh

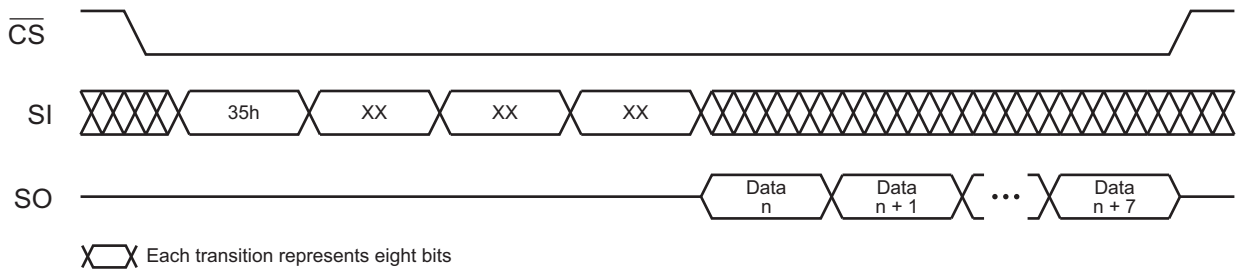


Figure 9-2. Read Sector Lockdown Register Timing

9.1.2 Freeze Sector Lockdown

The Sector Lockdown command can be permanently disabled, and the current sector lockdown state can be permanently frozen so that no additional sectors can be locked down aside from those already locked down. Any attempts to issue the Sector Lockdown command after the Sector Lockdown State has been frozen are ignored.

To issue the Freeze Sector Lockdown command, the $\overline{CS}$ pin must be asserted and the opcode sequence of 34h, 55h, AAh, and 40h must be clocked into the device. Any additional data clocked into the device are ignored. When the $\overline{CS}$ pin is deasserted, the current sector lockdown state is permanently frozen within a time of t_{LOCK}. Also, the SLE bit in the Status Register is permanently reset to a logic 0 to indicate that the Sector Lockdown command is permanently disabled.

Table 9-5. Freeze Sector Lockdown

Command	Byte 1	Byte 2	Byte 3	Byte 4
Freeze Sector Lockdown	34h	55h	AAh	40h

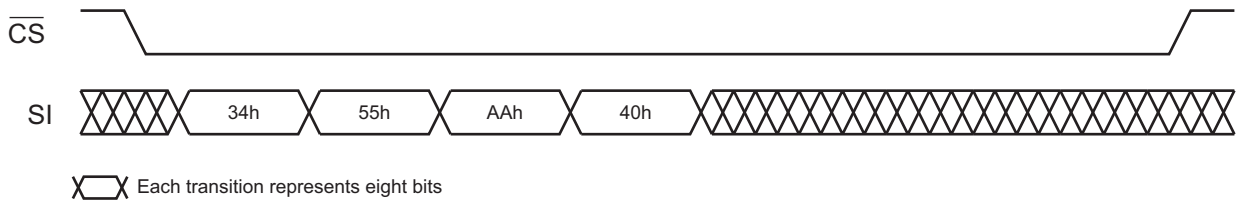


Figure 9-3. Freeze Sector Lockdown Timing

9.2 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as an One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Adesto and contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 9-6. Security Register

	Security Register Byte Number							
	0	1	· · ·	63	64	65	· · ·	127
Data Type	One-Time User Programmable				Factory Programmed by Adesto			

9.2.1 Programming the Security Register

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, a four-byte opcode sequence of 9Bh, 00h, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. Programming the Security Register takes place in a time of t_P, during which time the RDY/$\overline{BUSY}$ bit

in the Status Register indicates that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

If the full 64 bytes of data are not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, the data wraps back around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte is stored at byte location 0 of the Security Register.

Warning: **The user programmable portion of the Security Register can only be programmed one time.** Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command uses the internal buffer for processing. Therefore, the contents of the Buffer are altered from their previous state when this command is issued.

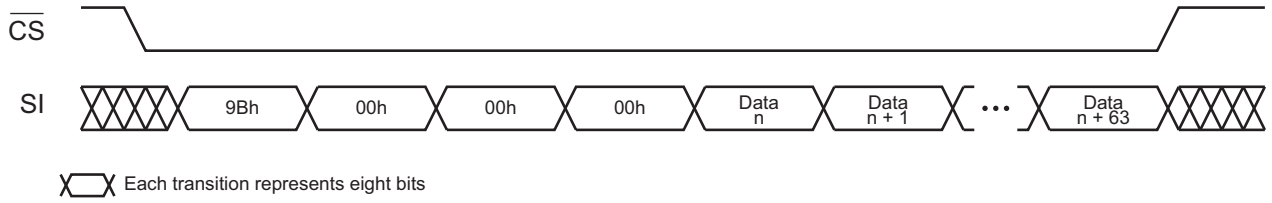


Figure 9-4. Program Security Register Timing

9.2.2 Reading the Security Register

To read the Security Register, an opcode of 77h and three dummy bytes must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin terminates the Read Security Register operation and put the SO pin into a high-impedance state.

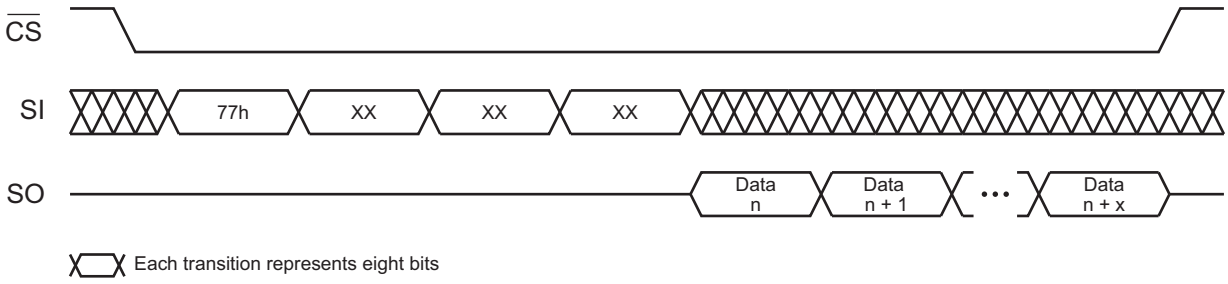


Figure 9-5. Read Security Register Timing

10 Additional Commands

10.1 Main Memory Page to Buffer Transfer

A page of data can be transferred from the main memory to the Buffer. To transfer a page of data using the standard DataFlash page size (264 bytes), an opcode of 53h must be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) which specify the page in main memory to be transferred, and nine dummy bits. To transfer a page of data using the binary page size (256 bytes), an opcode of 53h must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) which specify the page in the main memory to be transferred, and eight dummy bits.

The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the three address bytes from the input pin (SI). The transfer of the page of data from the main memory to the Buffer begins when the $\overline{CS}$ pin transitions from a low to a high state. During the page transfer time (t_{XFR}), the RDY/$\overline{BUSY}$ bit in the Status Register can be read to determine whether or not the transfer has been completed.

10.2 Main Memory Page to Buffer Compare

A page of data in main memory can be compared to the data in the Buffer as a method to ensure that data was successfully programmed after a Buffer to Main Memory Page Program command. To compare a page of data with the standard DataFlash page size (264 bytes), an opcode of 60h must be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9 - PA0) which specify the page in the main memory to be compared to the Buffer, and nine dummy bits. To compare a page of data with the binary page size (256 bytes), an opcode of 60h must be clocked into the device followed by three address bytes comprised of six dummy bits, 10 page address bits (A17 - A8) which specify the page in the main memory to be compared to the Buffer, and eight dummy bits.

The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{CS}$ pin, the data bytes in the selected Main Memory Page are compared with the data bytes in the Buffer. During the compare time (t_{COMP}), the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the part is busy. After the compare operation, bit 6 of the Status Register is updated with the result of the compare.

10.3 Auto Page Rewrite

This command must be used only if the possibility exists that static (non-changing) data are stored in one or more pages of a sector and the other pages of the same sector are erased and programmed a large number of times. Applications that modify data in a random fashion within a sector can fall into this category. To preserve data integrity of a sector, each page within a sector must be updated/rewritten at least once within every 50,000 cumulative page erase/program operations within that sector. The Auto Page Rewrite command provides a simple and efficient method to “refresh” a page in the main memory array in a single operation.

The Auto Page Rewrite command is a combination of the Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase commands. With the Auto Page Rewrite command, a page of data is first transferred from the main memory to the Buffer and then the same data is programmed back into the same page of main memory, essentially “refreshing” the contents of that page. To start the Auto Page Rewrite operation with the standard DataFlash page size (264 bytes), a one-byte opcode, 58h must be clocked into the device followed by three address bytes comprised of five dummy bits, 10 page address bits (PA9-PA0) that specify the page in main memory to be rewritten, and nine dummy bits.

To initiate an Auto Page Rewrite with the a binary page size (256 bytes), the opcode 58h must be clocked into the device followed by three address bytes consisting of six dummy bits, 10 page address bits (A17 - A8) that specify the page in the main memory that is to be rewritten, and eight dummy bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part first transfers data from the page in main memory to the Buffer and then programs the data

from the Buffer back into same page of main memory. The operation is internally self-timed and takes place in a maximum time of t_{EP}. During this time, the RDY/$\overline{BUSY}$ Status Register indicates that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, and there is no possibility of a page or pages of static data, then the programming algorithm shown in Figure 27-1, on page 64, is recommended; otherwise, if there is a chance that one or m ore pages of a sector contain static data, then the programming algorithm shown in Figure 27.2, on page 65, is recommended.

Contact Adesto for availability of devices that are specified to exceed the 50,000 cycle cumulative limit.

Note: The Auto Page Rewrite command uses the same opcodes as the Read-Modify-Write command. If data bytes are clocked into the device, the device performs a Read-Modify-Write operation. See the Read-Modify-Write command description on page 19 for more details.

10.4 Status Register Read

The two-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, Freeze Sector Lockdown status, erase/program error status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the $\overline{CS}$ pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence repeats itself, starting again with the first byte of the Status Register, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence can output new data. The RDY/$\overline{BUSY}$ status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the $\overline{CS}$ pin terminates the Status Register Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 10-1. Status Register Format – Byte 1

Bit	Name		Type (Note:)	Description	
7	RDY/$\overline{BUSY}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	COMP	Compare Result	R	0	Main memory page data matches buffer data.
				1	Main memory page data does not match buffer data.
5:2	DENSITY	Density Code	R	0101	2-Mbit
1	PROTECT	Sector Protection Status	R	0	Sector protection is disabled.
				1	Sector protection is enabled.
0	PAGE SIZE	Page Size Configuration	R	0	Device is configured for standard DataFlash page size (264 bytes).
				1	Device is configured for “power of 2” binary page size (256 bytes).

Note: R = Readable only.

Table 10-2. Status Register Format – Byte 2

Bit	Name		Type(Note:)	Description	
7	RDY/$\overline{BUSY}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	RES	Reserved for Future Use	R	0	Reserved for future use.
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	RES	Reserved for Future Use	R	0	Reserved for future use.
3	SLE	Sector Lockdown Enabled	R	0	Sector Lockdown command is disabled.
				1	Sector Lockdown command is enabled.
2	RES	Reserved for Future Use	R	0	Reserved for future use.
1	RES	Reserved for Future Use	R	0	Reserved for future use.
0	RES	Reserved for Future Use	R	0	Reserved for future use.

Note: R = Readable only.

10.4.1 RDY/$\overline{BUSY}$ Bit

The RDY/$\overline{BUSY}$ bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/$\overline{BUSY}$ bit to detect the if an internally timed operation is done, new Status Register data must be continually clocked out of the device until the state of the RDY/$\overline{BUSY}$ bit changes from a logic 0 to a logic 1 to indicate it is done.

10.4.2 COMP Bit

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using the COMP bit. If the COMP bit is a logic 1, then at least one bit of the data in the Main Memory Page does not match the data in the Buffer.

10.4.3 DENSITY Bits

The device density is indicated using the DENSITY bits. For the AT45DB021E, the four bit binary value is 0101. The decimal value of these four binary bits does not actually equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The DENSITY bits are not the same as the density code indicated in the JEDEC Device ID information. The DENSITY bits are provided only for backward compatibility to older generation DataFlash devices.

10.4.4 PROTECT Bit

The PROTECT bit provides information to the user on whether or not the sector protection has been enabled or disabled, either by the software-controlled method or the hardware-controlled method.

10.4.5 PAGE SIZE Bit

The PAGE SIZE bit indicates whether the Buffer size and the page size of the main memory array is configured for the “power of 2” binary page size (256 bytes) or the standard DataFlash page size (264 bytes).

10.4.6 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit is set to the logic 1 state. The EPE bit is not set if an erase or program operation aborts for any reason, such as an attempt to erase or program a protected region. The EPE bit is updated after every erase and program operation.

10.4.7 SLE Bit

The SLE bit indicates whether or not the Sector Lockdown command is enabled or disabled. If the SLE bit is a logic 1, then the Sector Lockdown command is still enabled and sectors can be locked down. If the SLE bit is a logic 0, then the Sector Lockdown command has been disabled and no further sectors can be locked down.

11 Deep Power-Down

During normal operation, the device is placed in the standby mode to consume less power as long as the $\overline{CS}$ pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, all commands, including the Status Register Read command, are ignored with the exception of the Resume from Deep Power-Down command. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is done by asserting the $\overline{CS}$ pin, clocking in the opcode B9h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode are ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Deep Power-Down mode within the maximum time of t_{EDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device aborts the operation and returns to the standby mode once the $\overline{CS}$ pin is deasserted. Also, the device defaults to the standby mode after a power cycle.

The Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

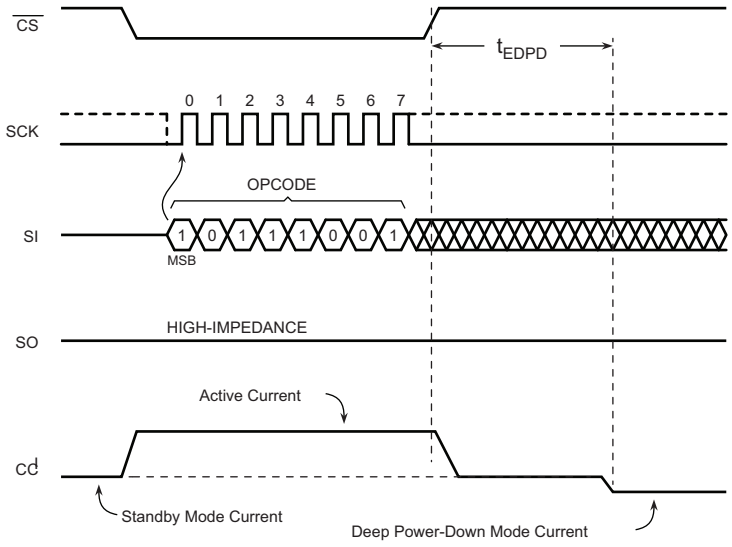


Figure 11-1. Deep Power-Down Timing

11.1 Resume from Deep Power-Down

In order to exit the Deep Power-Down mode and resume normal device operation, the Resume from Deep Power-Down command must be issued. The Resume from Deep Power-Down command is the only command that the device recognizes while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the $\overline{CS}$ pin must first be asserted and then the opcode ABh must be clocked into the device. Any additional data clocked into the device after the opcode are ignored. When the $\overline{CS}$ pin is deasserted, the device exits the Deep Power-Down mode and returns to the standby mode within the maximum time of t_{RDPD}. After the device has returned to the standby mode, normal command operations such as Continuous Array Read can be resumed.

If the complete opcode is not clocked in before the $\overline{CS}$ pin is deasserted, then the device aborts the operation and returns to the Deep Power-Down mode.

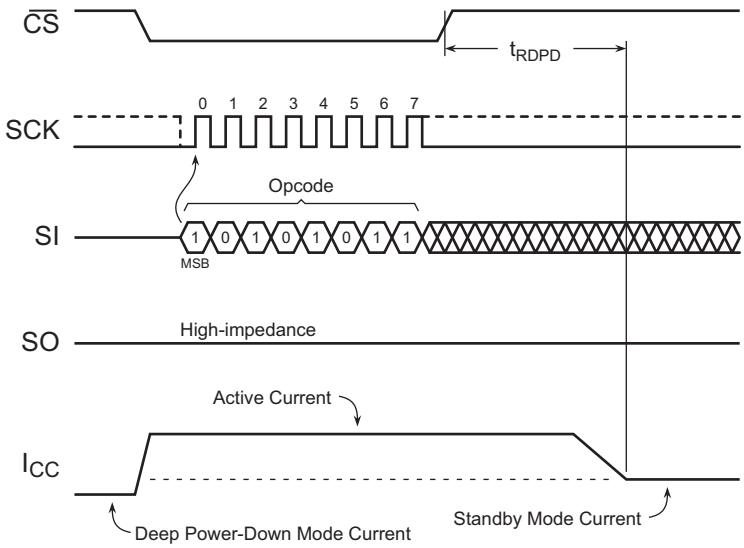


Figure 11-2. Resume from Deep Power-Down Timing

11.2 Ultra-Deep Power-Down

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry. Since almost all active circuitry is shut down in this mode to conserve power, the contents of the Buffer cannot be maintained. Therefore, any data stored in the Buffer are lost once the device enters the Ultra-Deep Power-Down mode.

When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands are ignored. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is done by asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode are ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Ultra-Deep Power-Down mode within the maximum time of t_{EUDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device aborts the operation and returns to the standby mode once the $\overline{CS}$ pin is deasserted. Also, the device defaults to the standby mode after a power cycle.

The Ultra-Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

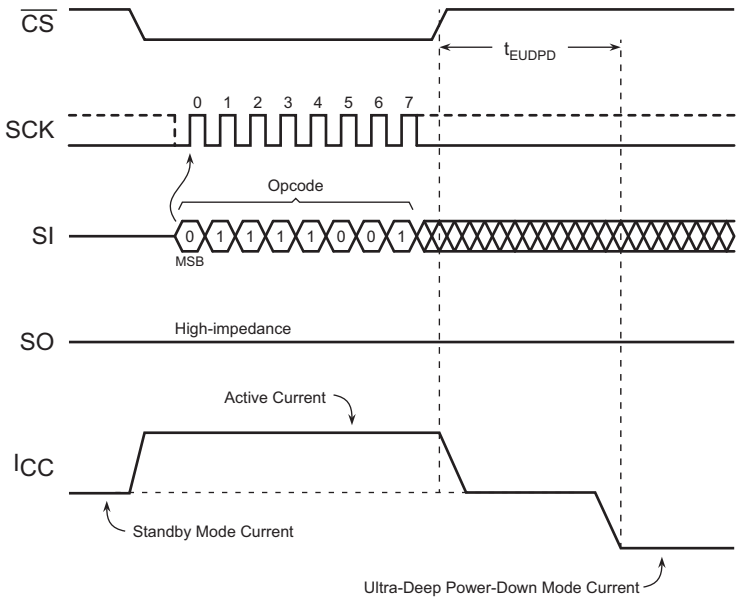


Figure 11-3. Ultra-Deep Power-Down Timing

11.3 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the $\overline{CS}$ pin must be pulsed by asserting the $\overline{CS}$ pin, waiting the minimum necessary t_{CSLU} time, and then deasserting the $\overline{CS}$ pin again. To facilitate simple software development, a dummy byte opcode can also be entered while the $\overline{CS}$ pin is being pulsed; the dummy byte opcode is ignored by the device in this case. After the $\overline{CS}$ pin has been deasserted, the device exits from the Ultra-Deep Power-Down mode and returns to the standby mode within a maximum time of t_{XUDPD}. If the $\overline{CS}$ pin is reasserted before the t_{XUDPD} time has elapsed in an attempt to start a new operation, then that operation is ignored and nothing is performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

Since the contents of the Buffer cannot be maintained while in the Ultra-Deep Power-Down mode, the Buffer contains undefined data when the device returns to the standby mode.

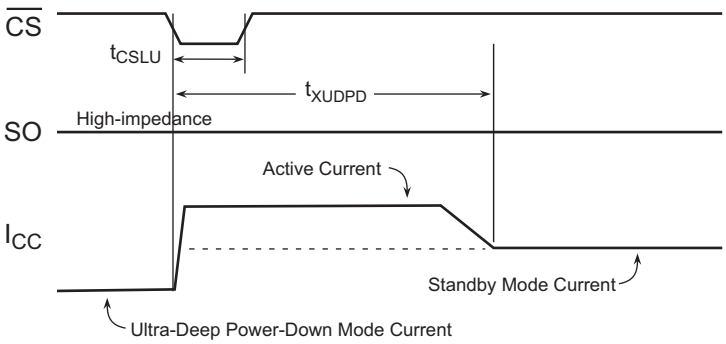


Figure 11-4. Exit Ultra-Deep Power-Down Timing

12 Buffer and Page Size Configuration

The memory array of DataFlash devices is actually larger than other Serial Flash devices in that extra user-accessible bytes are provided in each page of the memory array. For the AT45DB021E, there are an extra eight bytes of memory in each page for a total of an extra 8 kbytes (64 kbits) of user-accessible memory.

Some designers, however, might not want to take advantage of this extra memory and instead architect their software to operate on a “power of 2” binary, logical addressing scheme. To allow this, the DataFlash can be configured so that the Buffer and page sizes are 256 bytes instead of the standard 264 bytes. Also, the configuration of the Buffer and page sizes is reversible and can be changed from 264 bytes to 256 bytes or from 256 bytes to 264 bytes. The configured setting is stored in an internal nonvolatile register so that the Buffer and page size configuration is not affected by power cycles. The nonvolatile register has a limit of 10,000 erase/program cycles; therefore, be careful not to switch between the size options more than 10,000 times.

Devices are initially shipped from Adesto with the Buffer and page sizes set to 264 bytes. Devices can be ordered from Adesto pre-configured for the “power of 2” binary size of 256 bytes. For details, see Section 28, Ordering Information, on page 66.

To configure the device for “power of 2” binary page size (256 bytes), a four-byte opcode sequence of 3Dh, 2Ah, 80h, and A6h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. Programming nonvolatile register takes place in a time of t_{EP}, during which time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the configuration process and register program cycle in order for the Buffer and page size to be configured to 256 bytes.

To configure the device for standard DataFlash page size (264 bytes), a four-byte opcode sequence of 3Dh, 2Ah, 80h, and A7h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initialize the internally self-timed configuration process and nonvolatile register program cycle. Programming nonvolatile register takes place in a time of t_{EP}, during which time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the configuration process and register program cycle in order for the Buffer and page size to be configured to 264 bytes.

Table 12-1. Buffer and Page Size Configuration Commands

Command	Byte 1	Byte 2	Byte 3	Byte 4
“Power of 2” binary page size (256 bytes)	3Dh	2Ah	80h	A6h
DataFlash page size (264 bytes)	3Dh	2Ah	80h	A7h

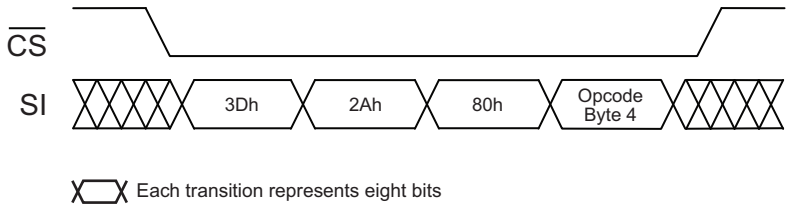


Figure 12-1. Buffer and Page Size Configuration Timing

13 Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC Standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information.

The Read Manufacturer and Device ID command is limited to a maximum clock frequency of f_{CLK}. Since not all Flash devices are capable of operating at very high clock frequencies, design applications to read the identification information from the devices at a reasonably low clock frequency; this ensures that all devices to be used in the application can be identified properly. Once the identification process is complete, the application can then increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the $\overline{CS}$ pin must first be asserted, and then the opcode 9Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output is the Manufacturer ID, followed by two bytes of the Device ID information. The fourth byte output is the Extended Device Information (EDI) String Length, which is 01h, indicating that one byte of EDI data follows. After the one byte of EDI data is output, the SO pin goes into a high-impedance state; therefore, additional clock cycles have no affect on the SO pin and no data are output. As indicated in the JEDEC Standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin terminates the Manufacturer and Device ID Read operation and puts the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 13-1. Manufacturer and Device ID Information

Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Byte 1)	23h
3	Device ID (Byte 2)	00h
4	Extended Device Information (EDI) String Length	01h
5	[Optional to Read] EDI Byte 1	00h

Table 13-2. Manufacturer and Device ID Details

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC code: 0001 1111 (1Fh for Adesto)
	0	0	0	1	1	1	1	1		
Device ID (Byte 1)	Family Code			Density Code					23h	Family code: 001 (AT45Dxxx Family) Density code: 00011 (2-Mbit)
	0	0	1	0	0	0	1	1		
Device ID (Byte 2)	Sub Code			Product Variant					00h	Sub code: 000 (Standard Series) Product variant:00000
	0	0	0	0	0	0	0	0		

Table 13-3. EDI Data

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
5	RFU			Device Revision					00h	RFU: Reserved for Future Use Device revision:00000 (Initial Version)
	0	0	0	0	0	0	0	0		

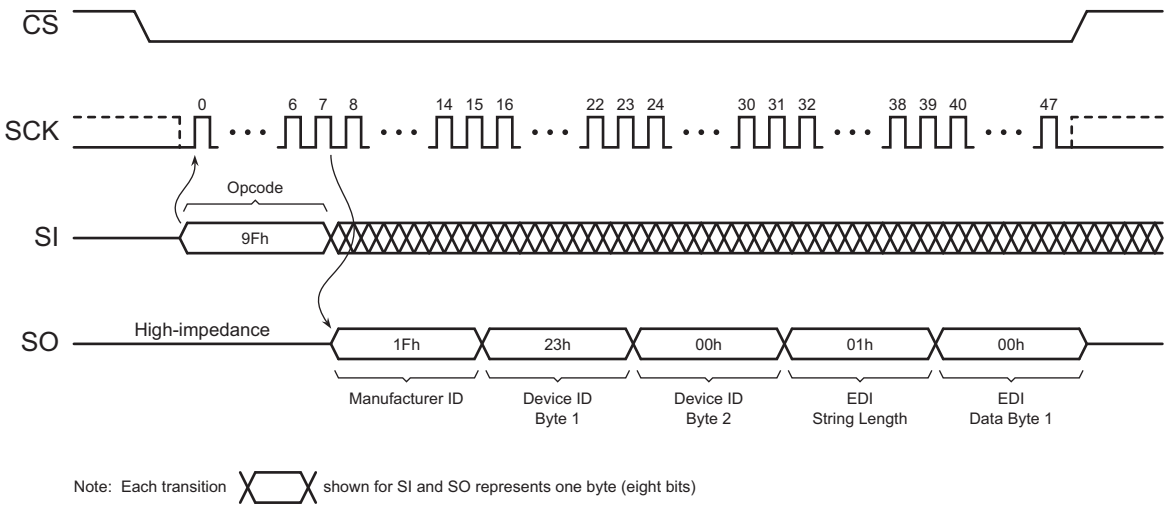


Figure 13-1. Read Manufacturer and Device ID Timing

14 Software Reset

In some applications, it might be necessary to prematurely terminate a program or erase cycle early rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Software Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state.

To perform a Software Reset, the $\overline{CS}$ pin must be asserted and a four-byte command sequence of F0h, 00h, 00h, and 00h must be clocked into the device. Any additional data clocked into the device after the last byte are ignored. When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress is terminated within a time t_{SWRST}. Since the program or erase operation might not complete before the device is reset, the contents of the page being programmed or erased cannot be guaranteed to be valid.

The Software Reset command has no effect on the states of the Sector Protection Register, the Sector Lockdown Register, or the Buffer and page size configuration.

The complete four-byte opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted; otherwise, no reset operation is performed.

Table 14-1. Software Reset

Command	Byte 1	Byte 2	Byte 3	Byte 4
Software Reset	F0h	00h	00h	00h

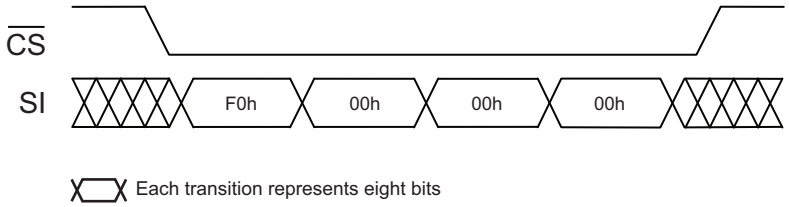


Figure 14-1. Software Reset Timing

15 Operation Mode Summary

The commands described previously can be grouped into four different categories to better describe which commands can be executed at what times.

Group A commands consist of:

1. Main Memory Page Read
2. Continuous Array Read (SPI)
3. Read Sector Protection Register
4. Read Sector Lockdown Register
5. Read Security Register
6. Buffer Read

Group B commands consist of:

1. Page Erase
2. Block Erase
3. Sector Erase
4. Chip Erase
5. Main Memory Page to the Buffer Transfer
6. Main Memory Page to the Buffer Compare
7. Buffer to Main Memory Page Program with Built-In Erase
8. Buffer to Main Memory Page Program without Built-In Erase
9. Main Memory Page Program through the Buffer with Built-In Erase
10. Main Memory Byte/Page Program through Buffer without Built-In Erase
11. Auto Page Rewrite
12. Read-Modify-Write

Group C commands consist of:

1. Buffer Write
2. Status Register Read
3. Manufacturer and Device ID Read

Group D commands consist of:

1. Erase Sector Protection Register
2. Program Sector Protection Register
3. Sector Lockdown
4. Program Security Register
5. Buffer and Page Size Configuration
6. Freeze Sector Lockdown

If a Group A command is in progress (not fully completed), do not start another command in Group A, B, C, or D. However, during the internally self-timed portion of Group B commands, any command in Group C can be executed. The Group B commands using the Buffer use Group C commands. Finally, during the internally self-timed portion of a Group D command, execute only the Status Register Read command.

16 Command Tables

Table 16-1. Read Commands

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Buffer Read (Low Frequency)	D1h
Buffer Read (High Frequency)	D4h

Table 16-2. Program and Erase Commands

Command	Opcode
Buffer Write	84h
Buffer to Main Memory Page Program with Built-In Erase	83h
Buffer to Main Memory Page Program without Built-In Erase	88h
Main Memory Page Program through Buffer with Built-In Erase	82h
Main Memory Byte/Page Program through Buffer without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah
Read-Modify-Write through Buffer 1	58h

Table 16-3. Protection and Security Commands

Command	Opcode
Enable Sector Protection	3Dh + 2Ah + 7Fh + A9h
Disable Sector Protection	3Dh + 2Ah + 7Fh + 9Ah
Erase Sector Protection Register	3Dh + 2Ah + 7Fh + CFh
Program Sector Protection Register	3Dh + 2Ah + 7Fh + FCh
Read Sector Protection Register	32h
Sector Lockdown	3Dh + 2Ah + 7Fh + 30h
Read Sector Lockdown Register	35h
Freeze Sector Lockdown	34h + 55h + AAh + 40h
Program Security Register	9Bh + 00h + 00h + 00h
Read Security Register	77h

Table 16-4. Additional Commands

Command	Opcode
Main Memory Page to Buffer Transfer	53h
Main Memory Page to Buffer Compare	60h
Auto Page Rewrite	58h
Deep Power-Down	B9h
Resume from Deep Power-Down	ABh
Ultra-Deep Power-Down	79h
Status Register Read	D7h
Manufacturer and Device ID Read	9Fh
Configure “Power of 2” (Binary) Page Size	3Dh + 2Ah + 80h + A6h
Configure Standard DataFlash Page Size	3Dh + 2Ah + 80h + A7h
Software Reset	F0h + 00h + 00h + 00h

Table 16-5. Legacy Commands [1]

Command	Opcode
Buffer Read	54H
Main Memory Page Read	52H
Continuous Array Read	68H
Status Register Read	57H

1. Legacy commands are not recommended for new designs.

Table 16-6. Detailed Bit-level Addressing Sequence for Binary Page Size (256 bytes), (X = dummy bit)

Page Size = 256-bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode Hex	Opcode Binary								Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
01h	0	0	0	0	0	0	0	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
02h	0	0	0	0	0	0	1	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
03h	0	0	0	0	0	0	1	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
0Bh	0	0	0	0	1	0	1	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1
1Bh	0	0	0	1	1	0	1	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	2
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
58h [1]	0	1	0	1	1	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
58h [2]	0	1	0	1	1	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
60h	0	1	1	0	0	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	X	X	X	X	X	X	A	A	A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
83h	1	0	0	0	0	0	1	1	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
D2h	1	1	0	1	0	0	1	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A
E8h	1	1	1	0	1	0	0	0	X	X	X	X	X	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4

1. Shown to indicate when Auto Page Rewrite Operation is executed.
2. Shown to indicate when Read Modify Write Operation is executed.

Table 16-7. Detailed Bit-level Addressing Sequence for Standard DataFlash Page Size (264 bytes)

Page Size = 264-bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode Hex	Opcode Binary								Reserved	Reserved	Reserved	Reserved	Reserved	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
01h	0	0	0	0	0	0	0	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
02h	0	0	0	0	0	0	1	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
03h	0	0	0	0	0	0	1	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
0Bh	0	0	0	0	1	0	1	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	1
1Bh	0	0	0	1	1	0	1	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	2
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
58h [1]	0	1	0	1	1	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
58h [2]	0	1	0	1	1	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
60h	0	1	1	0	0	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	X	X	X	X	X	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
83h	1	0	0	0	0	0	1	1	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A
88h	1	0	0	0	1	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A
D2h	1	1	0	1	0	0	1	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	4
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A
E8h	1	1	1	0	1	0	0	0	X	X	X	X	X	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	4

1. Shown to indicate when Auto Page Rewrite Operation is executed.
2. Shown to indicate when Read Modify Write Operation is executed.

Note: P = Page Address bit; B = Byte/Buffer Address bit; X = Dummy bit.

17 Power-On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the output pin (SO) is in a high impedance state, and a high-to-low transition on the CSB pin is required to start a valid instruction. The SPI mode (Mode 3 or Mode 0) is automatically selected on every falling edge of CSB by sampling the inactive clock state.

17.1 Power-Up/Power-Down Voltage and Timing Requirements

As the device initializes, there is a transient current demand. The system must be capable of providing this current to ensure correct initialization. During power-up, the device must not be READ for at least the minimum t_{VCSL} time after the supply voltage reaches the minimum V_{POR} level (V_{POR} min). While the device is being powered-up, the internal Power-On Reset (POR) circuitry keeps the device in a reset mode until the supply voltage rises above the minimum V_{cc}. During this time, all operations are disabled, and the device does not respond to any commands.

If the first operation to the device after power-up is a program or erase operation, then the operation cannot be started until the supply voltage reaches the minimum V_{CC} level and an internal device delay has elapsed. This delay is a maximum time of t_{PUW}. After the t_{PUW} time, the device is in the standby mode if CSB is at logic high or active mode if CSB is at logic low. For the case of Power-down then Power-up operation, or if a power interruption occurs (such that V_{CC} drops below V_{POR} max), the V_{cc} of the Flash device must be maintained below V_{PWD} for at least the minimum specified T_{PWD} time. This is to ensure the Flash device resets properly after a power interruption.

Table 17-1. Voltage and Timing Requirements for Power-Up/Power-Down

Symbol	Parameter	Min	Max	Units
V_{PWD} [1]	V_{CC} for device initialization		1.0	V
$t_{PWD(1)}$	Minimum duration for device initialization	300		µs
t_{VCSL}	Minimum V_{CC} to chip select low time for Read command	70		µs
$t_{VR(1)}$	V_{CC} rise time	1	500000	µs/V
V_{POR}	Power on reset voltage	1.45	1.6	V
t_{PUW}	Power up delay time before Program or Erase is allowed		3	ms

Not 100% tested (value guaranteed by design and characterization).

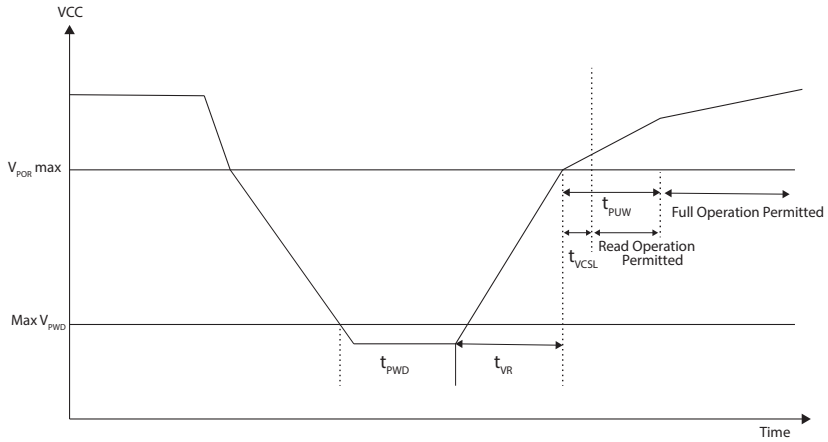


Figure 17-1. Power-Up Timing

18 System Considerations

The serial interface is controlled by the Serial Clock (SCK), Serial Input (SI), and Chip Select ($\overline{CS}$) pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. PCB traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash devices occurs during programming and erasing operations. The supply voltage regulator must be able to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erasing can lead to improper operation and possible data corruption.

19 Electrical Specifications

19.1 Absolute Maximum Ratings

Temperature under Bias . . . . . -55°C to +125°C

Storage Temperature. . . . . -65°C to +150°C

All Input Voltages
(except V_{CC} but including NC pins)
with Respect to Ground. . . . . -0.6 V to +6.25 V

All Output Voltages
with Respect to Ground. . . . . -0.6 V to V_{CC} + 0.6 V

Notice: Stresses beyond those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

19.2 DC and AC Operating Range

Parameter		AT45DB021E
Operating Temperature (Case)	Industrial	-40°C to 85°C
V_{CC} Power Supply		1.65 V to 3.6 V

19.3 DC Characteristics

Table 19-1. DC Parameter Values

Symbol	Parameter	Condition[3]	1.65 V to 3.6 V			2.3 V to 3.6 V			Units
			Min	Typ	Max	Min	Typ	Max	
I_{UDPD}	Ultra-Deep Power-Down Current	$\overline{CS}$= V_{CC}. All other inputs at 0V or V_{CC}		0.2	1		0.35	1	µA
I_{DPD}	Deep Power-Down Current	$\overline{CS}$= V_{CC}. All other inputs at 0V or V_{CC}		4.5	12		5	12	µA
I_{SB}	Standby Current	$\overline{CS}$= V_{CC}. All other inputs at 0V or V_{CC}		25	40		25	40	µA
I_{CC1}[1][2]	Active Current, Low Power Read (01h) Operation	f = 1 MHz; I_{OUT} = 0mA		6	9		6	9	mA
		f = 15 MHz; I_{OUT} = 0mA		7	10		7	10	mA
I_{CC2}[1][2]	Active Current, Read Operation	f = 50 MHz; I_{OUT} = 0mA		10	12		10	12	mA
		f = 85 MHz; I_{OUT} = 0mA		12	15		12	15	mA
I_{CC3}[1][2]	Active Current, Program Operation	$\overline{CS}$ = V_{CC}		10	12		10	12	mA
I_{CC4}[1][2]	Active Current, Erase Operation	$\overline{CS}$ = V_{CC}		8	12		8	12	mA
I_{LI}	Input Load Current	All inputs at CMOS levels			1			1	µA
I_{LO}	Output Leakage Current	All inputs at CMOS levels			1			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.2			V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.8			V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.2			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2 V			V_{CC} - 0.2 V			V

Notes: 1. Typical values measured at 1.8 V @ 25°C for the 1.65 V to 3.6 V range.
2. Typical values measured at 3.0 V @ 25°C for the 2.3 V to 3.6 V range.
All inputs (SI, SCK, $\overline{CS}$, $\overline{WP}$, and $\overline{RESET}$) are guaranteed by design to be 5 V tolerant.

19.4 AC Characteristics

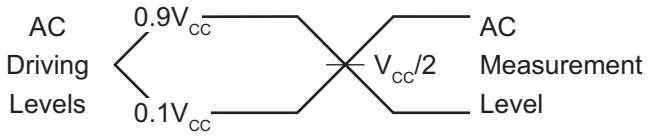
Symbol	Parameter	1.65 V to 3.6 V			2.3 V to 3.6 V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			70			70	MHz
f_{CAR1}	SCK Frequency for Continuous Read			70			85	MHz
f_{CAR2}	SCK Frequency for Continuous Read (Low Frequency)			33			33	MHz
f_{CAR3}	SCK Frequency for Continuous Read (Low Power Mode – 01h Opcode)			15			15	MHz
t_{WH}	SCK High Time	4			4			ns
t_{WL}	SCK Low Time	4			4			ns
t_{SCKR}(1)	SCK Rise Time, Peak-to-peak	0.1			0.1			V/ns
t_{SCKF}(1)	SCK Fall Time, Peak-to-peak	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	20			20			ns
t_{CSS}	$\overline{CS}$ Setup Time	6			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			5			ns
t_{SU}	Data In Setup Time	2			2			ns
t_{H}	Data In Hold Time	1			1			ns
t_{HO}	Output Hold Time	0			0			ns
t_{DIS}(1)	Output Disable Time			8			6	ns
t_{V}	Output Valid			7			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1			1	µs
t_{LOCK}	Freeze Sector Lockdown Time (from $\overline{CS}$ High)			200			200	µs
t_{EUDPD}(1)	$\overline{CS}$ High to Ultra-Deep Power-Down			3			3	µs
t_{CSLU}	Minimum $\overline{CS}$ Low Time to Exit Ultra-Deep Power-Down	20			20			ns
t_{XUDPD}	Exit Ultra-Deep Power-Down Time			240			120	µs
t_{EDPD}(1)	$\overline{CS}$ High to Deep Power-Down			2			2	µs
t_{RDPD}	Resume from Deep Power-Down Time			35			35	µs
t_{XFR}	Page to Buffer Transfer Time			100			100	µs
t_{COMP}	Page to Buffer Compare Time			100			100	µs
t_{RST}	$\overline{RESET}$ Pulse Width	10			10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1			1	µs
t_{SWRST}	Software Reset Time			35			35	µs

Note: 1. Values are based on device characterization, not 100% tested in production.

19.5 Program and Erase Characteristics

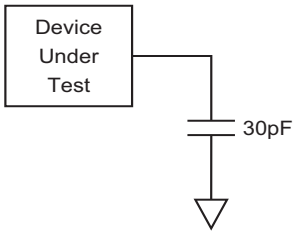
Symbol	**Parameter**	**Typ**	**Max**	**Typ**	**Max**	**Units**
t_{EP}	Page Erase and Programming Time (256/264 bytes)	10	35	10	25	ms
t_P	Page Programming Time	1.5	3	1.5	3	ms
t_{BP}	Byte Programming Time	8		8		µs
t_{PE}	Page Erase Time	6	25	6	25	ms
t_{BE}	Block Erase Time	25	35	25	35	ms
t_{SE}	Sector Erase Time	350	550	350	550	ms
t_{CE}	Chip Erase Time	3	4	3	4	s
t_{OTPP}	OTP Security Register Program Time	200	500	200	500	µs

20 Input Test Waveforms and Measurement Levels



t_R, t_F < 2ns (10% to 90%)

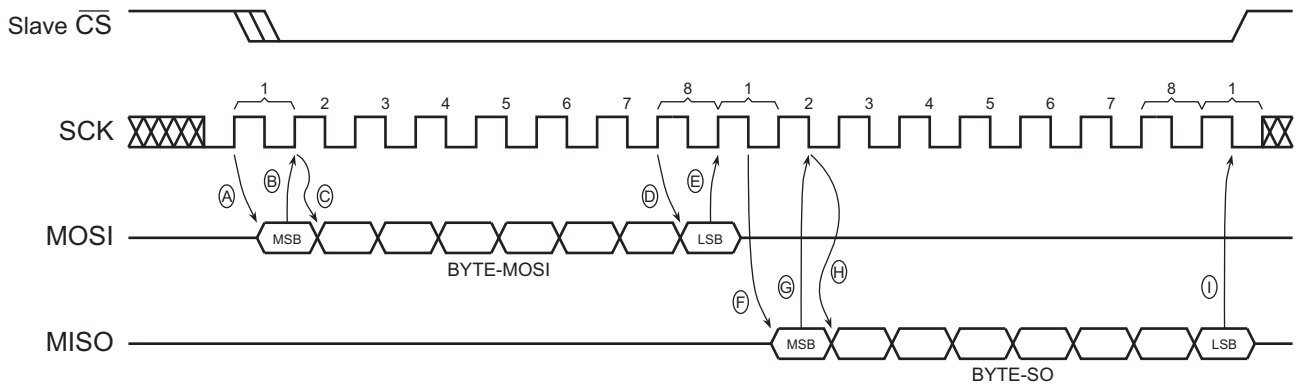
21 Output Test Load



22 Using the RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller must wait until the next falling edge of SCK to latch the data in. Similarly, the host controller must clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.



MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the DataFlash.

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
D. Last bit of BYTE-MOSI is clocked out from the Master
E. Last bit of BYTE-MOSI is clocked into the slave
F. Slave clocks out first bit of BYTE-SO
G. Master clocks in first bit of BYTE-SO
H. Slave clocks out second bit of BYTE-SO
I. Master clocks in last bit of BYTE-SO

Figure 22-1. RapidS Mode Timing

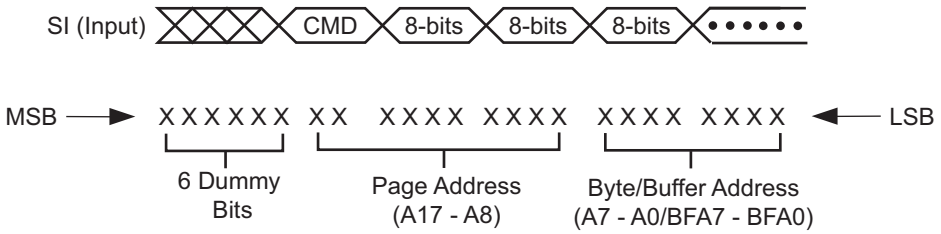


Figure 22-2. Command Sequence for Read/Write Operations for Page Size 256 Bytes (Except Status Register Read, Manufacturer, and Device ID Read)

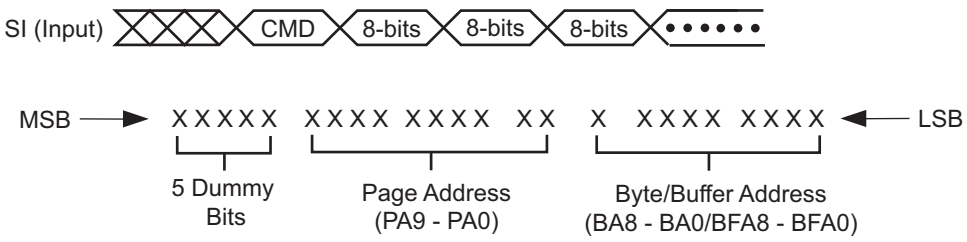


Figure 22-3. Command Sequence for Read/Write Operations for Page Size 264 Bytes (Except Status Register Read, Manufacturer, and Device ID Read)

23 AC Waveforms

Four different timing waveforms are shown in Figure 23-1 through Figure 23-4. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing Waveforms 1 and 2 conform to RapidS serial interface but for frequencies only up to 70 MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and 4 illustrate general timing diagrams for RapidS serial interface. These are similar to Waveform 1 and 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 70 MHz) of the RapidS serial case.

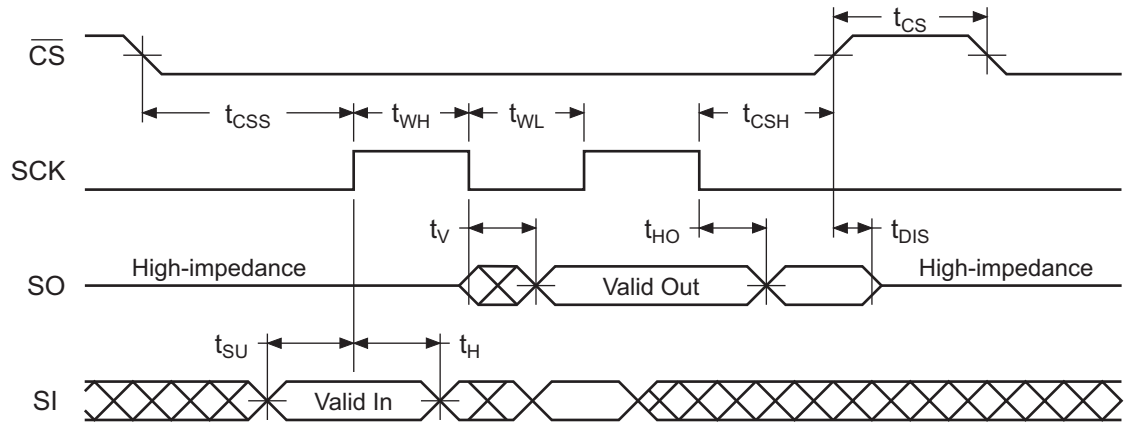


Figure 23-1. Waveform 1 = SPI Mode 0 Compatible Timing

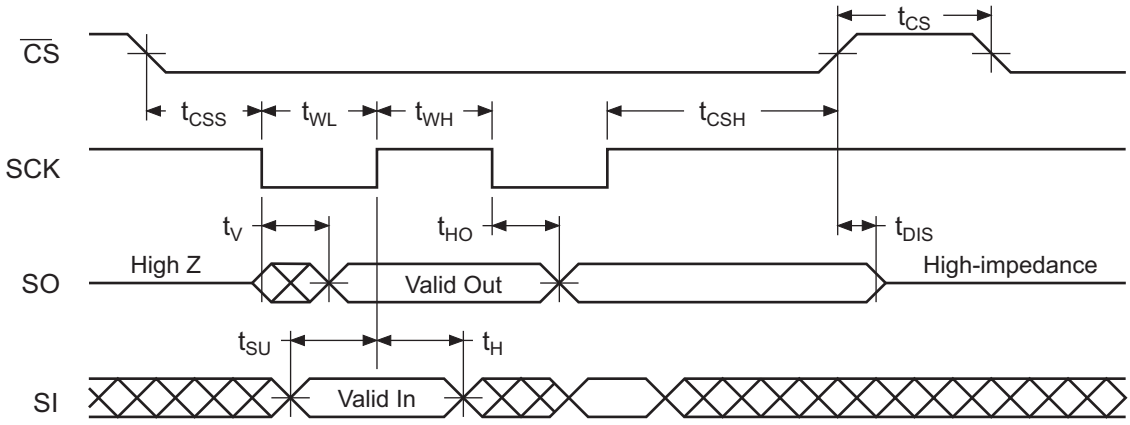


Figure 23-2. Waveform 2 = SPI Mode 3 Compatible Timing

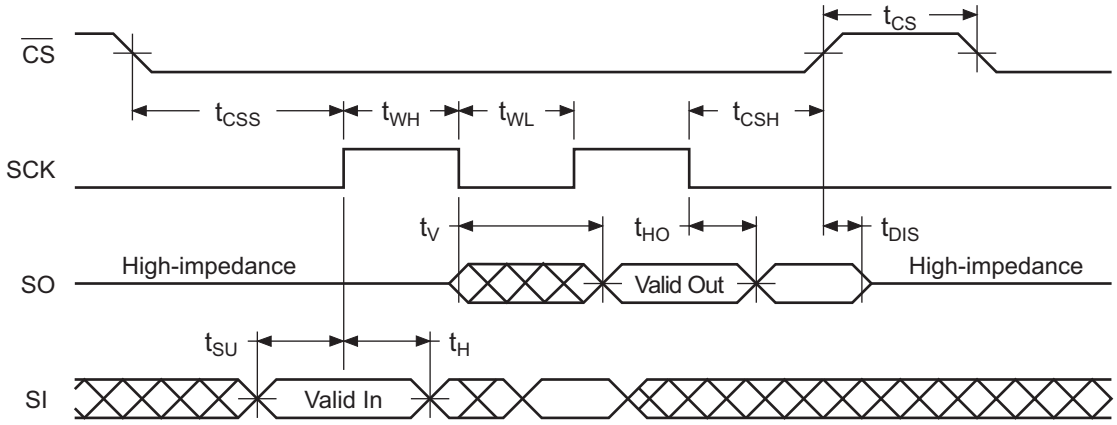


Figure 23-3. Waveform 3 = RapidS Mode 0 Timing

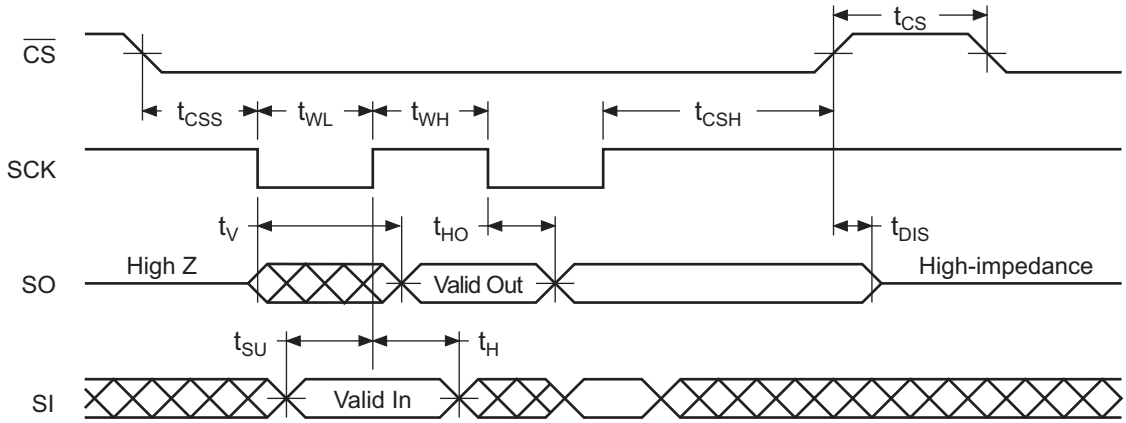


Figure 23-4. Waveform 4 = RapidS Mode 3 Timing

24 Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

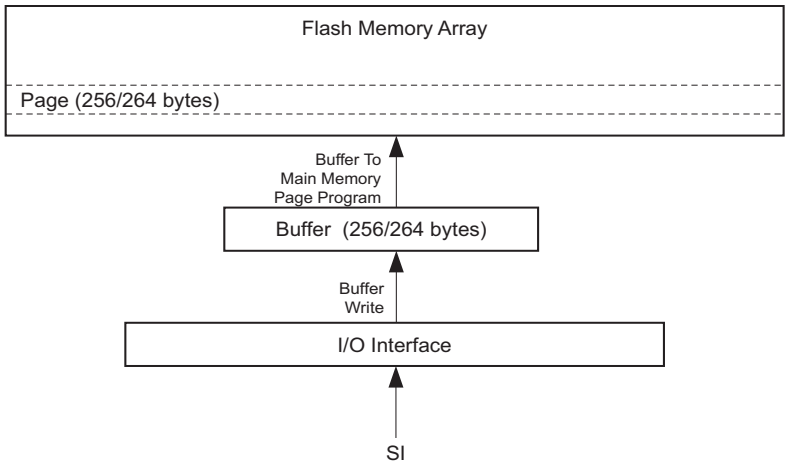


Figure 24-1. Block Diagram

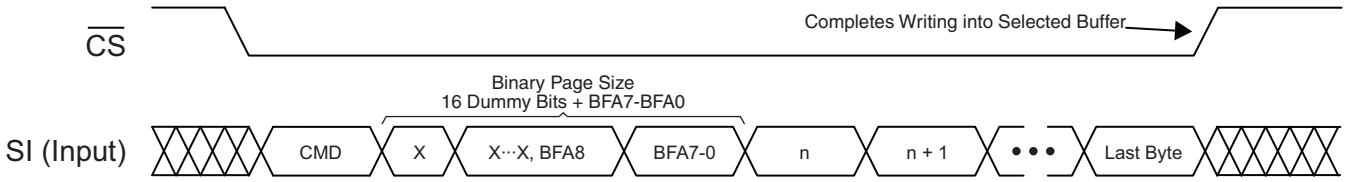


Figure 24-2. Buffer Write

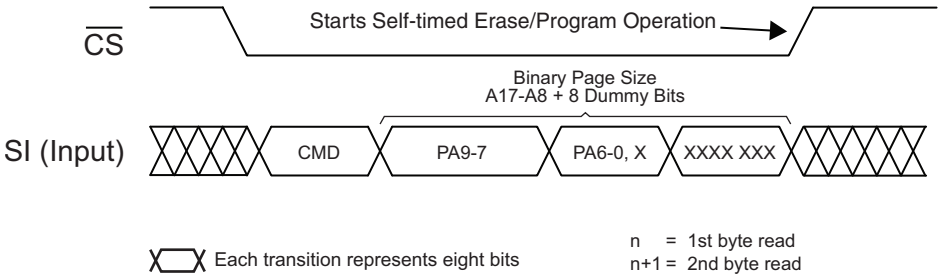


Figure 24-3. Buffer to Main Memory Page Program

25 Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

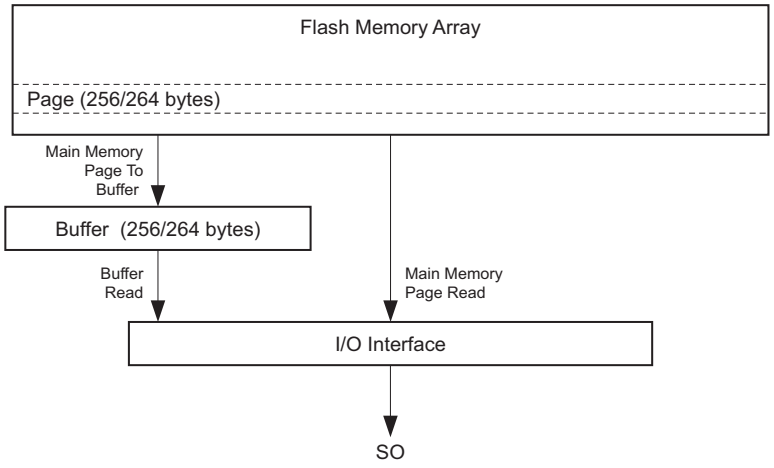


Figure 25-1. Block Diagram

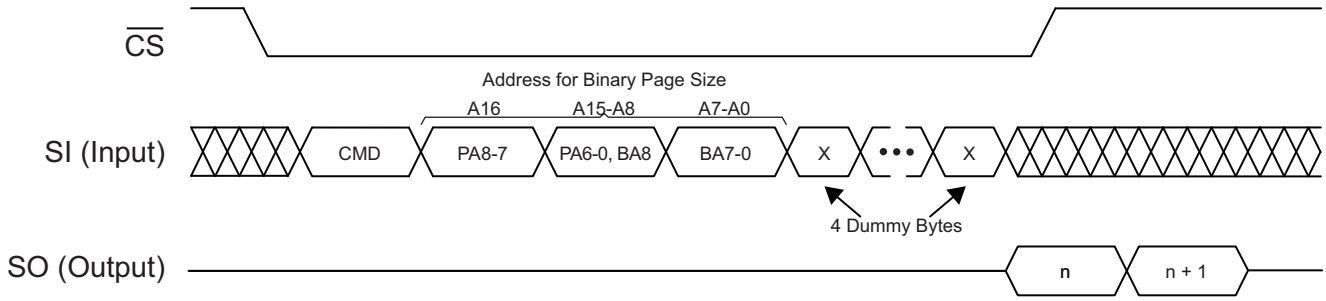


Figure 25-2. Main Memory Page Read

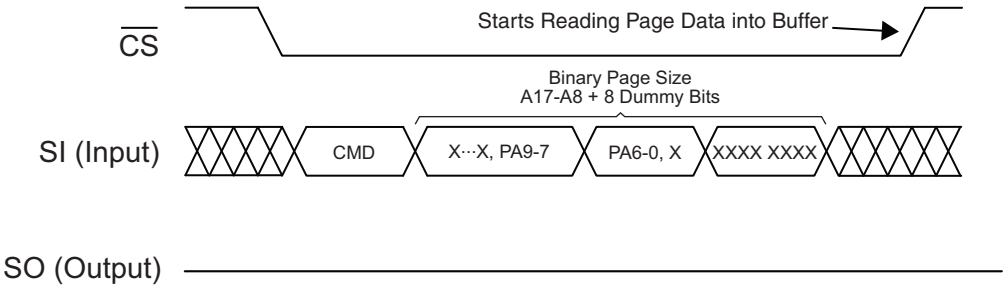


Figure 25-3. Main Memory Page to Buffer Transfer
Data From the selected Flash Page is read into the Buffer

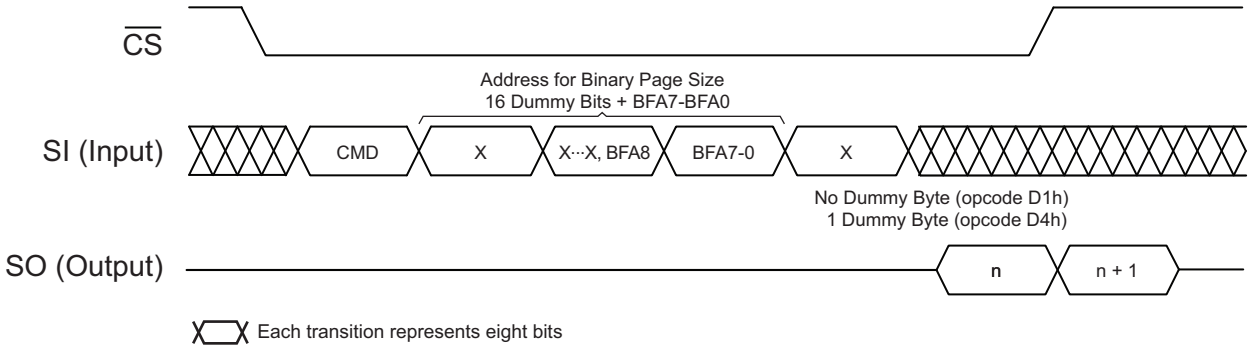


Figure 25-4. Buffer Read

26 Detailed Bit-Level Read Waveforms: RapidS Mode 0/Mode 3

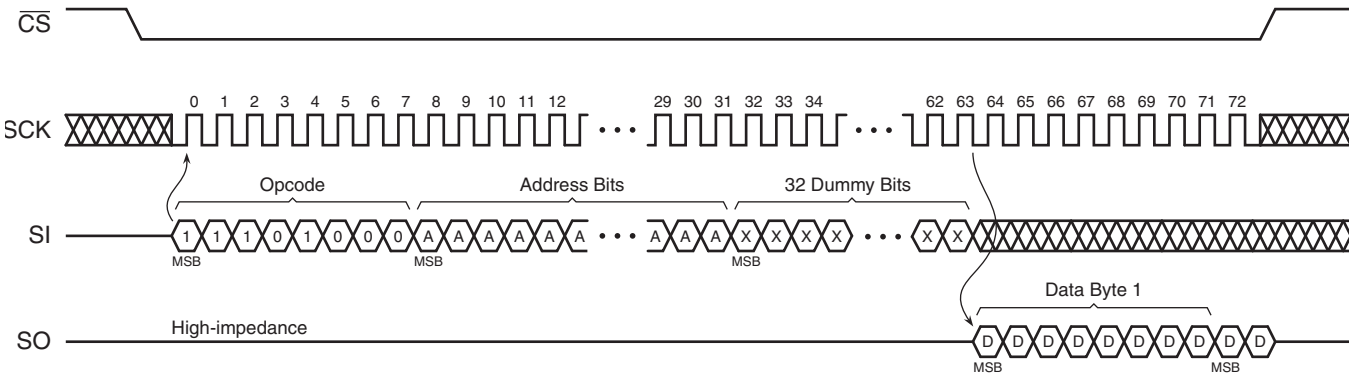


Figure 26-1. Continuous Array Read (Legacy Opcode E8h) Timing

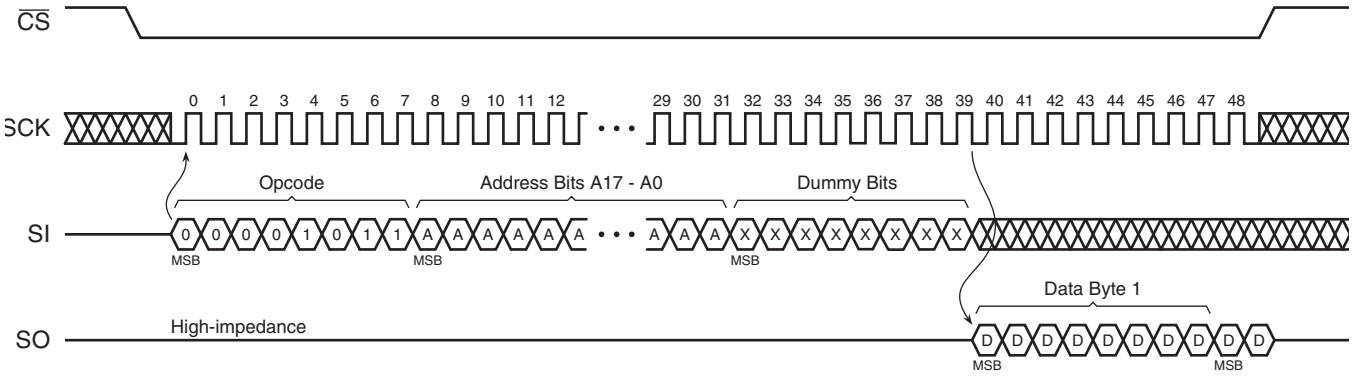


Figure 26-2. Continuous Array Read (Opcode 0Bh) Timing

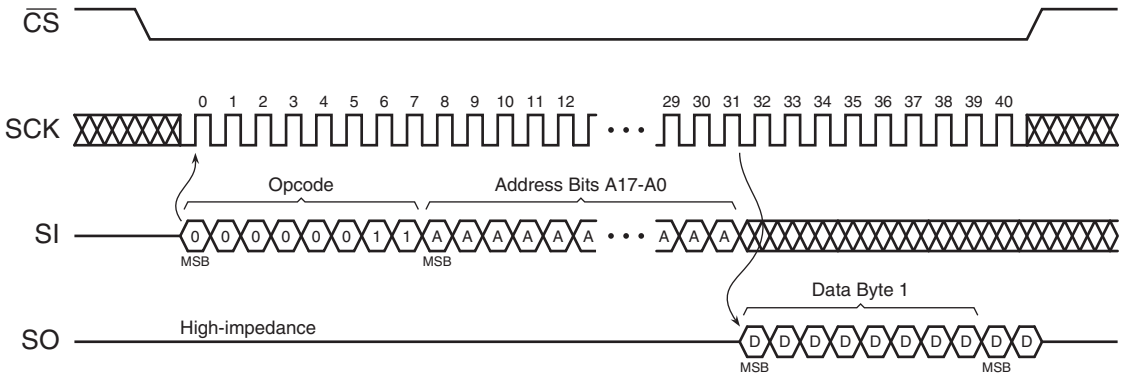


Figure 26-3. Continuous Array Read (Opcode 01h or 03h) Timing

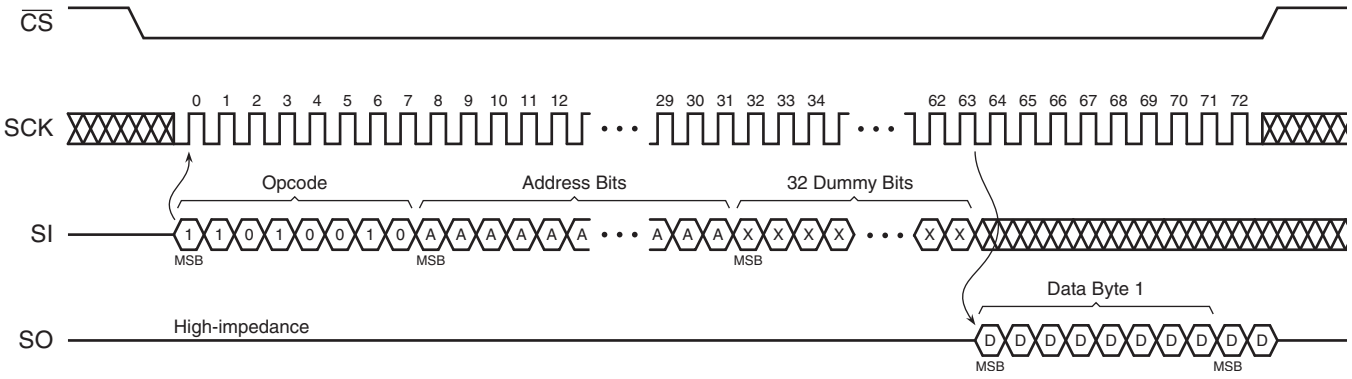


Figure 26-4. Main Memory Page Read (Opcode D2h) Timing

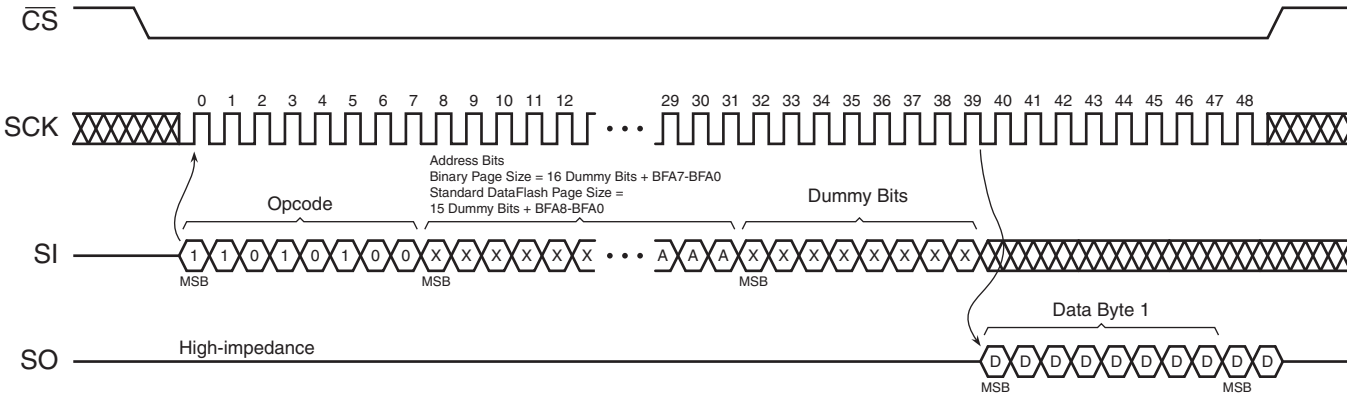


Figure 26-5. Buffer Read (Opcode D4h) Timing

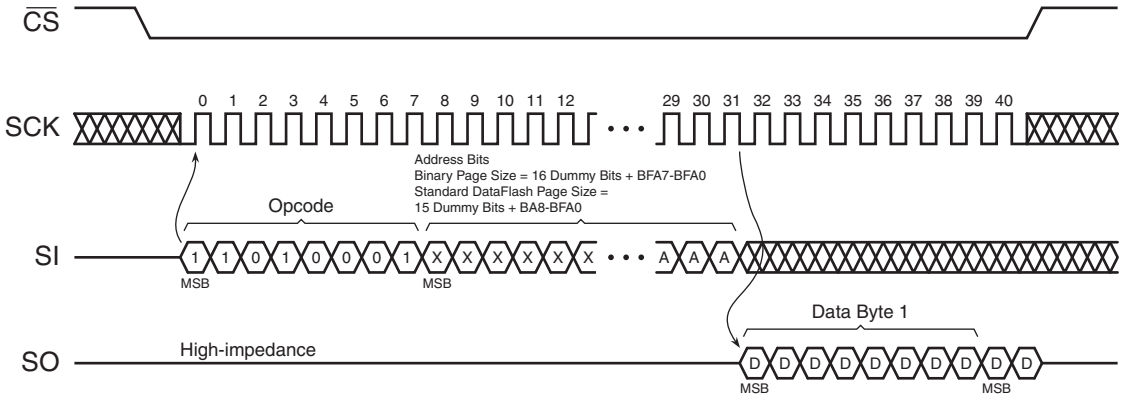


Figure 26-6. Buffer Read – Low Frequency (Opcode D1h) Timing

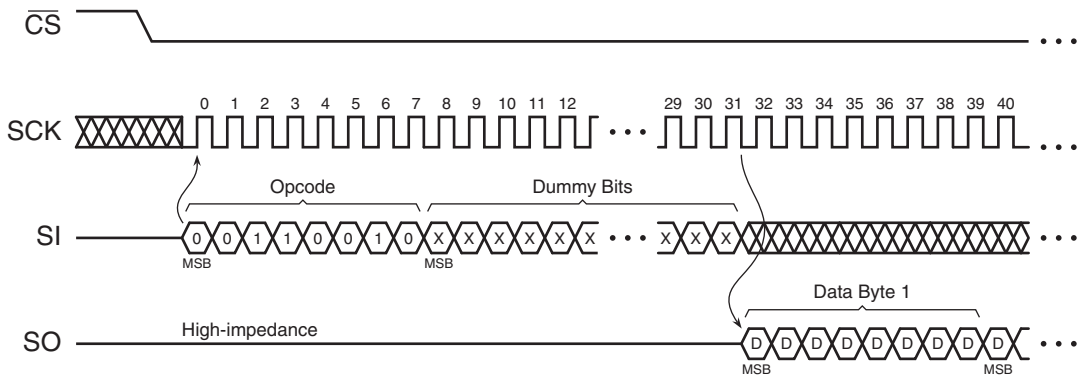


Figure 26-7. Read Sector Protection Register (Opcode 32h) Timing

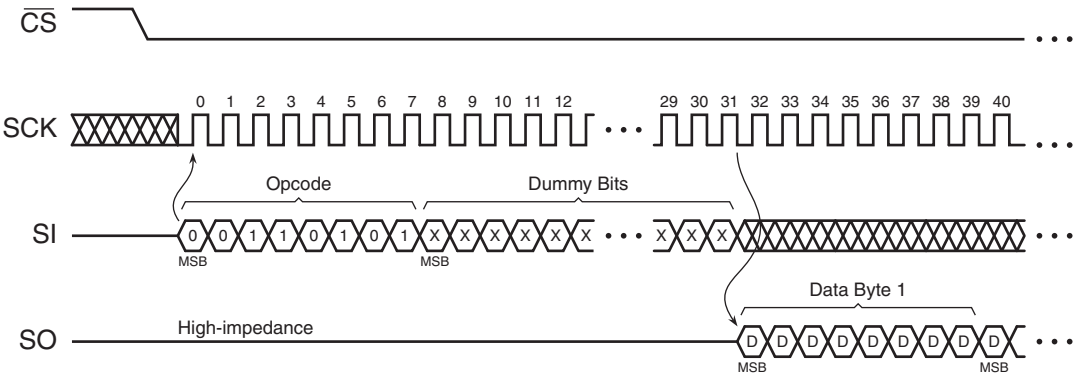


Figure 26-8. Read Sector Lockdown Register (Opcode 35h) Timing

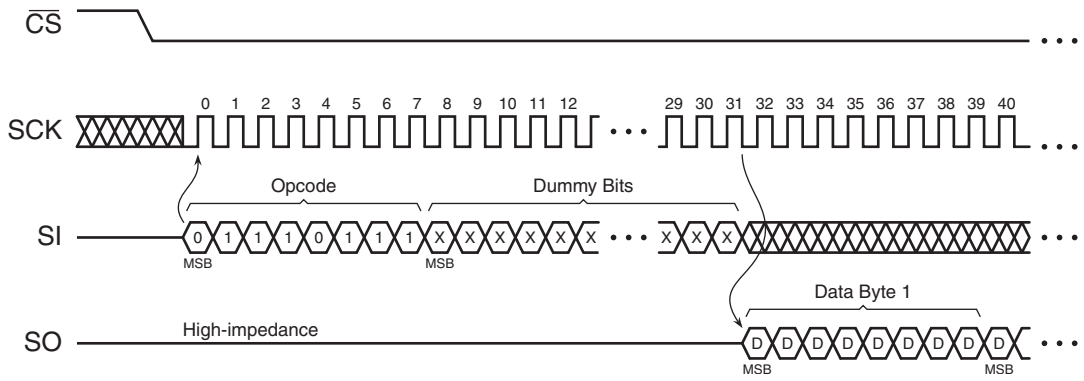


Figure 26-9. Read Security Register (Opcode 77h) Timing

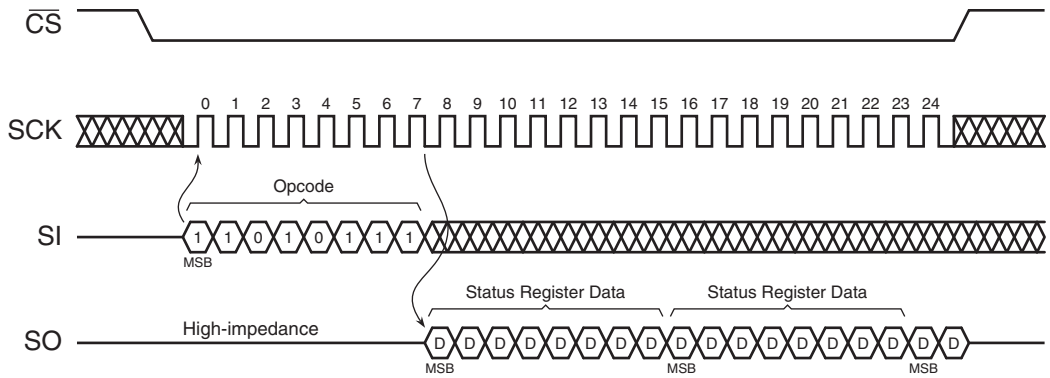


Figure 26-10. Status Register Read (Opcode D7h) Timing

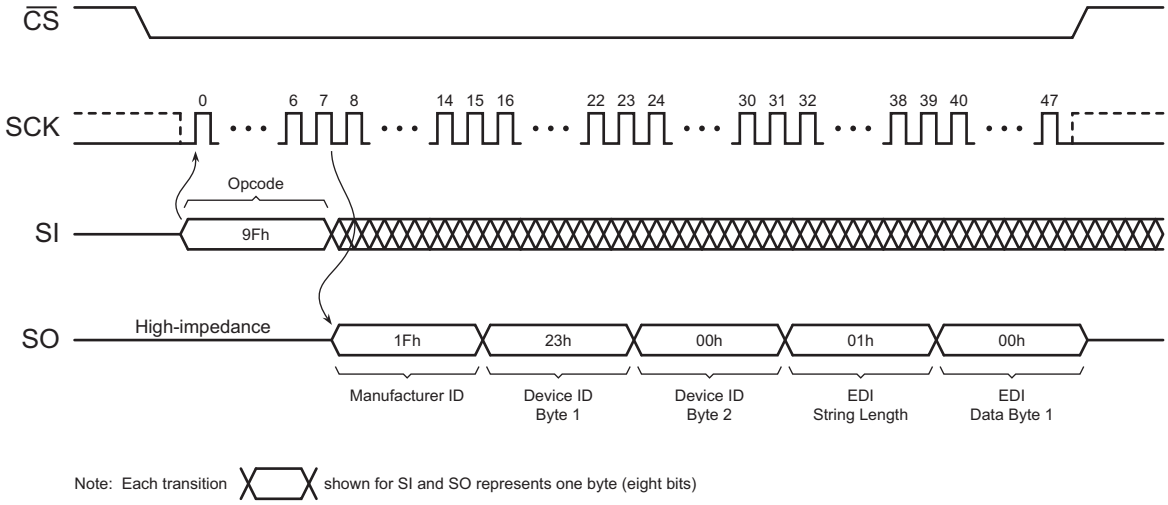


Figure 26-11. Manufacturer and Device Read (Opcode 9Fh) Timing

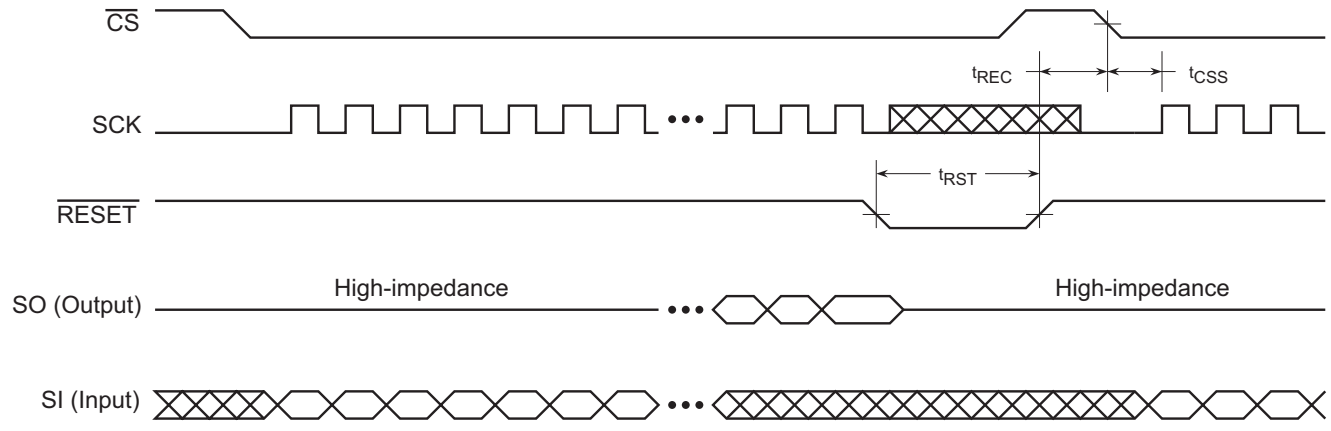


Figure 26-12. Reset Timing

Note: 1. The $\overline{CS}$ signal must be high before the $\overline{RESET}$ signal is deasserted.

27 Auto Page Rewrite Flowchart

27.1 Sequential Programming

This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page. A page can be written using either a Main Memory Page Program operation or a buffer write operation followed by a buffer to Main Memory Page Program operation. The algorithm above shows the programming of a single page. The algorithm is repeated sequentially for each page within the entire array.

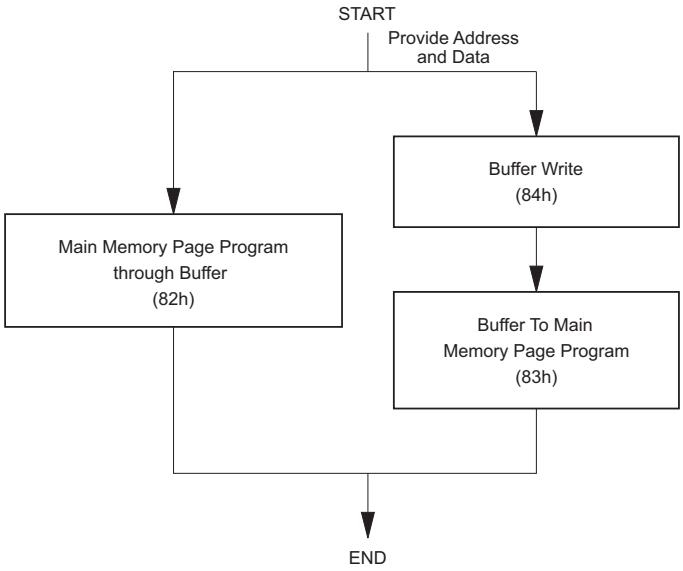


Figure 27-1. Algorithm for Programming or Re-programming of the Entire Array Sequentially

27.2 Random Programming

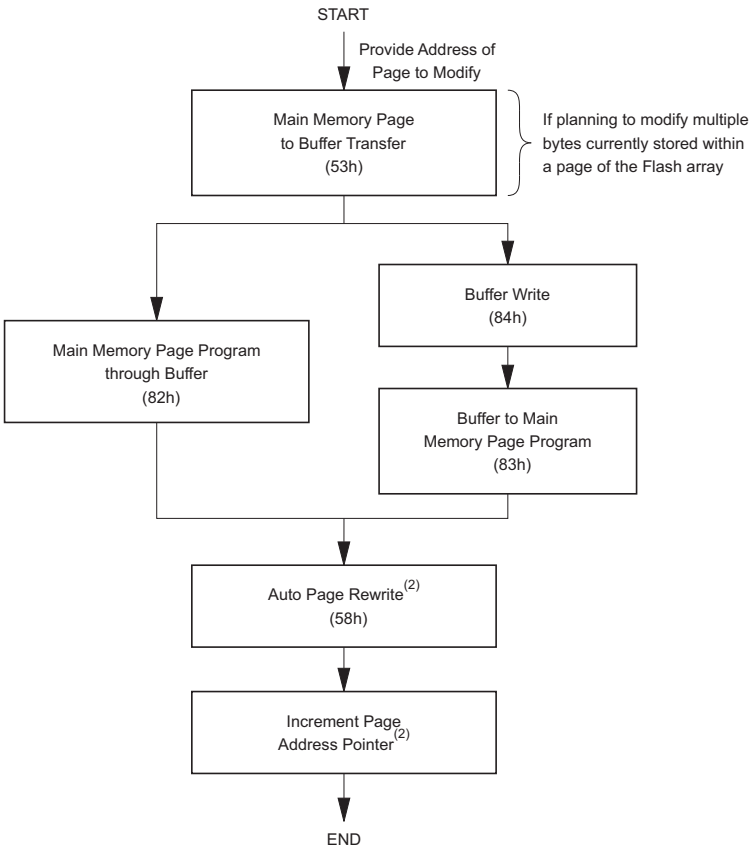
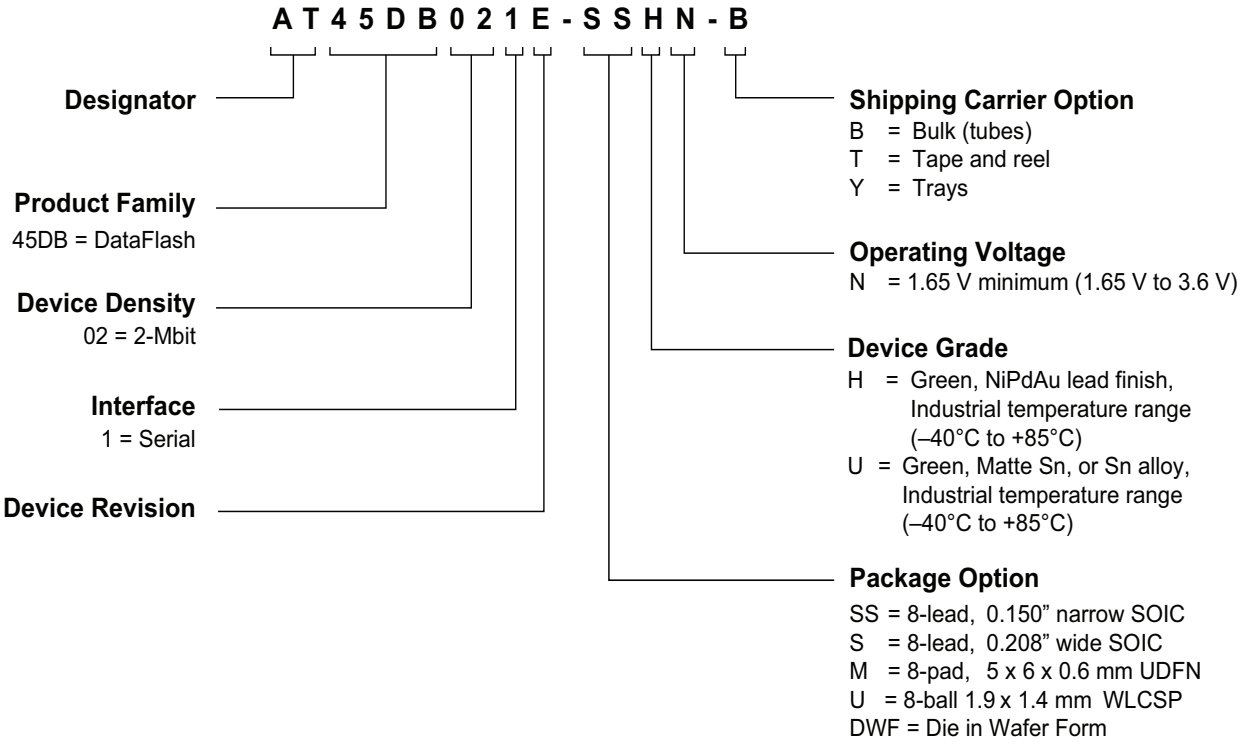


Figure 27-2. Algorithm for Programming or Re-programming of the Entire Array Randomly

Notes:
1. To preserve data integrity, each page of an DataFlash sector must be updated/rewritten at least once within every 50,000 cumulative page erase and program operations.
2. A page address pointer must be maintained to indicate which page is to be rewritten. The auto page rewrite command must use the address specified by the page address pointer
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications can choose to wait until 50,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector.

28 Ordering Information

28.1 Ordering Detail



28.2 Ordering Codes (Standard DataFlash Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB021E-SSHN-B [1]	8S1	NiPdAu	1.65 V to 3.6 V	70 MHz	Industrial (-40°C to 85°C)
AT45DB021E-SSHN-T [1]					
AT45DB021E-SHN-B [1]	8S2				
AT45DB021E-SHN-T [1]					
AT45DB021E-MHN-Y [1]	8MA1				
AT45DB021E-MHN-T [1]					
AT45DB021E-UUN-T [1,3]	CS2-8A				
AT45DB021E-DWF [2]	DWF				

Notes:
1. The shipping carrier suffix is not marked on the device.
2. Contact Adesto for mechanical drawing or Die Sales information.
3. Contact Adesto for availability.

28.3 Ordering Codes (Binary Page Mode)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB021E-SSHN2B-T [1,3]	8S1	NiPdAu	1.65 V to 3.6 V	70 MHz	Industrial (-40°C to 85°C)
AT45DB021E-SHN2B-T [1,2,3]	8S2				
AT45DB021E-MHN2B-T [1,3]	8MA1				
AT45DB021E-UUN2B-T [1,3,4]	CS2-8A				

Notes:
1. The shipping carrier suffix is not marked on the device.
2. Not recommended for new design. Use the 8S1 package option.
3. Parts ordered with suffix code ‘2B’ are shipped in tape and reel (T&R) with the page size set to 256 bytes. This option is only available for shipping in T&R (-T).
4. Contact Adesto for availability.

Package Code	Description
8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)
CS2-8A	8-ball 1.9 x 1.4 mm Wafer Level Chip Scale Package
DWF	Die in Wafer Form

28.4 Ordering Codes (Reserved)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB021E-SSHNHA-T [1,2]	8S1	NiPdAu	1.65 V to 3.6 V	70 MHz	Industrial (-40°C to 85°C)
AT45DB021E-SHNHA-T [1,2]	8S2				
AT45DB021E-SSHNHC-T [1,2]	8S1				
AT45DB021E-SHNHC-T [1,2]	8S2				

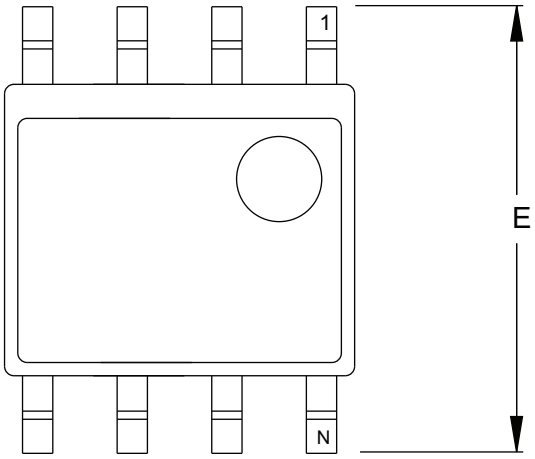
Notes:
1. The shipping carrier suffix is not marked on the device.
2. Parts ordered with suffix code ‘HA’ are shipped in tape and reel (T&R) only with the page size set to 264 bytes.
3. Parts ordered with suffix code ‘HC’ are shipped in tape and reel (T&R) only with the page size set to 256 bytes.

Contact Adesto for a description of these ‘Reserved’ codes.

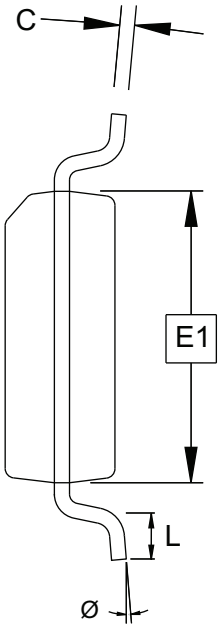
Package Code	Description
8S1	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)

29 Packaging Information

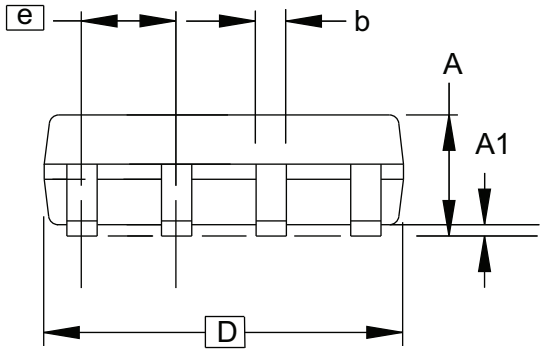
29.1 8S1 – 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

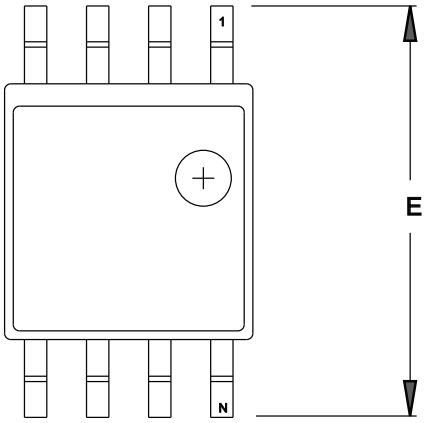
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

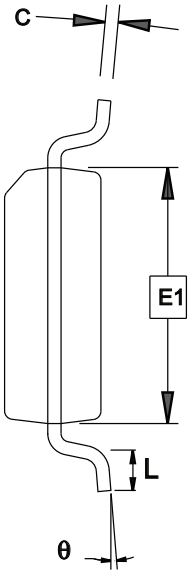
6/22/11

Adesto **Package Drawing Contact:** contact@adestotech.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

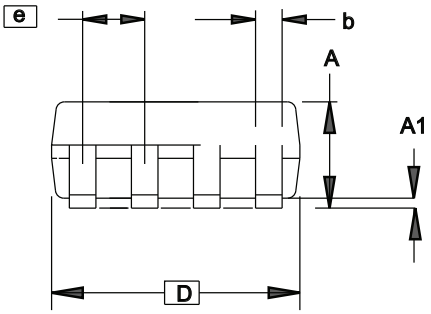
29.2 8S2 – 8-lead EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

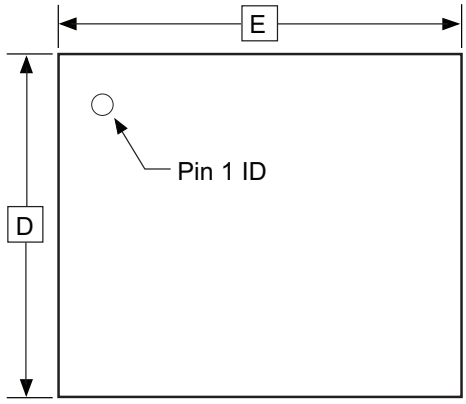
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			3

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

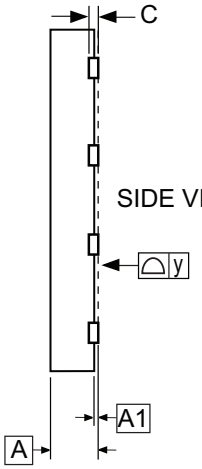
4/15/08

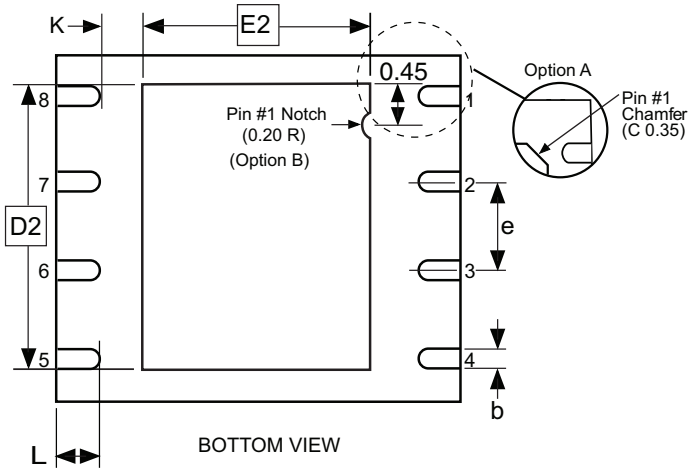
Adesto Package Drawing Contact: contact@adestotech.com	TITLE 8S2, 8-lead, 0.208” Body, Plastic Small Outline Package (EIAJ)	GPC STN	DRAWING NO. 8S2	REV. F

29.3 8MA1 – 8-pad UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

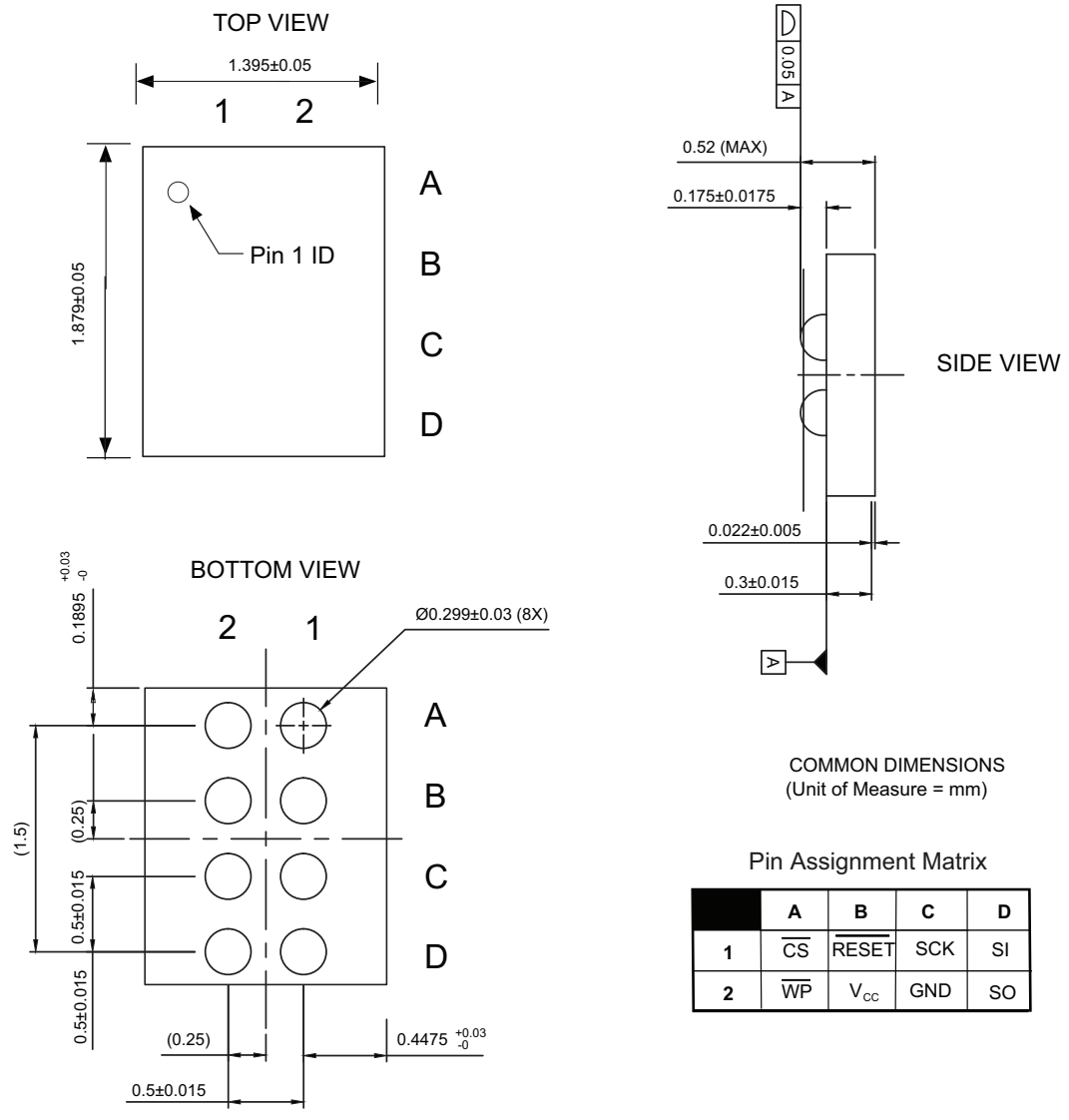
SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

Adesto Package Drawing Contact: contact@adestotech.com	TITLE 8MA1, 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	GPC YFG	DRAWING NO. 8MA1	REV. D

29.4 CS2-8A – 8-ball WLCSP



COMMON DIMENSIONS
(Unit of Measure = mm)

Pin Assignment Matrix

	A	B	C	D
1	$\overline{CS}$	$\overline{RESET}$	SCK	SI
2	$\overline{WP}$	V_{CC}	GND	SO

Notes: 1. The terminal #1 ID is a Laser-marked Feature.

12/22/15

Adesto Package Drawing Contact: contact@adestotech.com	TITLE CS2-8A, 8-ball ((2 x 4 Array), Wafer Level Chip Scale Package (WLCSP)	GPC YFG	DRAWING NO. CS2-8A	REV. A

30 Revision History

Doc. Rev.	Date	Comments
8789A	05/2012	Initial document release.
8789B	11/2012	Corrected pinout diagrams to top view. Added Read-Modify-Write section. For figures Program Sector Protection Register, Read Sector Protection Register Command, and Read Sector Lockdown Register Command, changed the opcode from n +15 to n +7. Added note at end of section, Auto Page Rewrite. Updated figure, Exit Ultra-Deep Power-Down. In table, Additional Commands, changed “Auto Page Rewrite through Buffer” to “Auto Page Rewrite or Read Modify Write through Buffer”. Power-Up Timing, increased V_{POR} max from 1.55 to 1.60. t_{XUDPD}, 1.65 V increased maximum 70µs to 120µs and 2.3 V maximum from 70µs to 240µs. tSE, increased typical from 250ms to 350ms and maximum from 450ms to 550ms. Increased 1.65 V and 2.3 V typical and maximum values for I_{DPD}, I_{SB}, I_{CC1}, and I_{CC2}. Added Legacy Commands table. Updated datasheet status to preliminary. Updated to Adesto template.
8789C	6/2013	Updated electrical and power specifications. Removed CCUN-T package from ordering codes, (not available with this device). Removed references to UBGA package (not available with this device). Moved “Buffer Read” from Group C to Group A in Operation Mode Summary. Removed reference to concurrent read capability. Removed preliminary datasheet status.
8789D	7/2013	Updated Auto Page Rewrite cycle to 50,000 cumulative page erase/program operations. Added reserved part order codes.Updated DC conditions for $V_{OL.}$
8789E	10/2013	Corrected Low Power Read Option (up to 15 MHz).
8789F	7/2015	Expanded explanation of Power up/Power down (Section 16). Added Die in Wafer Form package option.Corrected the Read-Modify-Write description (Section 6.10). Removed unavailable package and pin out diagram. Corrected Tables 15-6 and 15-7. Added information on Power Up (Section 16.1). Updated Tables 12-1 and 12-3. Updated condition description for I_{UDPD}, I_{DPD}, and $I_{SB.}$ Updated Deep Power Down and Ultra Deep Power Down timing diagrams.
8789G	3/2016	Added WLCSP package option. Updated Condition description for I_{DPD}, and I_{SB}. Added footnote to t_{DIS}, t_{EUDPD}, t_{EPD}.
8789H	1/2017	Added patent information.
8789I	7/2020	Updated format and layout. Copy edited throughout (no change in technical information). For packages ending in SHN-B and SHN-T, removed link to note in the Ordering Codes tables that states: “Not recommended for new designs. Use the 8S1 package option.”

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