

CMOS 8-Input NOR/OR

High-Voltage Types(20-Volt Rating)

DESCRIPTION

CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead dual-in-line plastic packages (N suffix), 14-lead small-outline packages (M suffixes) and 14 lead thin shrink small-outline packages (MT suffixes).

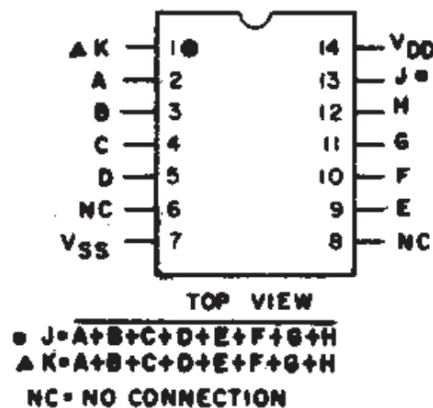
Features

- Medium-Speed Operation: $t_{PHL}, t_{PLH} = 75\text{ns}$ (typ.) at $V_{DD} = 10\text{V}$
- Buffered inputs and output
- 5V, 10V and 15V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20V
- Maximum input current of 1 μA at 18V over full package-temperature range: 100nA at 18V and 25°C
- Noise margin (over full package-temperature range): 1V at $V_{DD} = 5\text{V}$ 2V at $V_{DD} = 10\text{V}$ 2.5V at $V_{DD} = 15\text{V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B "Standard Specifications for Description of B Series CMOS Devices"

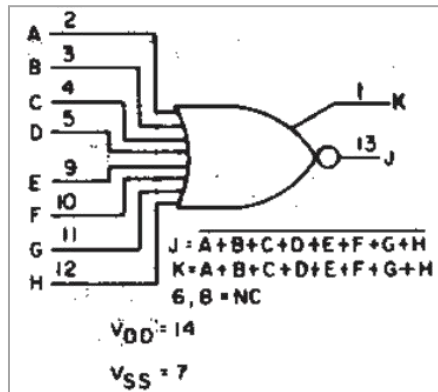
ORDERING INFORMATION

Device	Package Type	Marking	Packing	Packing Qty
CD4078BE	DIP14	CD4078BE	TUBE	1000pcs/box
CD4078BM /TR	SOP14	CD4078B	REEL	2500pcs/reel
CD4078BMT/TR	TSSOP14	CD4078B	REEL	2500pcs/reel

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONDITION		MIN	MAX
Voltages referenced to vss terminal		-0.5V	+20V
Input voltage range all inputs		-0.5V	V _{dd} +0.5V
DC input current any one input		±10mA	
Device dissipation per output transistor	for ta=full package-temperature range(all package types)	100mW	
	operating-temperature range(TA)	-40°C	+85°C
	storage temperature range(Tstg)	-65°C	+150°C
Lead temperature(during soldering): at distance 1/16±1/32inch(1.59+0.79mm)from case for 10s max		+265°C	

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CD4078BMT/TR	TSSOP14	CD4078B	REEL	2500pcs/reel

RECOMMENDED OPERATING CONDIYIONS

For maximum reliability, nominal operating conditions should be selected so shat operation is laways within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply Voltage Range (For TA Full Package Temperature Range)	5	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

At TA=25°C; Input tr tf=20ns, CL=50pf, RL=200kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
	VDD VOLTSZ		TYP.	MAX.	
Propagation Delay Time, t _{PHL} , t _{PLH}	5		150	300	ns
	10		75	150	
	15		55	110	
Propagation Time, t _{PHL} , t _{PLH}	5		400	200	ns
	10		50	100	
	15		40	80	
Input Capacitance, C _{IN}	Any Input		5	7.5	pF

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES(°C)					UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25					
				-40	+85	Min.		Typ.	
Quiescent Device Current, IDD Max.	—	0.5	5	0.25	7.5	—	0.01	0.25	μA
	—	0.10	10	0.5	15	—	0.01	0.5	
	—	0.15	15	1	30	—	0.01	1	
	—	0.20	20	5	150	—	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.61	0.42	0.51	1		mA
	0.5	0.10	10	1.5	1.1	1.3	2.6		
	1.5	0.15	15	4	2.8	3.4	6.8		
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.61	-0.42	-0.51	-1		mA
	2.5	0.5	5	-1.8	-1.3	-1.6	-3.2		
	9.5	0.10	10	-1.5	-1.1	-1.3	-2.6		
	13.5	0.15	15	-4	-2.8	-3.4	-6.8		
Output Voltage Low Level, V _{OL} Max.	—	0.5	5	0.05			0	0.05	V
	—	0.10	10	0.05			0	0.05	
	—	0.15	15	0.05			0	0.05	
Output Voltage High Level, V _{OH} Min.	—	0.5	5	1.95		4.95	5		V
	—	0.10	10	9.95		9.95	10		
	—	0.15	15	14.95		14.95	15		
Input Low Voltage. V _{IL} Max.	0.5	—	5	1.5		—	—	1.5	V
	4.5	—	5	1.5		—	—	1.5	
	1.9	—	10	3		—	—	3	
	1.5	—	15	4		—	—	4	
Input High Voltage. V _{IN} Min.	0.5	—	5	3.5		3.5	—	—	V
	4.5	—	5	3.5		3.5	—	—	
	1.9	—	10	7		7	—	—	
	1.5	—	15	11		11	—	—	
Input Current V _{IN} Max.		0.18	18	±0.1	±1	—	±10-5	±0.1	μA

TYPICAL CHARACTERISTIC

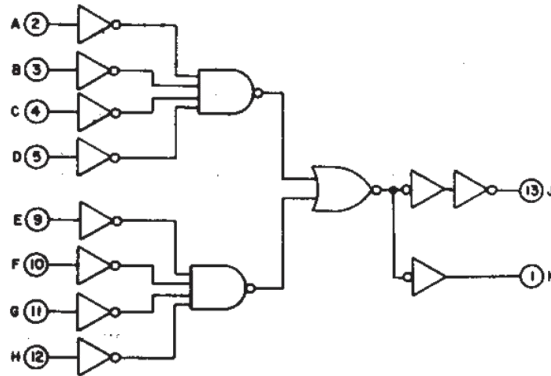


Fig.1-Logic diagram.

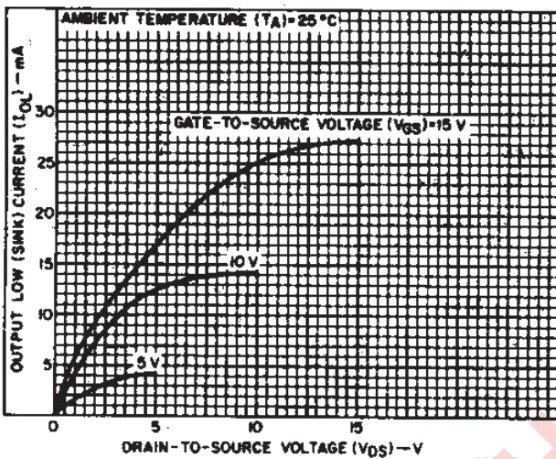


Fig.2-Typical output low(sink) current characteristics.

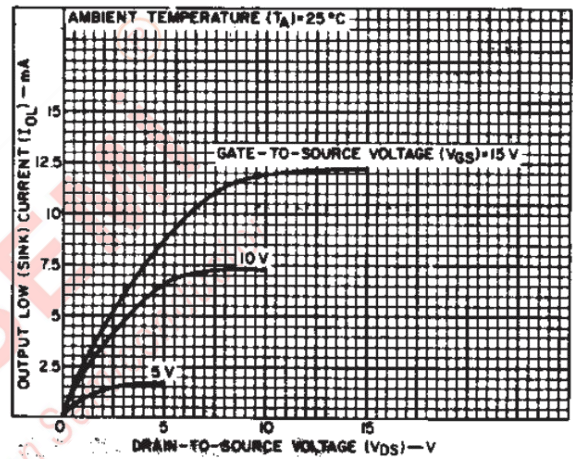


Fig.3-Minimum output low(sink) current characteristics.

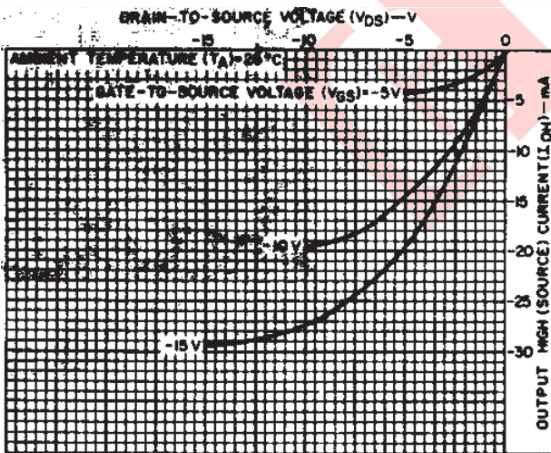


Fig.4 -Typical output high(souce)current characteristics.

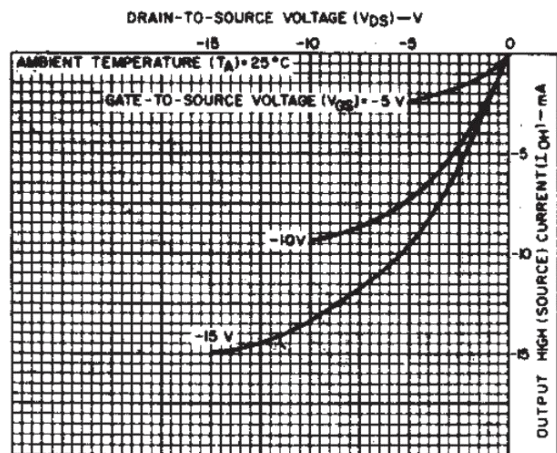


Fig.5 -Minimum output high(source)currnt characteristics.

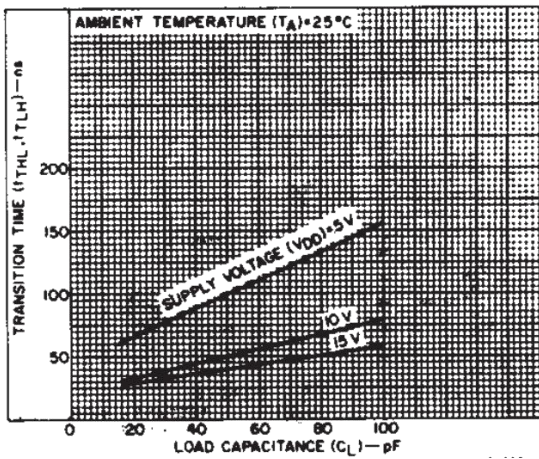


Fig.6 -Typical transition time as a function of load capacitance.

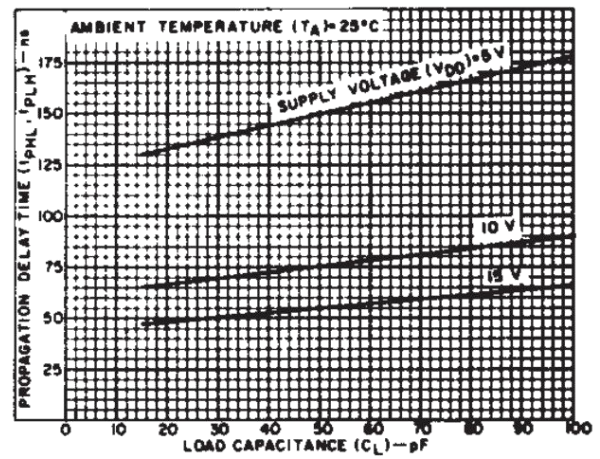


Fig.7 -Typical propagation delay time as a function of load capacitance.

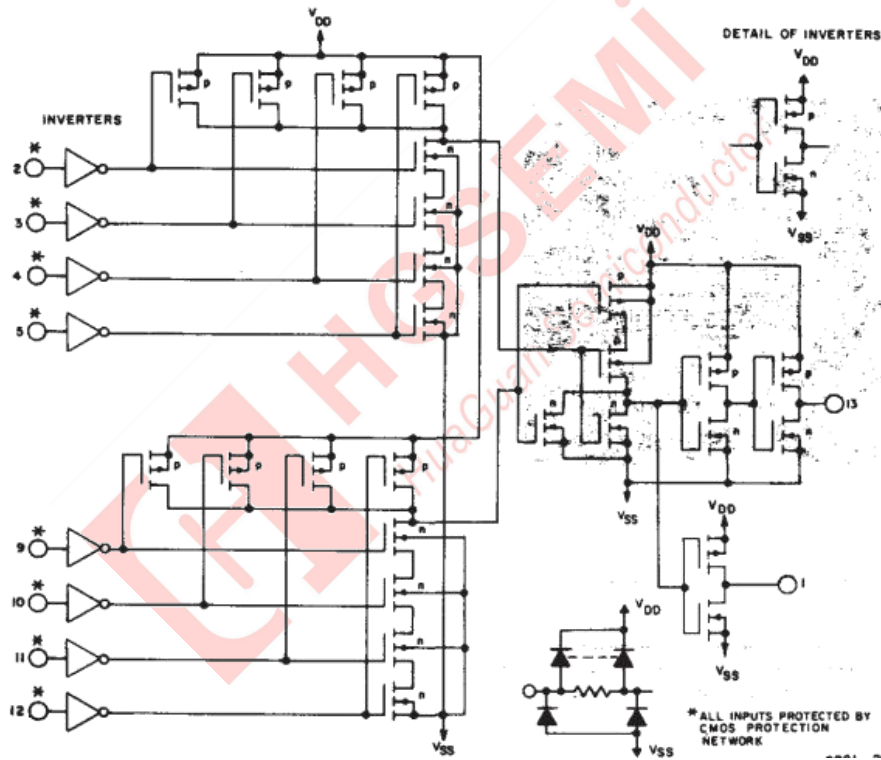


Fig.8 -Schematic diagram.

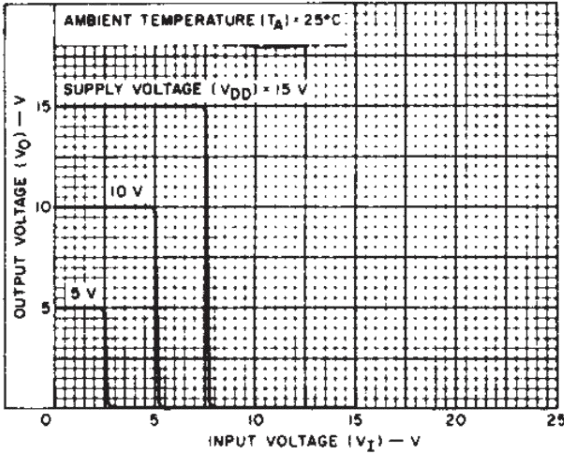


Fig.9 -Typical voltage transfer charac-teristics(NOR output).

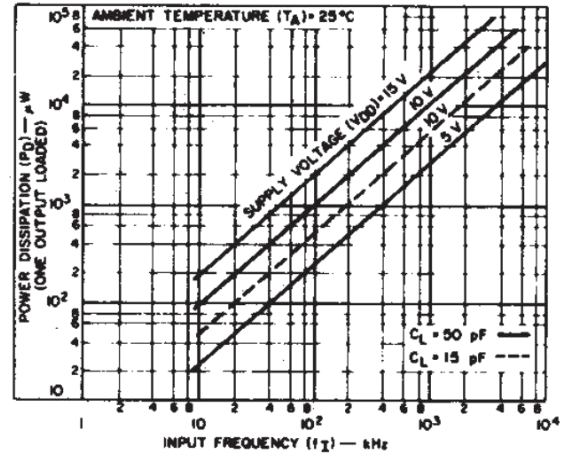


Fig.10 -Typical dynamic power dissipation as a function of frequency.

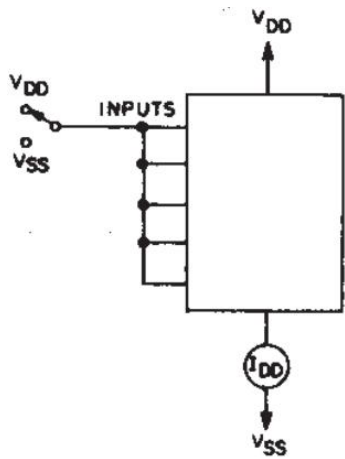


Fig.11 -Quiescent-device-current test circuit.

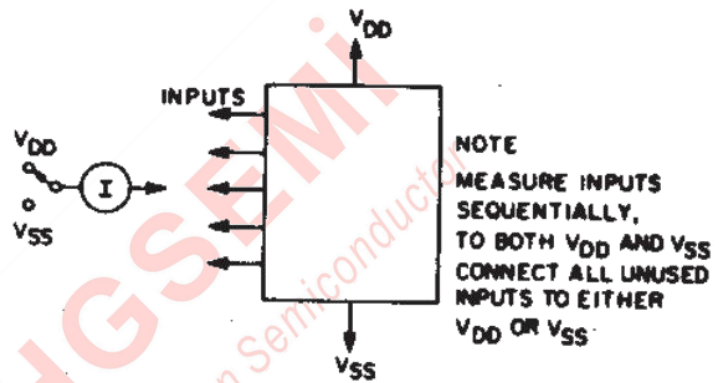


Fig.12 -Input current test circuit.

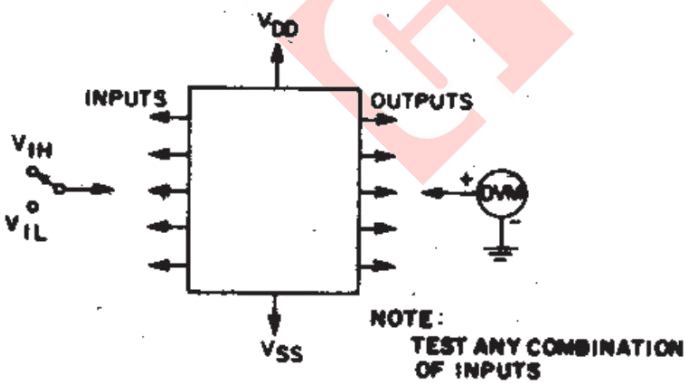


Fig.13 -Input voltage test circuit.

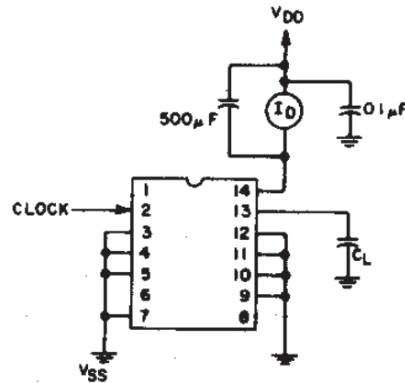
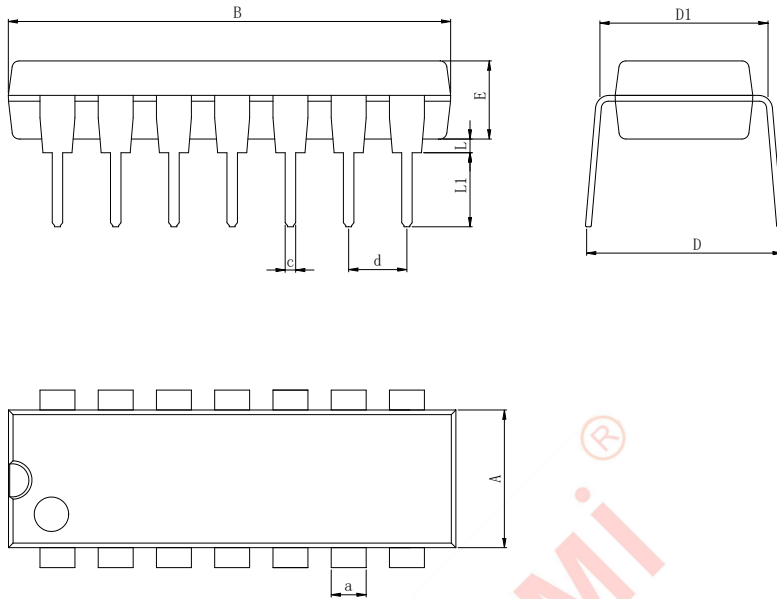


Fig.14 -Dynamic power dissipation test circuit

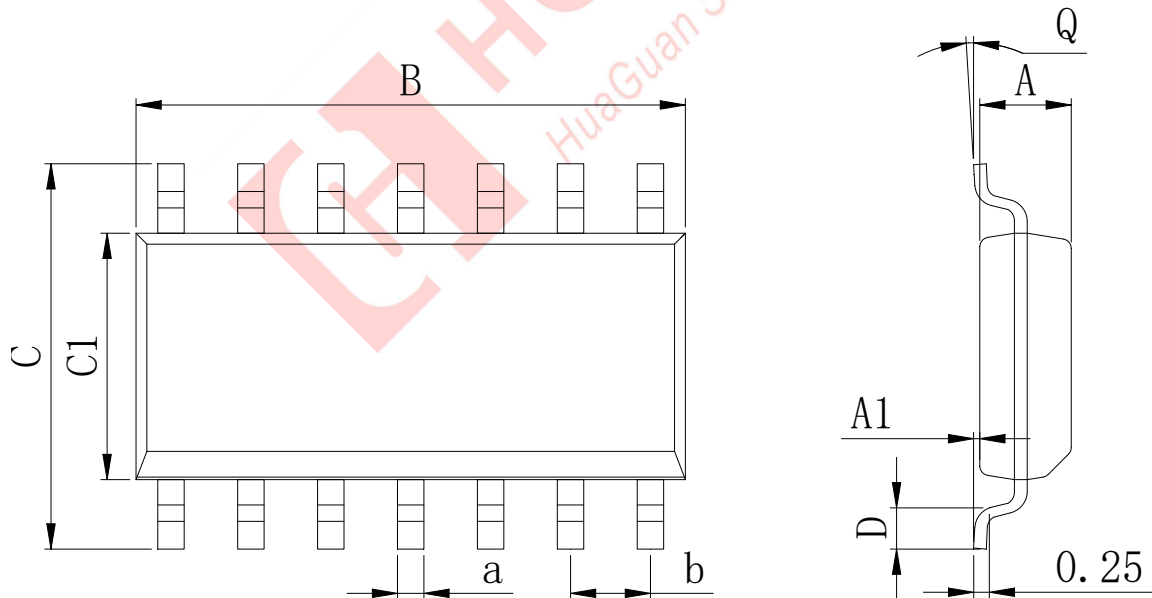
Physical Dimensions

DIP-14L



Dimensions In Millimeters(DIP14L)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

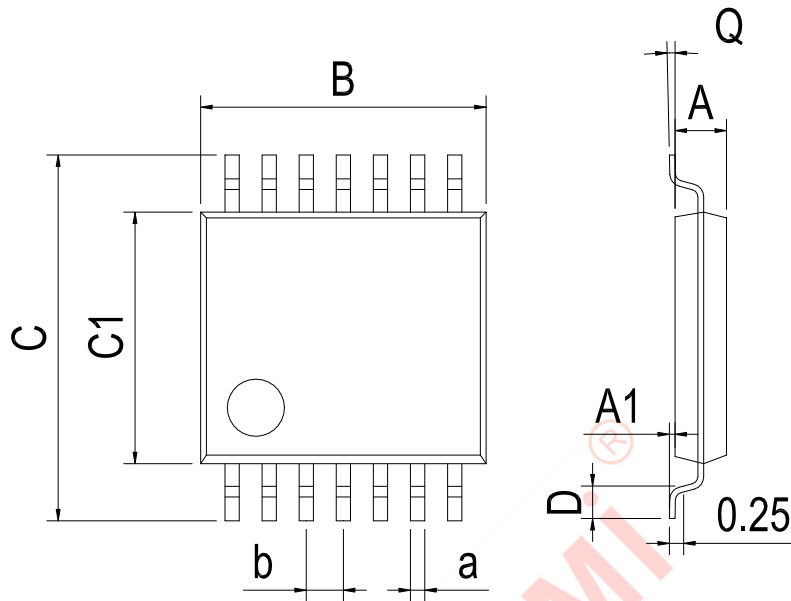
SOP14L



Dimensions In Millimeters(SOP14L)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-14L



Dimensions In Millimeters(TSSOP14L)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

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