High Voltage, Latch-up Proof, 4-Channel Multiplexer

Data Sheet

ADG5404

FEATURES

- Latch-up proof
- 8 kV HBM ESD rating
- Low on resistance (<10 Ω)
- ±9 V to ±22 V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at ±15 V, ±20 V, +12 V, and +36 V
- V_{SS} to V_{DD} analog signal range

FUNCTIONAL BLOCK DIAGRAM

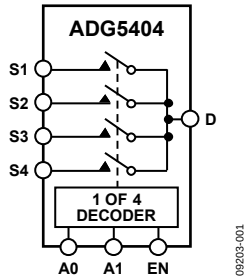

Figure 1.

APPLICATIONS

- Relay replacement
- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems

GENERAL DESCRIPTION

The ADG5404 is a complementary metal-oxide semiconductor (CMOS) analog multiplexer, comprising four single channels.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

The ADG5404 is designed on a trench process, which guards against latch-up. A dielectric trench separates the P and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.

The ADG5404 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up. A dielectric trench separates the P and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON}.
3. Dual-Supply Operation. For applications where the analog signal is bipolar, the ADG5404 can be operated from dual supplies of up to ±22 V.
4. Single-Supply Operation. For applications where the analog signal is unipolar, the ADG5404 can be operated from a single-rail power supply of up to 40 V.
5. 3 V logic-compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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7/2011—Rev. 0 to Rev. A

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7/2010—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9.8			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 23
	11	14	16	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.2			Ω typ	V_S = ±10 V, I_S = −10 mA
	1.6	2	2.2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.4	±2	±16	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 25
	±0.4	±2	±16	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	187			ns typ	R_L = 300 Ω, C_L = 35 pF
	242	285	330	ns max	V_S = 10 V; see Figure 30
t_{ON} (EN)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	204	247	278	ns max	V_S = 10 V; see Figure 32
t_{OFF} (EN)	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	168	183	ns max	V_S = 10 V; see Figure 32
Break-Before-Make Time Delay, t_D	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			12	ns min	V_{S1} = V_{S2} = 10 V; see Figure 31
Charge Injection, Q_{INJ}	220			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.009			% typ	R_L = 1k Ω, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	53			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss	−0.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)	19			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	92			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	132			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 23
	10	13	15	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.5			Ω typ	V_S = ±15 V, I_S = −10 mA
	1.8	2.2	2.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 24
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 24
	±0.4	±2	±16	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 25
	±0.4	±2	±16	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	175			ns typ	R_L = 300 Ω, C_L = 35 pF
	224	262	301	ns max	V_S = +10 V; see Figure 30
t_{ON} (EN)	148			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	222	250	ns max	V_S = 10 V; see Figure 32
t_{OFF} (EN)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	142	159	173	ns max	V_S = 10 V; see Figure 32
Break-Before-Make Time Delay, t_D	40			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 31
Charge Injection, Q_{INJ}	290			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.008			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	54			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss	−0.6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)	18			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	88			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	129			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			μA typ	Digital inputs = 0 V or V_{DD}
	70		110	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

+12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	19			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 23
	22	27	31	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.8	1	1.2	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	4.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	5.5	6.5	7.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.4	±2	±16	nA max	
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = 1 V/10 V; see Figure 25
	±0.4	±2	±16	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	266			ns typ	R_L = 300 Ω, C_L = 35 pF
	358	446	515	ns max	V_S = +8 V; see Figure 30
t_{ON} (EN)	260			ns typ	R_L = 300 Ω, C_L = 35 pF
	339	423	485	ns max	V_S = 8 V; see Figure 32
t_{OFF} (EN)	135			ns typ	R_L = 300 Ω, C_L = 35 pF
	162	189	210	ns max	V_S = 8 V; see Figure 32
Break-Before-Make Time Delay, t_D	125			ns typ	R_L = 300 Ω, C_L = 35 pF
			45	ns min	V_{S1} = V_{S2} = 8 V; see Figure 31
Charge Injection, Q_{INJ}	92			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1MHz; see Figure 26
Channel-to-Channel Crosstalk	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.075			% typ	R_L = 1k Ω, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	43			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss	−1.36			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)	22			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	105			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	140			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			μA typ	Digital inputs = 0 V or V_{DD}
	50		65	μA max	
V_{DD}			9/40	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

+36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	10.6			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 23
	12	15	17	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.7			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	3.2	3.8	4.5	Ω max	
LEAKAGE CURRENTS					V_{DD} =39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 24
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 24
	±0.4	±2	±16	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/30 V; see Figure 25
	±0.4	±2	±16	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	196			ns typ	R_L = 300 Ω, C_L = 35 pF
	256	276	314	ns max	V_S = 18 V; see Figure 30
t_{ON} (EN)	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	214	247	273	ns max	V_S = 18 V; see Figure 32
t_{OFF} (EN)	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	172	167	176	ns max	V_S = 18 V; see Figure 32
Break-Before-Make Time Delay, t_D	52			ns typ	R_L = 300 Ω, C_L = 35 pF
			13	ns min	V_{S1} = V_{S2} = 18 V; see Figure 31
Charge Injection, Q_{INJ}	280			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1MHz; see Figure 26
Channel-to-Channel Crosstalk	−58			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 1k Ω, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	47			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
Insertion Loss	−0.85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
C_S (Off)	18			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	89			pF typ	V_S = 18 V, f = 1 MHz
C_D, C_S (On)	128			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			μA typ	Digital inputs = 0 V or V_{DD}
	100		130	μA max	
V_{DD}			9/40	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	165	96	49	mA max
LFCSP (θ_{JA} = 30.4°C/W)	290	141	57	mA max
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	176	101	51	mA max
LFCSP (θ_{JA} = 30.4°C/W)	282	146	58	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	114	72	42	mA max
LFCSP (θ_{JA} = 30.4°C/W)	203	112	53	mA max
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	149	89	48	mA max
LFCSP (θ_{JA} = 30.4°C/W)	263	133	56	mA max

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	515 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D[2]	Data + 15%
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the Sx and D pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

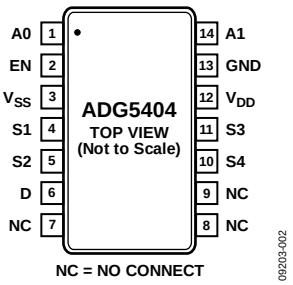


Figure 2. TSSOP Pin Configuration

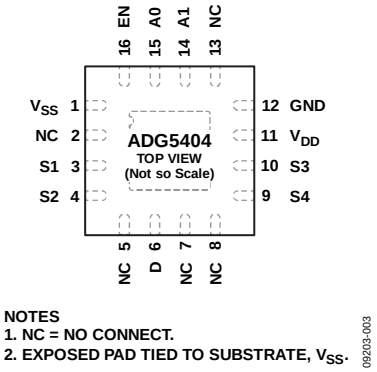


Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
3	1	V_{SS}	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. Can be an input or an output.
5	4	S2	Source Terminal. Can be an input or an output.
6	6	D	Drain Terminal. Can be an input or an output.
7 to 9	2, 5, 7, 8, 13	NC	No Connection.
10	9	S4	Source Terminal. Can be an input or an output.
11	10	S3	Source Terminal. Can be an input or an output.
12	11	V_{DD}	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

TRUTH TABLE

Table 8.

EN	A1	A0	S1	S2	S3	S4
0	X[1]	X[1]	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

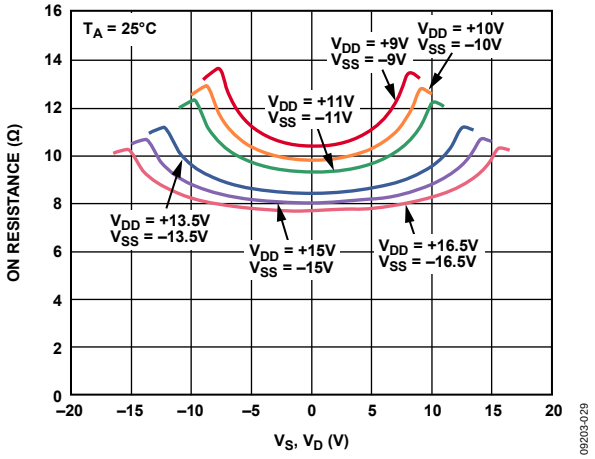


Figure 4. R_{ON} as a Function of V_D (V_S), Dual Supply

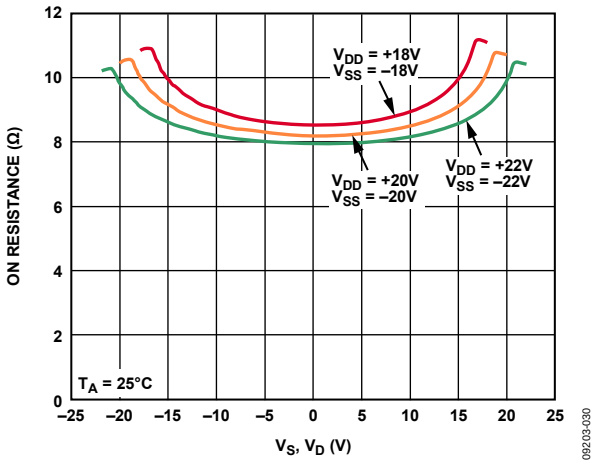


Figure 5. R_{ON} as a Function of V_D (V_S), Dual Supply

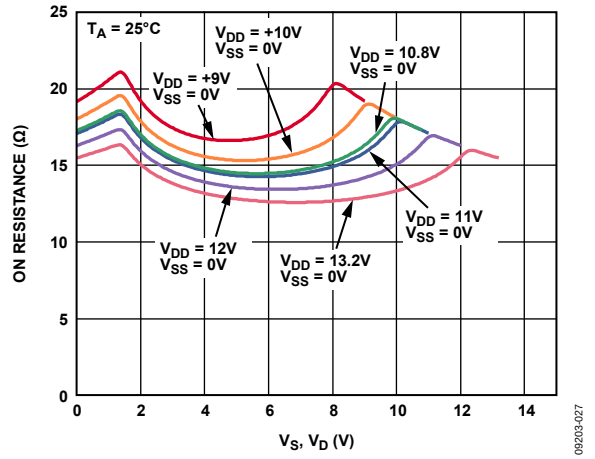


Figure 6. R_{ON} as a Function of V_D (V_S), Single Supply

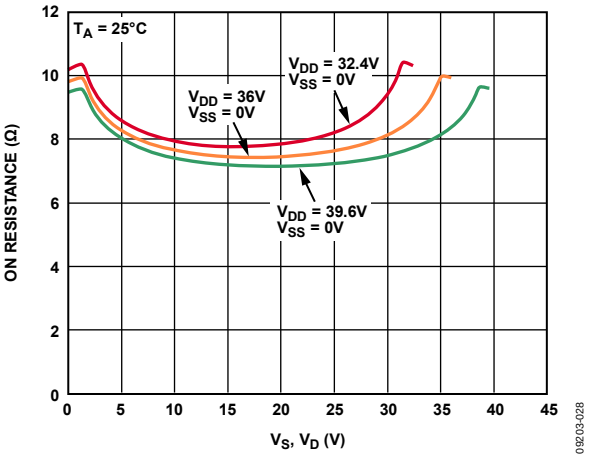


Figure 7. R_{ON} as a Function of V_D (V_S), Single Supply

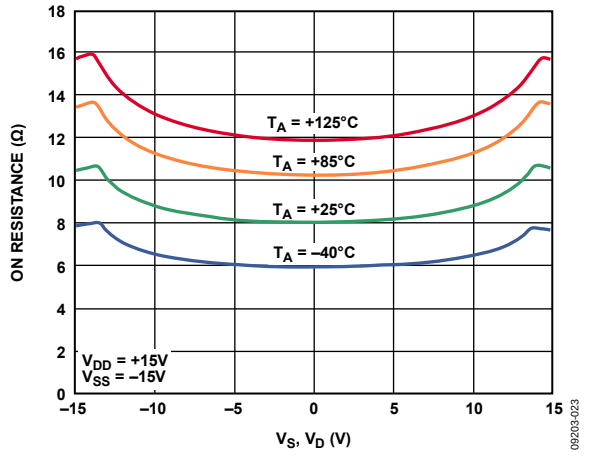


Figure 8. R_{ON} as a Function of V_D (V_S) for Different Temperatures, ±15 V Dual Supply

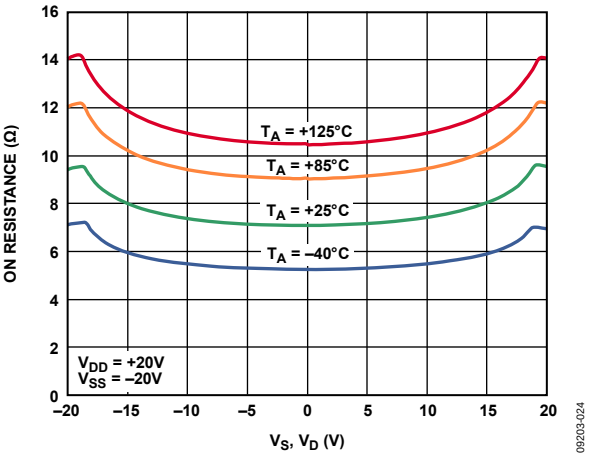


Figure 9. R_{ON} as a Function of V_D (V_S) for Different Temperatures, ±20 V Dual Supply

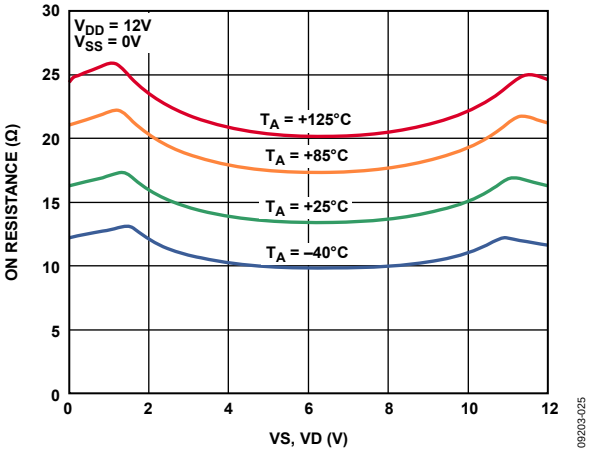


Figure 10. R_{ON} as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

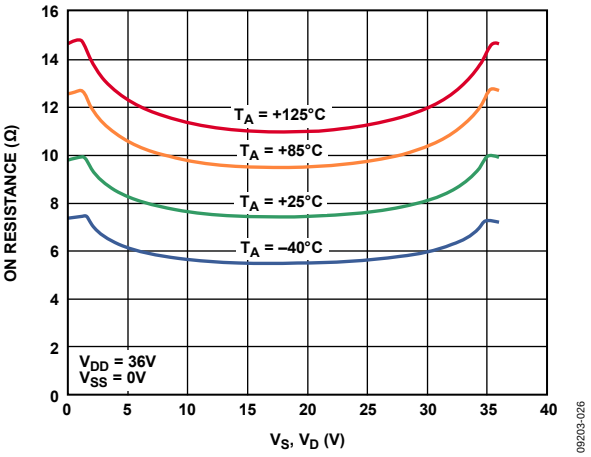


Figure 11. R_{ON} as a Function of V_D (V_S) for Different Temperatures, 36 V Single Supply

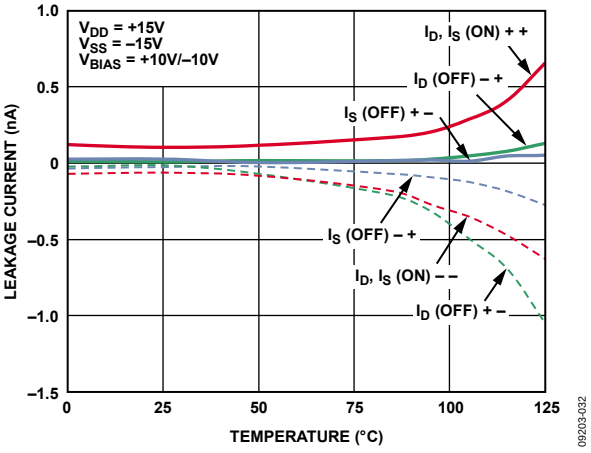


Figure 12. Leakage Currents vs. Temperature, ±15 V Dual Supply

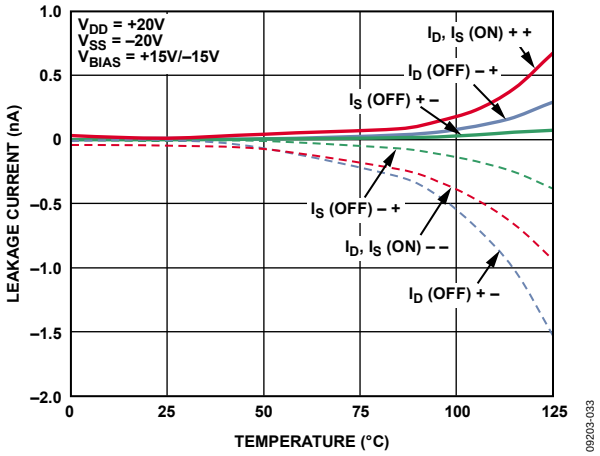


Figure 13. Leakage Currents vs. Temperature, ±20 V Dual Supply

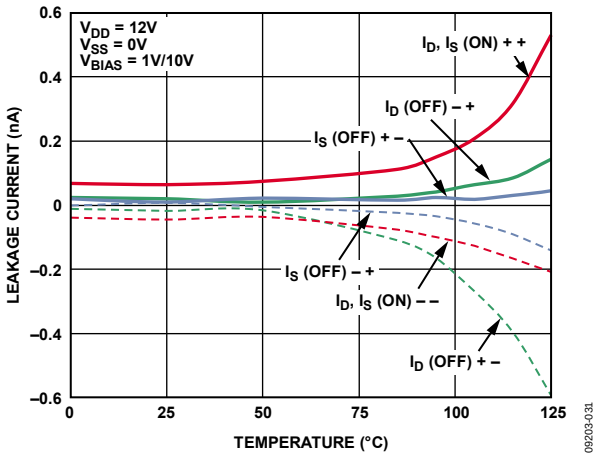


Figure 14. Leakage Currents vs. Temperature, 12 V Single Supply

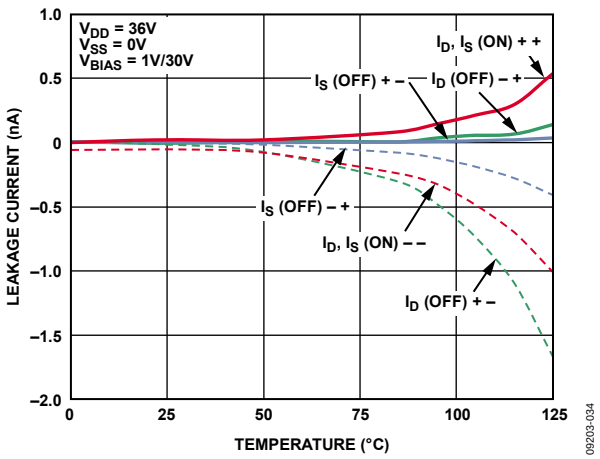


Figure 15. Leakage Currents vs. Temperature, 36 V Single Supply

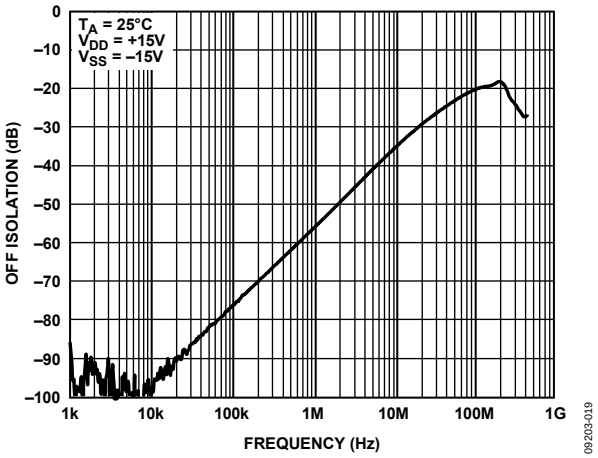


Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

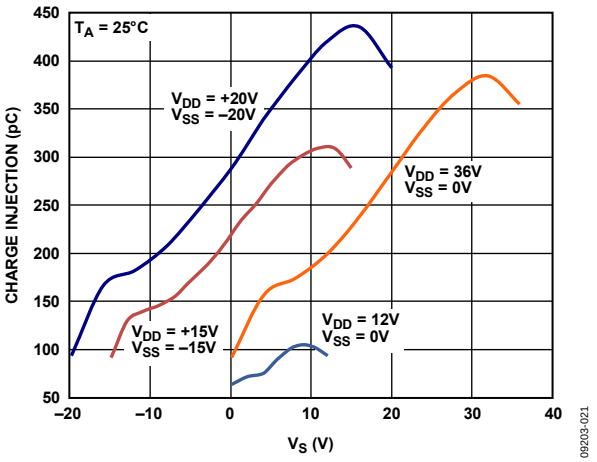


Figure 19. Charge Injection vs. Source Voltage

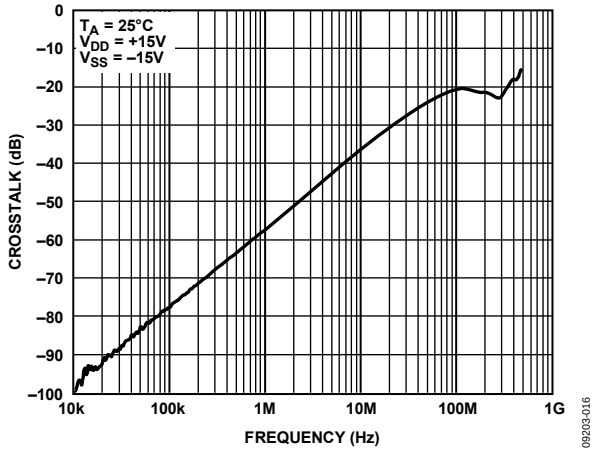


Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

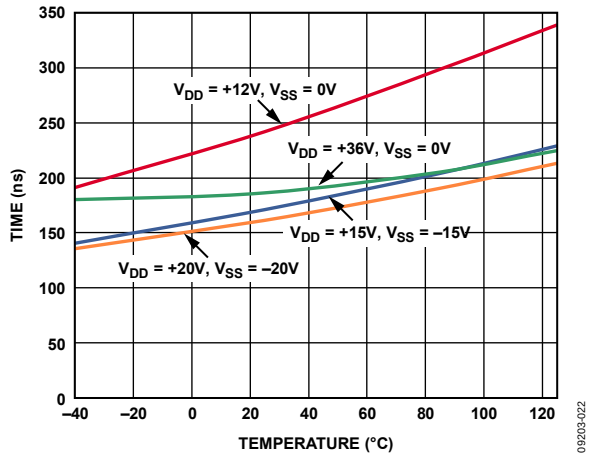


Figure 20. Transition Time vs. Temperature

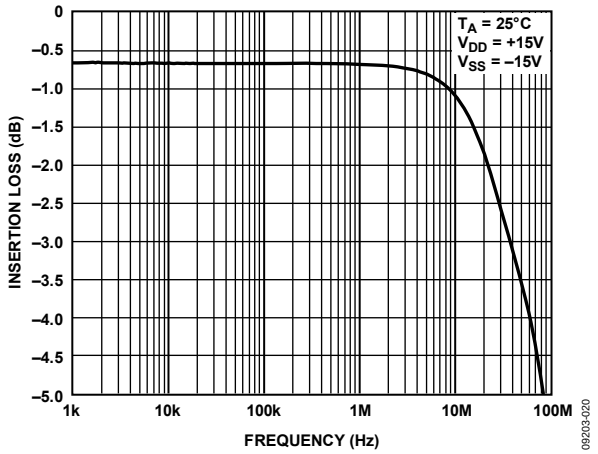


Figure 18. On Response vs. Frequency, ±15 V Dual Supply

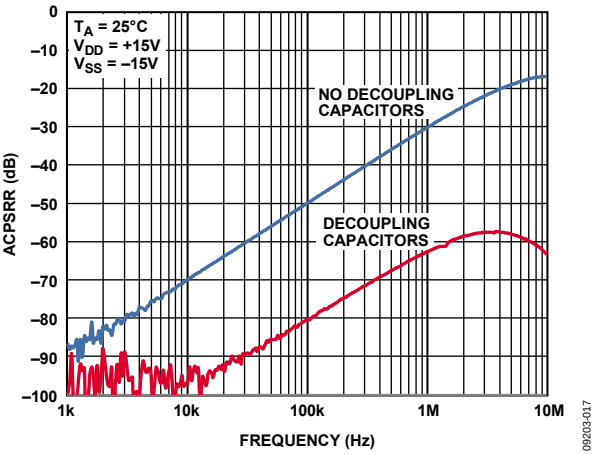


Figure 21. ACPSRR vs. Frequency, ±15 V Dual Supply

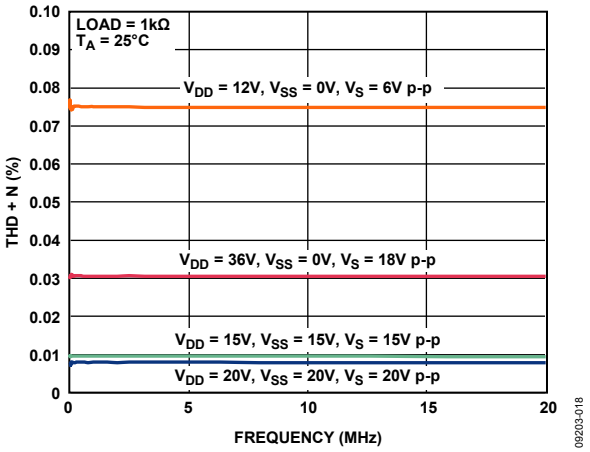


Figure 22. THD + N vs. Frequency, ±15 V Dual Supply

TEST CIRCUITS

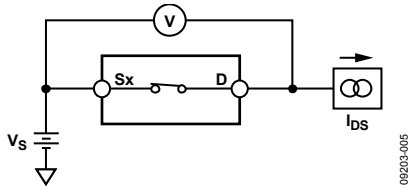


Figure 23. On Resistance

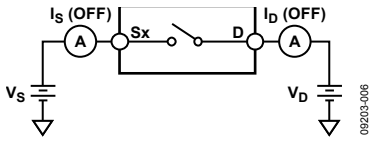


Figure 24. Off Leakage

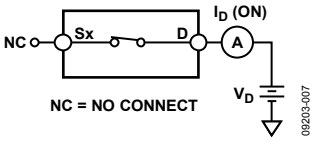


Figure 25. On Leakage

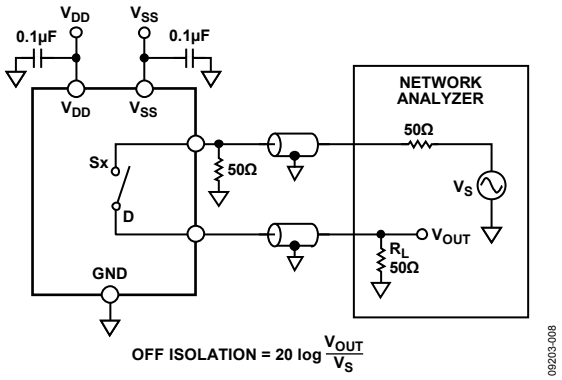


Figure 26. Off Isolation

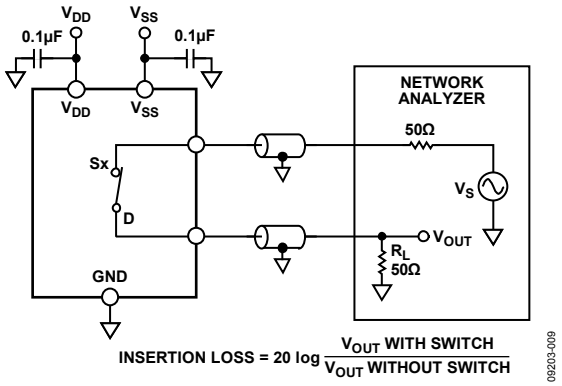


Figure 27. Bandwidth

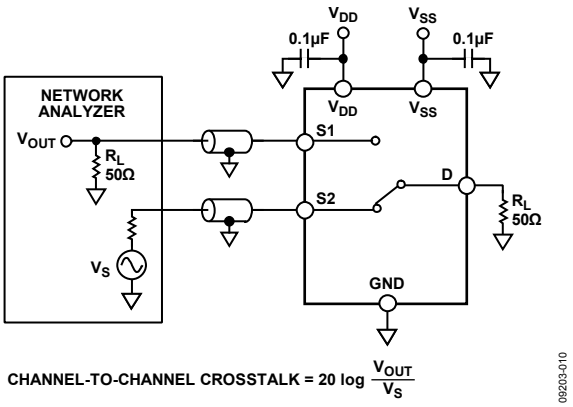


Figure 28. Channel-to-Channel Crosstalk

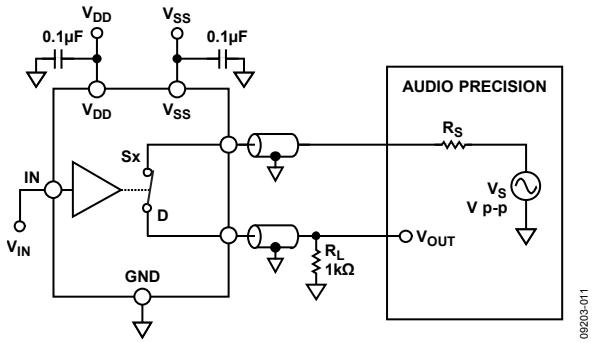


Figure 29. THD + Noise

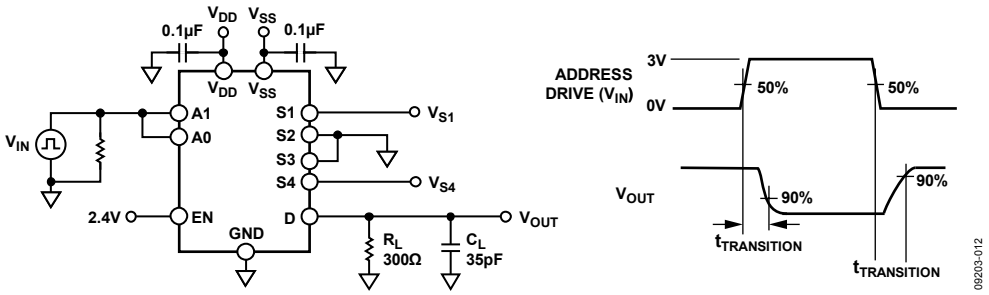


Figure 30. Address to Output Switching Times

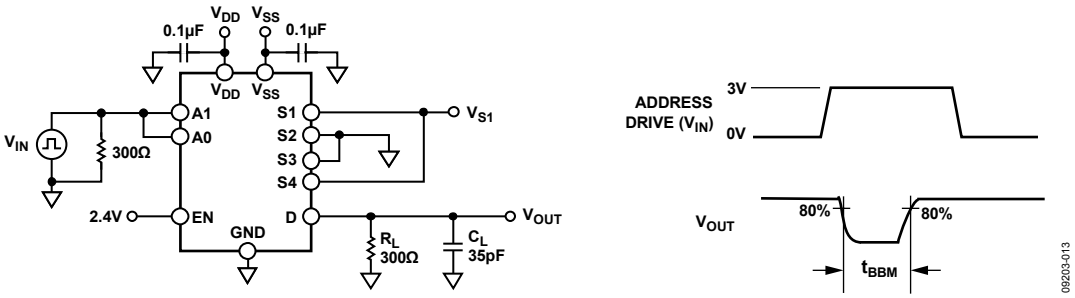


Figure 31. Break-Before-Make Time Delay

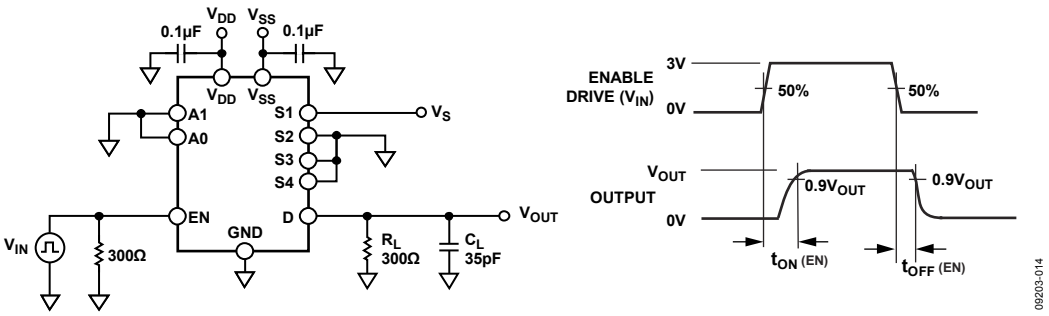


Figure 32. Enable-to-Output Switching Delay

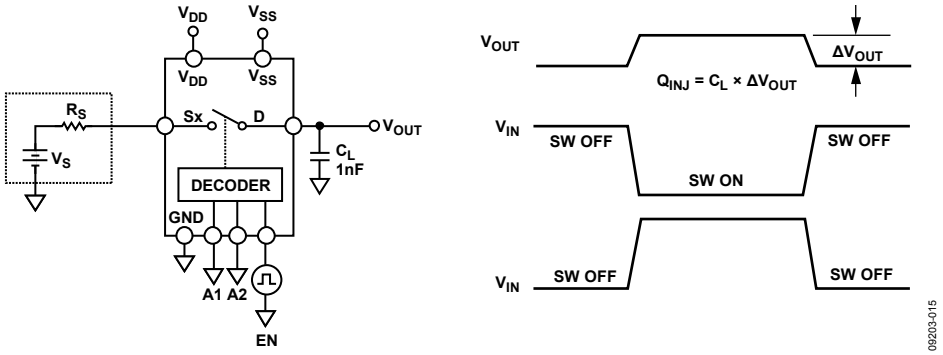


Figure 33. Charge Injection

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$
The delay time between the 50% and 90% points of the digital input and switch-on condition when switching from one address state to another.

t_{ON} (EN)
The delay between applying the digital control input and the output switching on. See Figure 32.

t_{OFF} (EN)
The delay between applying the digital control input and the output switching off.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)
The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the part's ability to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the ADG5404, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

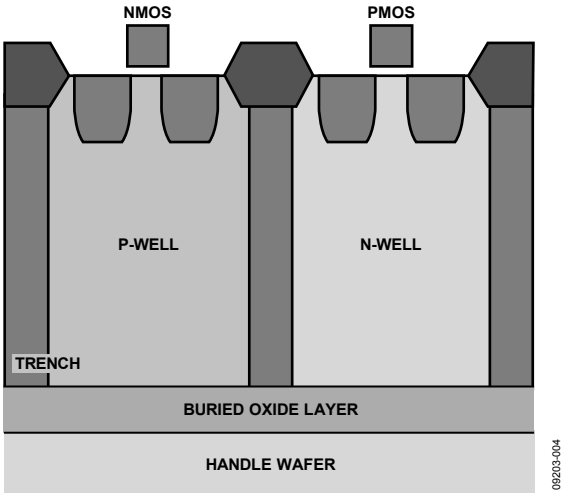
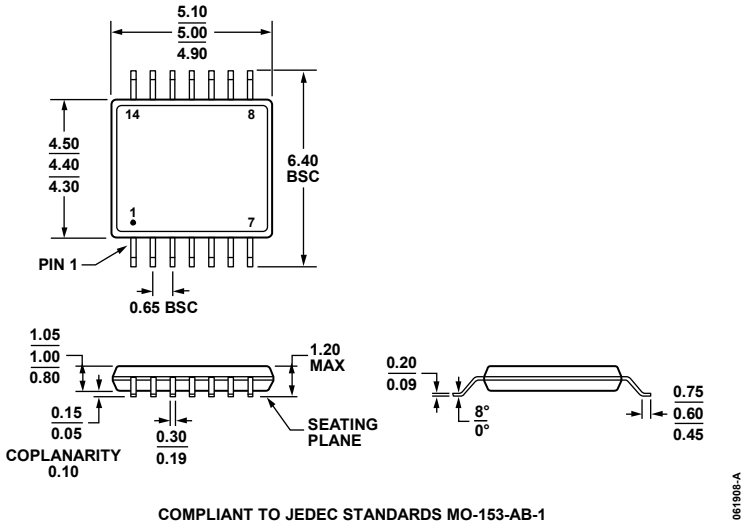


Figure 34. Trench Isolation

APPLICATIONS INFORMATION

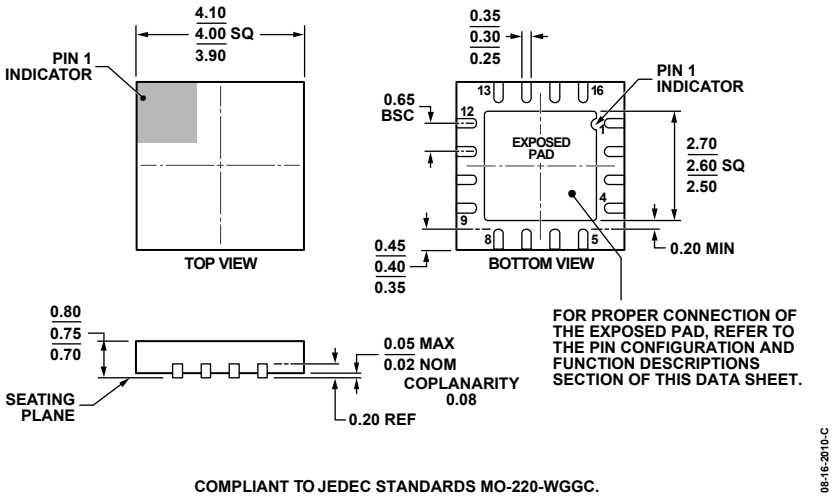
The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5404 high voltage multiplexer allows single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V. The ADG5404, as well as three other ADG54xx family members, ADG5412/ADG5413 and ADG5436, achieve an 8 kV human body model ESD rating that provides a robust solution and eliminates the need for separate protection circuitry designs in some applications.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 35. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5404BRUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5404BRUZ-REEL7	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5404BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17

[1] Z = RoHS Compliant Part.