PIC16(L)F1788/1789 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1788/1789 family devices that you have received conform functionally to the current Device Data Sheet (DS400041675**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1788/1789 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1788/1789 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID	Revision ID (Silicon Revision)	
		B0	B1
PIC16F1788	302Bh	2040h	2041h
PIC16LF1788	302Dh	2040h	2041h
PIC16F1789	302Ah	2040h	2041h
PIC16LF1789	302Ch	2040h	2041h

Note 1: The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.

2: Refer to the *"PIC16(L)F178X Memory Programming Specification"* (DS41457) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revision(1)	
				B0	B1
Comparator	Low-Power mode	1.1	Improper Low-Power mode operation.	X	X
PSMC	Rising Edge Input	2.1	Period and falling edge race condition.	X	X
PSMC	64 MHz Clock	2.2	Failure to operate when PLLEN Configuration bit is set.	X	X
PSMC	Auto-Shutdown	2.3	The PSMC fails to Auto-Restart under certain conditions.	X	X
PSMC	Auto-Shutdown	2.4	The PxASE bit may be stuck high in Auto-Shutdown mode.	X	X
Resets	Low-Power Sleep	3.1	$\overline{\text{MCLR}}$ Reset during Low-Power Sleep will be reported as a POR Reset (PIC16F1788/1789 devices only).	X	X
CPU	BRA/BRW	4.1	An interrupt during execution of BRA or BRW instruction can return an incorrect PC value.	X	
FVR	2x and 4x Gain	5.1	Output tolerance is ± 8%.	X	X
CCP3	Capture	6.1	TTL Input suppresses capture event.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B1**).

1. Module: Comparator

1.1 No Low-Power, No Low-Speed Mode

The comparator operation in Low-Power, Low-Speed mode (CxSP = 0) may not perform properly.

Work around

Use the comparator in High-Power mode.

Affected Silicon Revisions

B0	B1						
X	X						

2. Module: PSMC

2.1 Rising Edge Inhibit

When the period and falling edge sources are from the same asynchronous input, then a race condition may occur where the period is detected before the falling edge. When this occurs, the falling edge properly terminates the cycle but subsequent rising edge inputs are ignored.

Work around

To configure the PSMC for fixed off-time and variable frequency, set the following:

- Period = Asynchronous feedback
- Rising Event = Synchronous @ PSMCxPH = 0
- Falling Event = Synchronous @ PSMCxDC = Off Time
- Output inverted so drive time is from falling event to period event.

Affected Silicon Revisions

B0	B1						
X	X						

2.2 64 MHz Clock

When the Configuration bits select both PLL enabled and INTOSC as the default system clock, then the 64 MHz PSMC clock will not operate after a device Reset until the IRCF[3:0] bits of the OSCCON register are set to '111x'. The IRCF bits can then be set to any desired value and the 64 MHz clock will continue to operate.

Work around

Ensure that the PLLEN bit of the CONFIG2 register is cleared when the FOSC[2:0] bits of the CONFIG1 register select the INTOSC (FOSC[2:0] = 100).

Affected Silicon Revisions

B0	B1						
X	X						

2.3 The PSMC Fails to Auto-Restart Under Certain Conditions

Under the following conditions, the PSMC may fail to Auto-Restart:

- Ambient temperature is above 50°C
- PSMC clock frequency is above 32 MHz
- PSMC Operating mode = Push-pull output
- PSMCxPHH = 0 and PSMCxPHL = 0

Work around

- Select a PSMC clock source that is less than or equal to 32 MHz
- Delay the rising and falling events by increasing the value of the PSMCxPHL and PSMCxDCL by 0x01 or higher value
- When the auto-shutdown source deasserts, toggle the PSMCxEN bit to restart the PSMC output

Affected Silicon Revisions

B0	B1						
X	X						

2.4 The PxASE Bit May be Stuck High in Auto-Shutdown Mode

When Auto-Shutdown is configured for Auto-Restart, the PxASE bit may be stuck high when the Auto-Shutdown source deasserts. When this occurs, the PSMC outputs will get stuck in their shutdown states and will not be able to start.

Work around

When the Auto-Shutdown source deasserts, toggle the PSMCxEN bit to restart the PSMC outputs.

Affected Silicon Revisions

B0	B1						
X	X						

3. Module: Resets

3.1 Low-Power Sleep (PIC16F1788/1789 devices only)

When the device is in Low-Power Sleep (VREGPM = 1 and SLEEP instruction is executed), a MCLR Reset will be reported as a POR Reset:

- $\overline{PD}$ = 1
- $\overline{POR}$ = 0
- RDMCLR = 1

Work around

Use Normal-Power Sleep mode (VREGPM = 0).

Affected Silicon Revisions

B0	B1						
X	X						

4. Module: CPU

4.1 BRA/BRW

If a BRA or BRW instruction is executed concurrently with an interrupt event, the ISR routine can restore the PC to an incorrect value.

Work around

Use the GOTO instruction rather than the BRA or BRW instruction.

Affected Silicon Revisions

B0	B1						
X							

5. Module: FVR

5.1 2x and 4x Gain Selections

The 2x and 4x gain selections are within ± 8% of the nominal value. The 1x output selection is within ± 4% of the nominal, as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

B0	B1						
X	X						

6. Module: CCP3

6.1 CCP3 Capture (PIC16(L)F1789 only)

When the input threshold control for RE0 is configured for TTL, then the CCP3 capture input is ignored.

Work around

Use ST threshold.

Affected Silicon Revisions

B0	B1						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS400041675**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (05/2013)

Initial release of this document.

Rev B Document (07/2013)

Added Silicon Revision B1; Added Module 6; Other minor corrections.

Rev C Document (03/2023)

Updated Table 2; Added sections 2.3 and 2.4; Other minor corrections.

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