



# STS7NF60L

## N-CHANNEL 60V - 0.017 $\Omega$ - 7.5A SO-8 STripFET™ II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS7NF60L	60 V	< 0.0195 $\Omega$	7.5 A

- TYPICAL R<sub>DS(on)</sub> = 0.017  $\Omega$
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

### DESCRIPTION

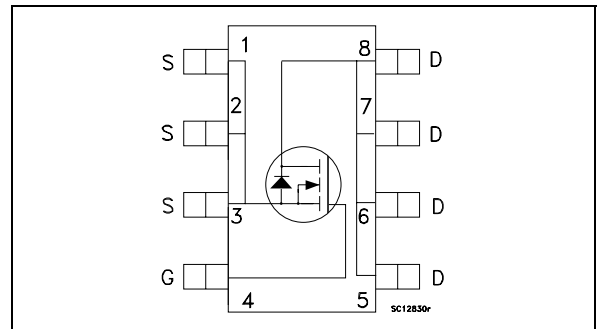
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	60	V
V <sub>GS</sub>	Gate- source Voltage	$\pm 16$	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	7.5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.7	A
I <sub>DM</sub> (*)	Drain Current (pulsed)	30	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	350	mJ

(\*) Pulse width limited by safe operating area.

(1) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 7.5 A V<sub>DD</sub> = 30 V

## STS7NF60L

### THERMAL DATA

Rthj-amb(#)	Thermal Resistance Junction-ambient	Max	50	°C/W
T <sub>j</sub>	Maximum Operating Junction Temperature		150	°C
T <sub>stg</sub>	Storage Temperature		-55 to 150	°C

(#) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu and t ≤ 10 sec.

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16 V			±100	nA

#### ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 3.5 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 3.5 A		0.017 0.019	0.0195 0.0215	Ω Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V I <sub>D</sub> = 3.5 A		13		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1700 300 100		pF pF pF

**ELECTRICAL CHARACTERISTICS** (continued)

SWITCHING ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		15 27		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}$ $I_D = 7.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 2)		25 4.5 7	34	nC nC nC

SWITCHING OFF (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		47 20		ns ns

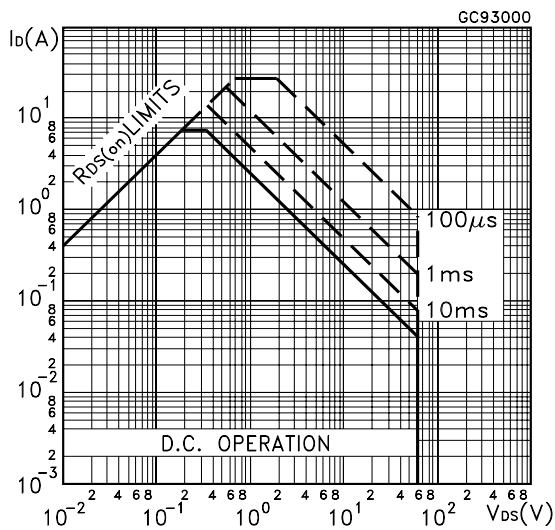
SOURCE DRAIN DIODE (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				7.5 30	A A
$V_{SD}$	Forward On Voltage	$I_{SD} = 7.5\text{ A}$ $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7.5\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		55 110 3.9		ns nC A

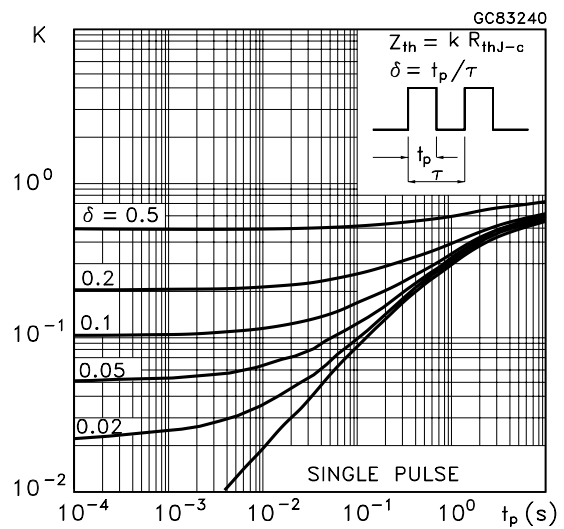
(\*) Pulse width  $\leq 300\ \mu\text{s}$ , duty cycle 1.5 %.

(●) Pulse width limited by safe operating area.

Safe Operating Area

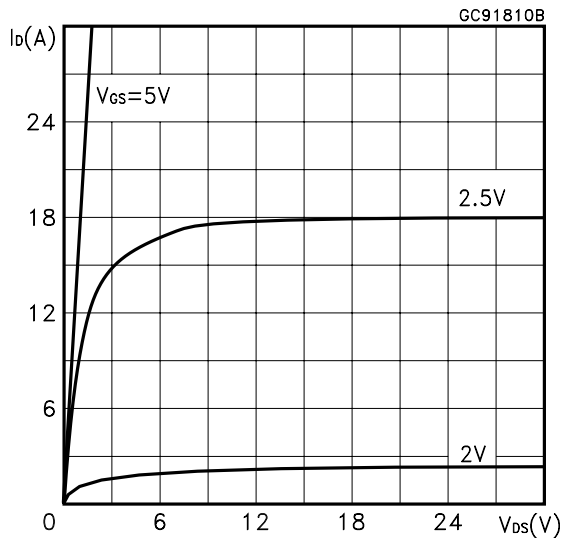


Thermal Impedance

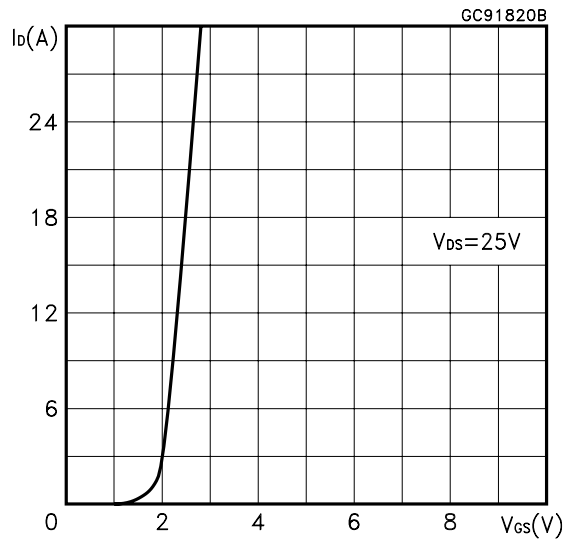


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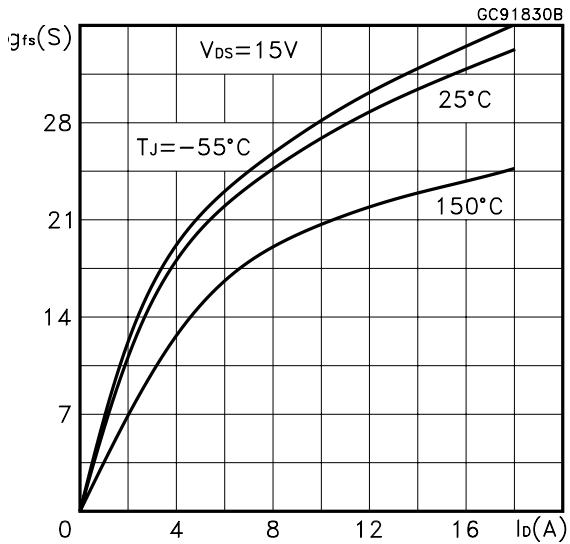
Output Characteristics



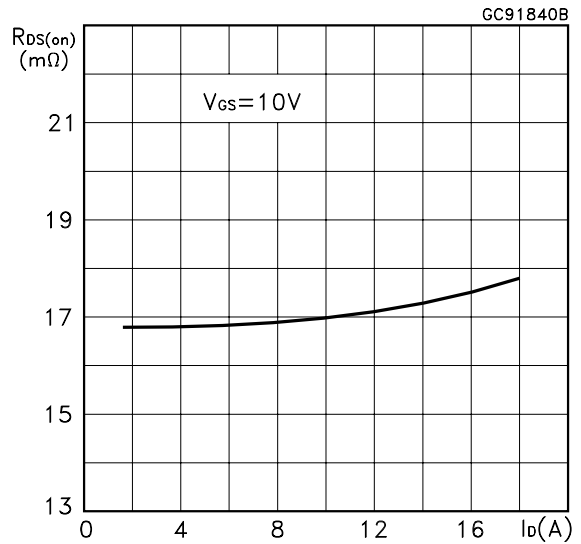
Transfer Characteristics



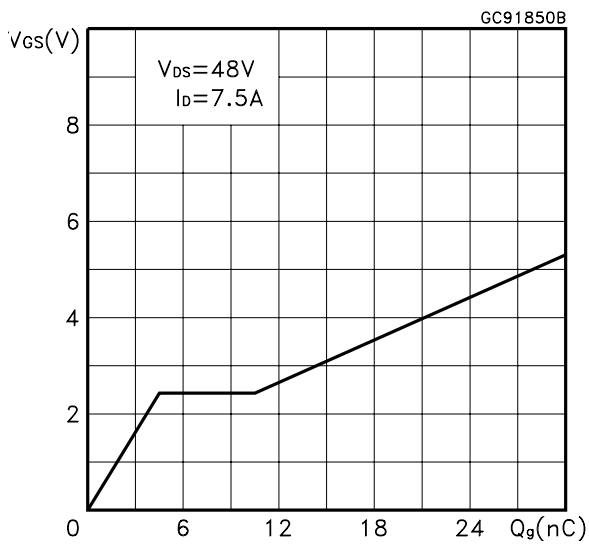
Transconductance



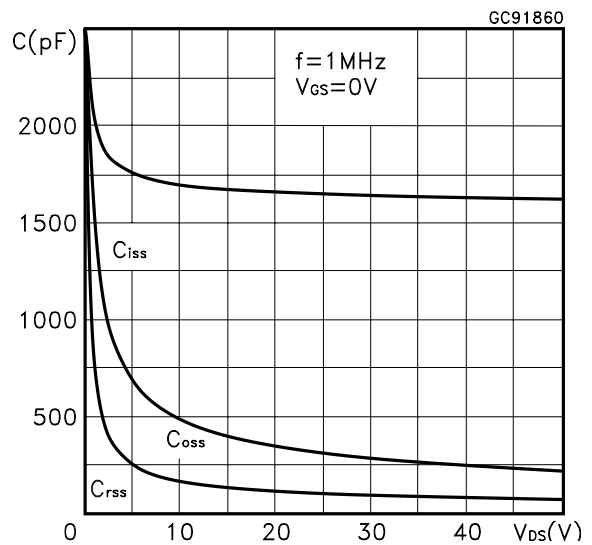
Static Drain-source On Resistance



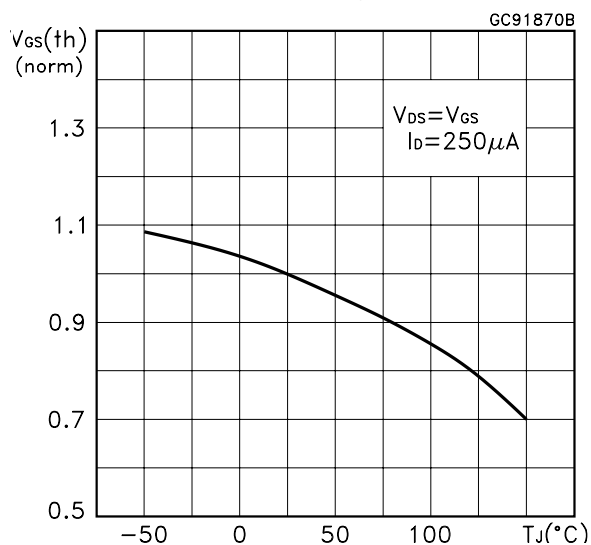
Gate Charge vs Gate-source Voltage



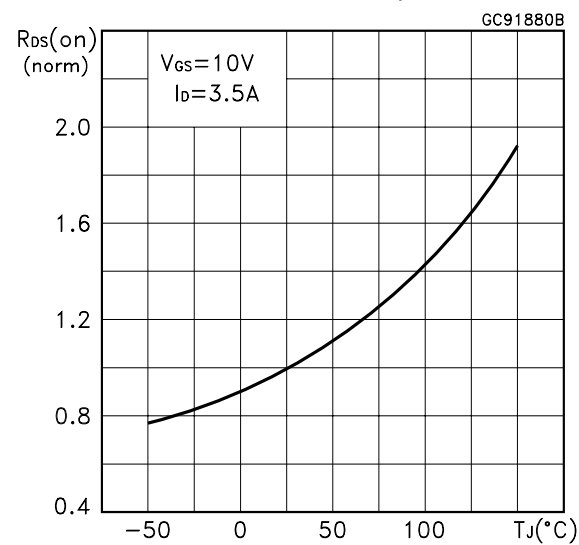
Capacitance Variations



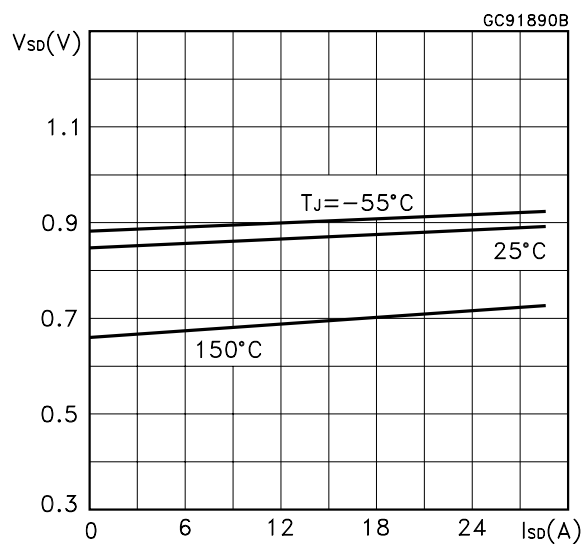
Normalized Gate Threshold Voltage vs Temperature



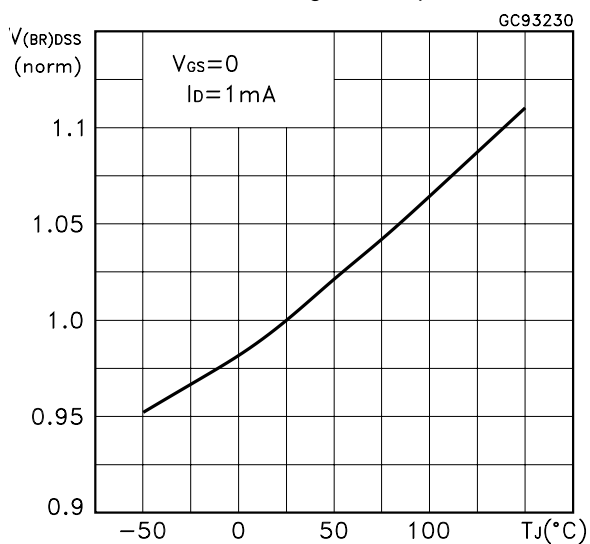
Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature



**Fig. 1: Unclamped Inductive Load Test Circuit**



**Fig. 2: Unclamped Inductive Waveform**



**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**



**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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