2 A/1.25 A, 1.2 MHz, Synchronous, Step-Down DC-to-DC Regulators

Data Sheet

ADP2119/ADP2120

FEATURES

- Continuous output current
  - ADP2119: 2 A
  - ADP2120: 1.25 A
- 145 mΩ and 70 mΩ integrated MOSFETs
- Input voltage range from 2.3 V to 5.5 V
- Output voltage from 0.6 V to V_{IN}
- ±1.5% output accuracy
- 1.2 MHz fixed switching frequency
- Synchronizable between 1 MHz and 2 MHz
- Selectable PWM or PFM mode operation
- Current mode architecture
- Precision threshold enable input
- Power-good flag
- Voltage tracking
- Integrated soft start
- Internal compensation
- Startup with precharged output
- UVLO, OVP, OCP, and thermal shutdown
- 10-lead, 3 mm × 3 mm LFCSP_WD package
- Supported by ADIsimPower™ design tool

APPLICATIONS

- Point of load conversion
- Communications and networking equipment
- Industrial and instrumentation
- Consumer electronics
- Medical applications

TYPICAL APPLICATION CIRCUIT

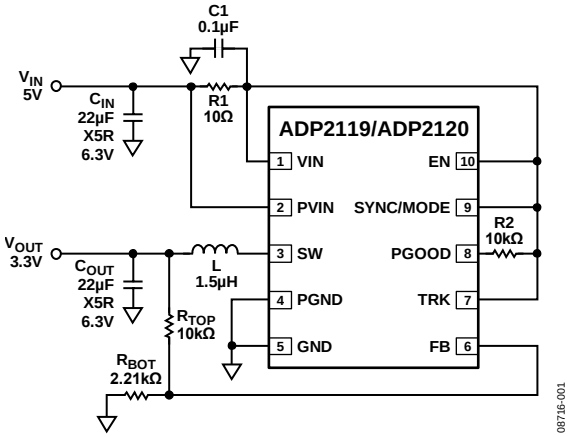

Figure 1.

GENERAL DESCRIPTION

The ADP2119/ADP2120 are low quiescent current, synchronous, step-down dc-to-dc regulators in a compact 3 mm × 3 mm LFCSP_WD package. Both devices use a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. Under light load conditions, they can be configured to operate in a pulse frequency modulation (PFM) mode, which reduces switching frequency to save power.

The ADP2119/ADP2120 support input voltages from 2.3 V to 5.5 V. The output voltage can be adjusted from 0.6 V up to the input voltage (V_{IN}) for the adjustable version, whereas the fixed output version is available in preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V. The ADP2119/ADP2120 require minimal external parts and provide a high efficiency solution with their integrated power switches, synchronous rectifiers, and internal compensation. Each IC draws less than 2 µA current from the input source when it is disabled. Other key features include undervoltage lockout (UVLO), integrated soft start to limit inrush current at startup, overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).

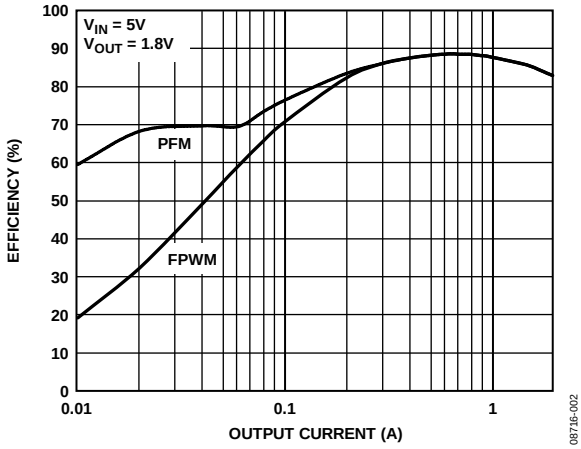

Figure 2. ADP2119 Efficiency vs. Output Current

Rev. A

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6/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{PVIN} = 3.3 V, EN = VIN, SYNC/MODE = VIN at T_J = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIN and PVIN						
VIN Voltage Range	V_{IN}		2.3		5.5	V
PVIN Voltage Range	V_{PVIN}		2.3		5.5	V
Quiescent Current	I_{VIN}	No switching, SYNC/MODE = GND		150	200	µA
		Switching, no load, SYNC/MODE = VIN		680	900	µA
Shutdown Current	I_{SHDN}	V_{IN} = V_{PVIN} = 5.5 V, EN = GND		0.3	2	µA
VIN Undervoltage Lockout Threshold	UVLO	V_{IN} rising		2.2	2.3	V
		V_{IN} falling	2	2.1		V
OUTPUT CHARACTERISTICS						
Load Regulation[1]		ADP2119, I_O = 0 A to 2 A		0.08		%/A
Load Regulation[2]		ADP2120, I_O = 0 A to 1.25 A		0.08		%/A
Line Regulation[1]		ADP2119, I_O = 1 A		0.05		%/V
Line Regulation[2]		ADP2120, I_O = 1 A		0.05		%/V
FB						
FB Regulation Voltage	V_{FB}	V_{IN} = 2.3 V to 5.5 V	0.591	0.6	0.609	V
FB Bias Current	I_{FB}	V_{IN} = 2.3 V to 5.5 V		0.01	0.1	µA
SW						
High-Side On Resistance[3]		V_{IN} = V_{PVIN} = 3.3 V, I_{SW} = 200 mA		145	190	mΩ
Low-Side On Resistance[3]		V_{IN} = V_{PVIN} = 3.3 V, I_{SW} = 200 mA		70	100	mΩ
SW Peak Current Limit		High-side switch, V_{IN} = V_{PVIN} = 3.3 V (ADP2119)	2.5	3	3.5	A
		High-side switch, V_{IN} = V_{PVIN} = 3.3 V (ADP2120)	1.6	2	2.4	A
SW Maximum Duty Cycle		V_{IN} = V_{PVIN} = 5.5 V, full frequency			100	%
SW Minimum On Time[4]		V_{IN} = V_{PVIN} = 5.5 V, full frequency		100		ns
TRK						
TRK Input Voltage Range			0		600	mV
TRK-to-FB Offset Voltage		TRK = 0 mV to 500 mV	−15		+15	mV
TRK Input Bias Current					100	nA
FREQUENCY						
Oscillator Frequency	f_S		1.02	1.2	1.38	MHz
SYNC/MODE						
Synchronization Range			1		2	MHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input High Voltage			1.3			V
SYNC Input Low Voltage					0.4	V
INTEGRATED SOFT START						
Soft Start Time		All switching frequencies		1024		Clock cycles
		f_S = 1.2 MHz		853		µs
PGOOD						
Power-Good Range		FB rising threshold	105	110	115	%
		FB rising hysteresis		2.5		%
		FB falling threshold	85	90	95	%
		FB falling hysteresis		2.5		%
Power-Good Deglitch Time		From FB to PGOOD		16		Clock cycles
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1 mA		150	200	mV
PGOOD Output Low Resistor		I_{PGOOD} = 1 mA		150	200	Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN						
EN Input Rising Threshold		V_{IN} = 2.3 V to 5.5 V	1.12	1.2	1.28	V
EN Input Hysteresis		V_{IN} = 2.3 V to 5.5 V		100		mV
EN Pull-Down Resistor				1		MΩ
THERMAL						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

[1] Specified by the circuit in Figure 54.
[2] Specified by the circuit in Figure 58.
[3] Pin-to-pin measurements.
[4] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, PVIN	−0.3 V to +6 V
SW	−0.3 V to +6 V
FB, SYNC/MODE, EN, TRK, PGOOD	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead LFCSP_WD	40	°C/W

BOUNDARY CONDITION

θ_{JA} is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

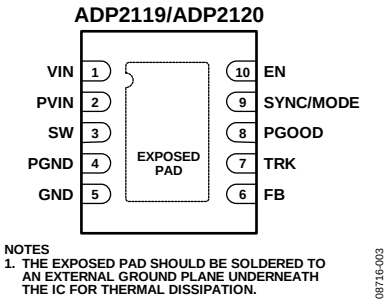

Figure 3. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Bias Voltage Input Pin. Connect a bypass capacitor (0.1 µF minimum) between this pin and GND and a small (10 Ω) resistor between this pin and PVIN.
2	PVIN	Power Input Pin. Connect this pin to the input power source. Connect a bypass capacitor between this pin and PGND.
3	SW	Switch Node Output. Connect this pin to the output inductor.
4	PGND	Power Ground. Connect this pin to the power ground plane and to the high current return for the power MOSFET.
5	GND	Analog Ground. Connect this pin to the ground plane.
6	FB	Feedback Voltage Sense Input. Connect this pin to a resistor divider from V_{OUT}. For the fixed output version, connect to V_{OUT} directly.
7	TRK	Tracking Input. To track a master voltage, drive TRK from a resistor divider from the master voltage. If the tracking function is not used, connect TRK to VIN.
8	PGOOD	Power-Good Output (Open Drain). Connect this pin to a resistor to any pull-up voltage < 5.5 V.
9	SYNC/MODE	Synchronization Input (SYNC). Connect this pin to an external clock between 1 MHz and 2 MHz to synchronize the switching frequency to the external clock (see the Oscillator and Synchronization section for details). FPWM/PFM Selection (MODE). When this pin is connected to VIN, the PFM mode is disabled and the part works in continuous conduction mode (CCM) only. When this pin is connected to ground, the PFM mode is enabled and becomes active at light loads.
10	EN	Precision Threshold Enable Input Pin. An external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to VIN. This pin has a 1 MΩ pull-down resistor to GND.
EPAD	Exposed Pad	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{PVIN} = 5 V, V_{OUT} = 1.2 V, L = 1.5 µH, C_{IN} = 22 µF, C_{OUT} = 2 × 22 µF, unless otherwise noted.

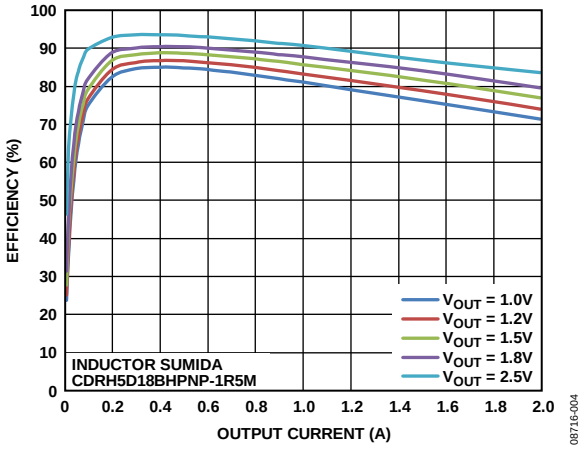

Figure 4. Efficiency (ADP2119, V_{IN} = 3.3 V, FPWM) vs. Output Current

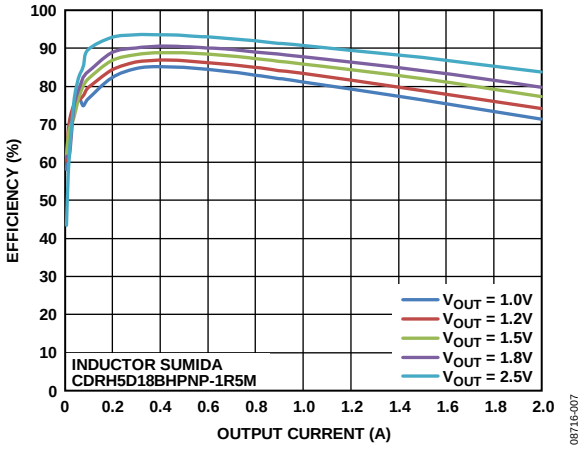

Figure 7. Efficiency (ADP2119, V_{IN} = 3.3 V, PFM) vs. Output Current

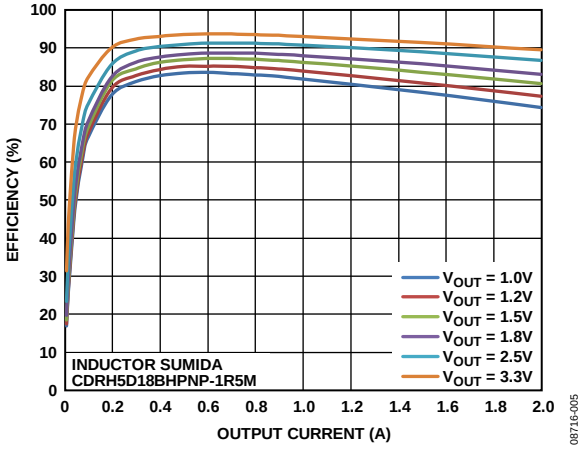

Figure 5. Efficiency (ADP2119, V_{IN} = 5 V, FPWM) vs. Output Current

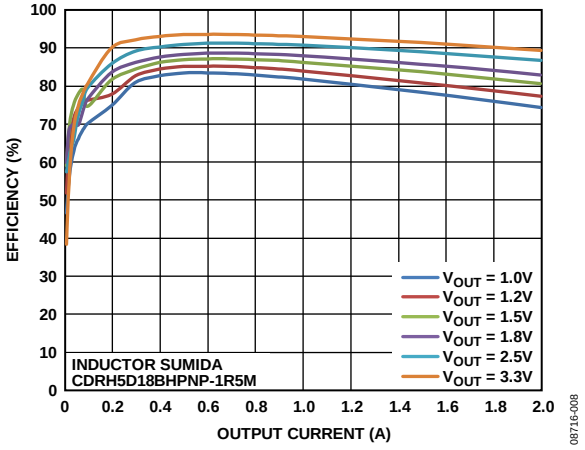

Figure 8. Efficiency (ADP2119, V_{IN} = 5 V, PFM) vs. Output Current

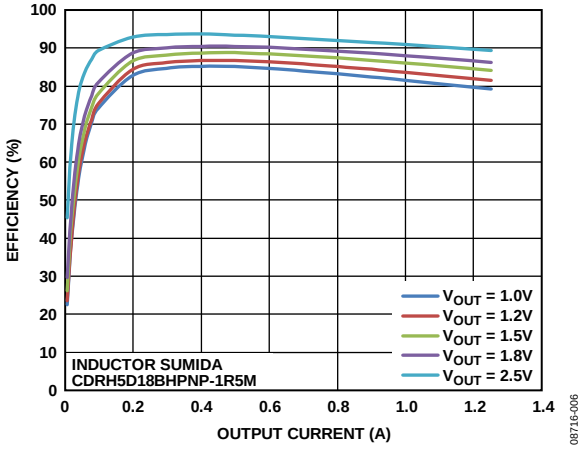

Figure 6. Efficiency (ADP2120, V_{IN} = 3.3 V, FPWM) vs. Output Current

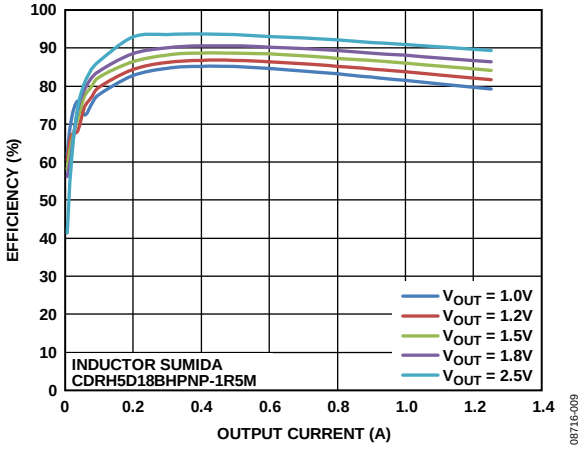

Figure 9. Efficiency (ADP2120, V_{IN} = 3.3 V, PFM) vs. Output Current

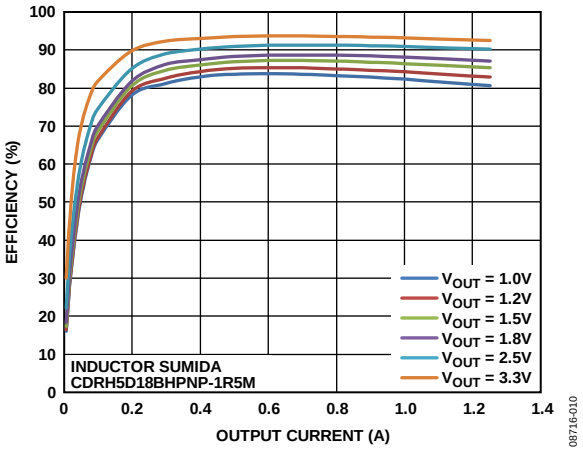

Figure 10. Efficiency (ADP2120, V_{IN} = 5 V, FPWM) vs. Output Current

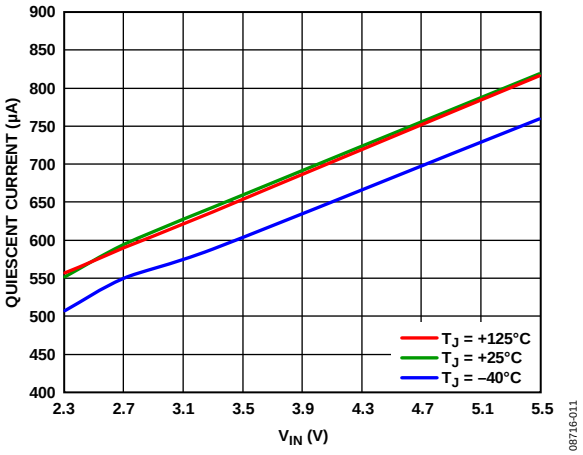

Figure 11. Quiescent Current vs. V_{IN} (Switching)

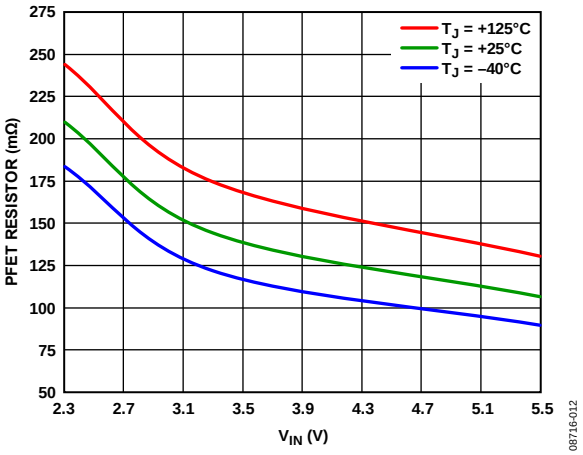

Figure 12. PFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

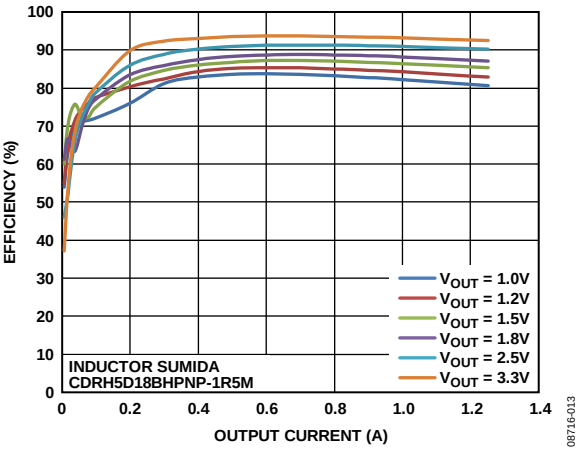

Figure 13. Efficiency (ADP2120, V_{IN} = 5 V, PFM) vs. Output Current

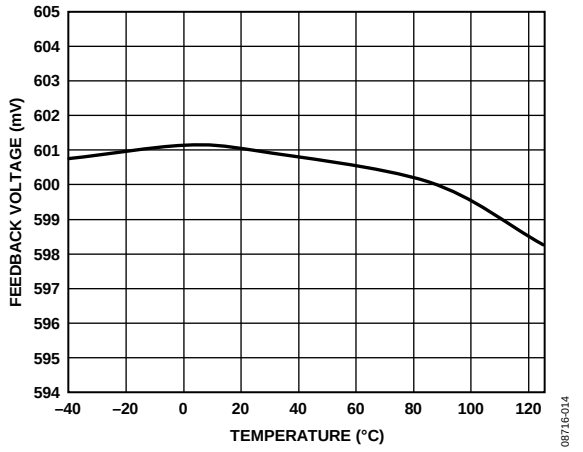

Figure 14. Feedback Voltage vs. Temperature (V_{IN} = 3.3 V)

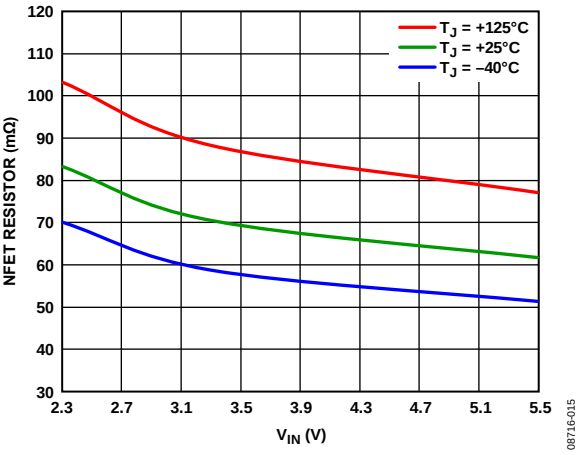

Figure 15. NFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

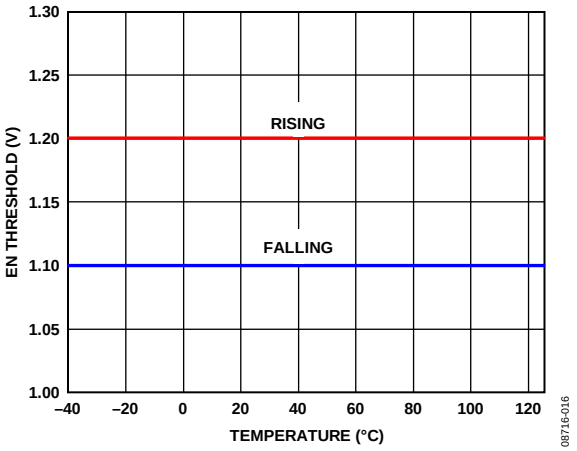

Figure 16. EN Threshold vs. Temperature

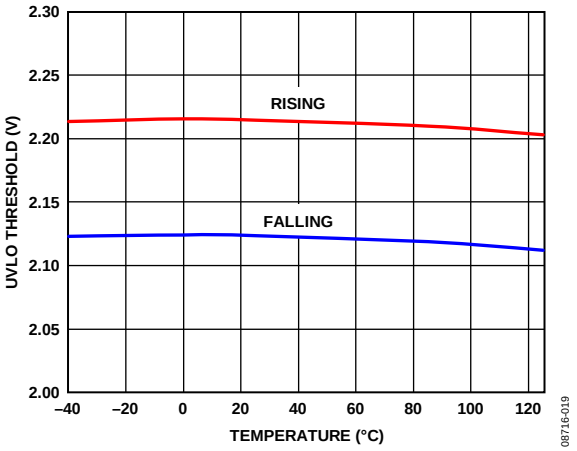

Figure 19. UVLO Threshold vs. Temperature (V_{IN} = 3.3 V)

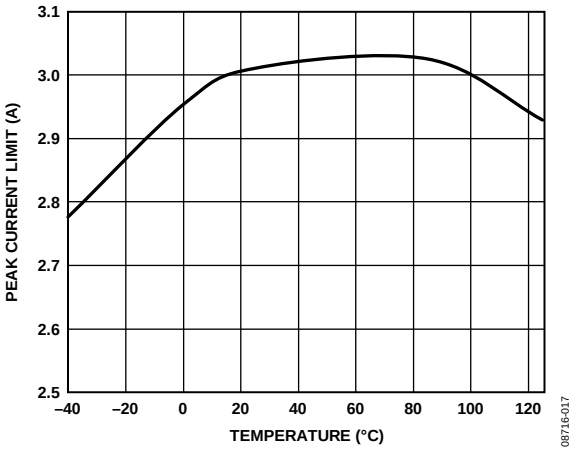

Figure 17. Peak Current Limit vs. Temperature (ADP2119, V_{IN} = 3.3 V)

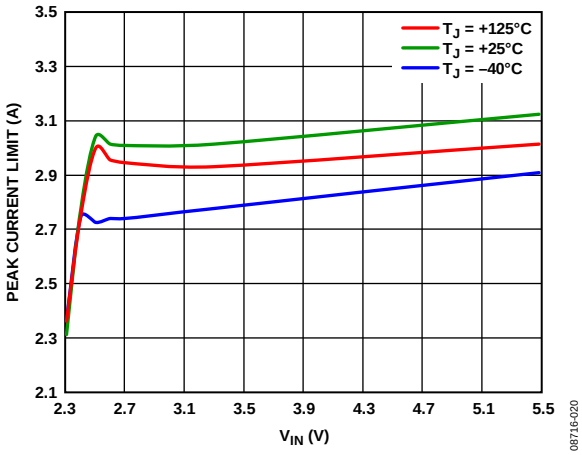

Figure 20. Peak Current Limit vs. V_{IN} (ADP2119)

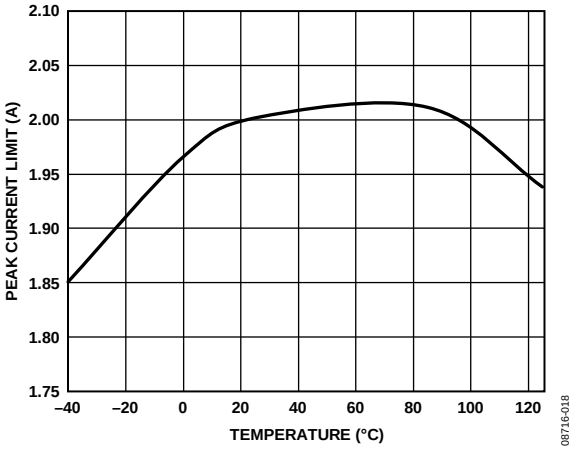

Figure 18. Peak Current Limit vs. Temperature (ADP2120, V_{IN} = 3.3 V)

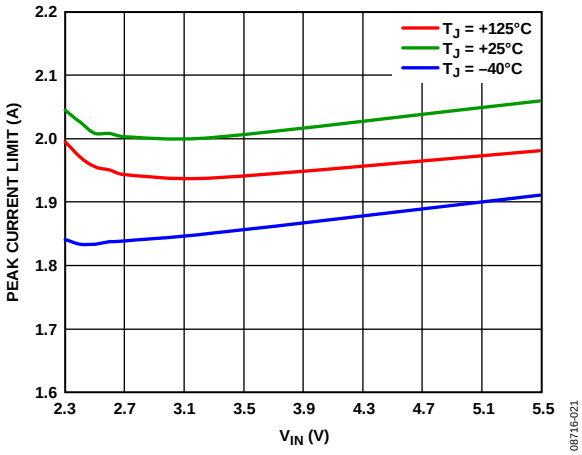

Figure 21. Peak Current Limit vs. V_{IN} (ADP2120)

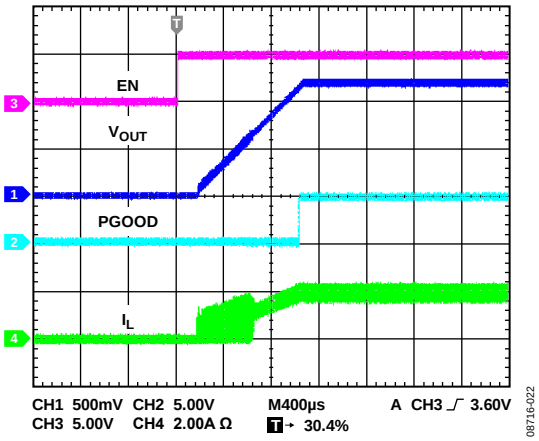

Figure 22. Soft Start with Full Load (ADP2119, V_{IN} = 5 V)

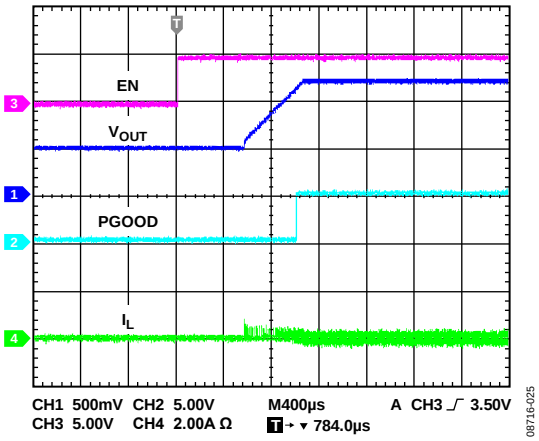

Figure 25. Soft Start with Precharged Output (ADP2119, V_{IN} = 5 V)

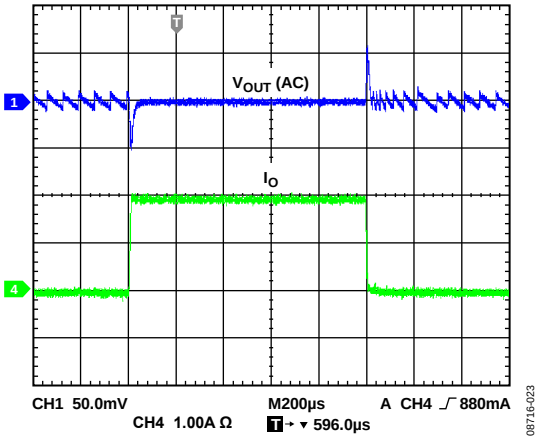

Figure 23. Load Transient (ADP2119, PFM, V_{IN} = 5 V)

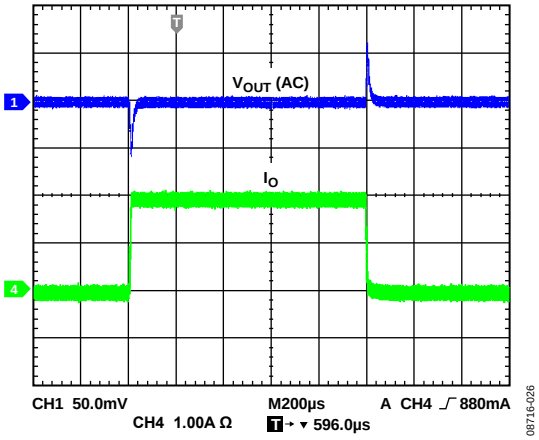

Figure 26. Load Transient (ADP2119, FPWM, V_{IN} = 5 V)

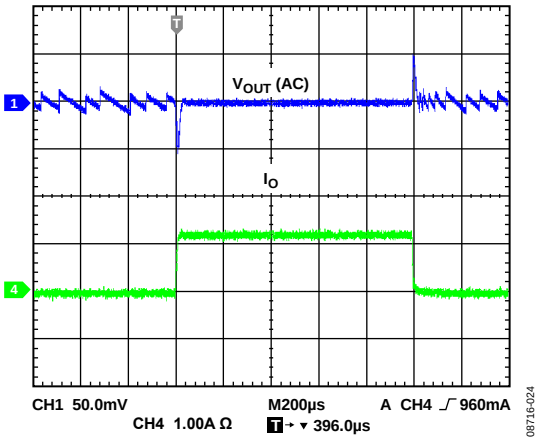

Figure 24. Load Transient (ADP2120, PFM, V_{IN} = 5 V)

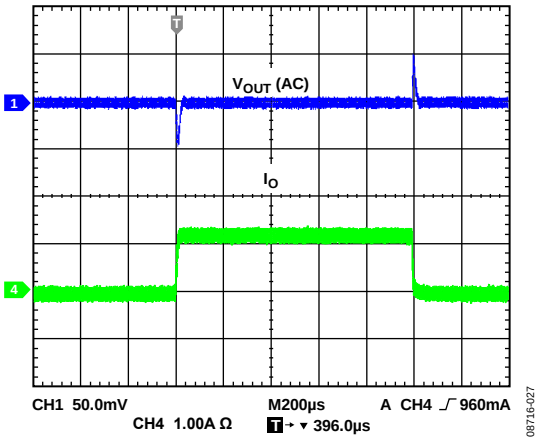

Figure 27. Load Transient (ADP2120, FPWM, V_{IN} = 5 V)

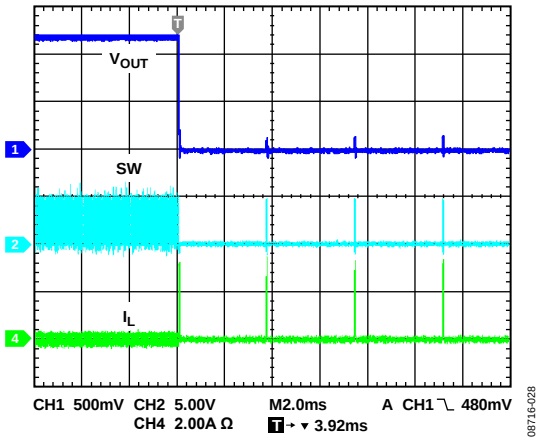

Figure 28. Output Short (ADP2119)

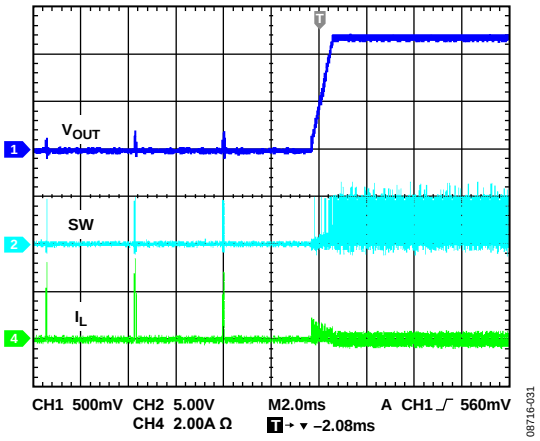

Figure 31. Output Short Recovery (ADP2119)

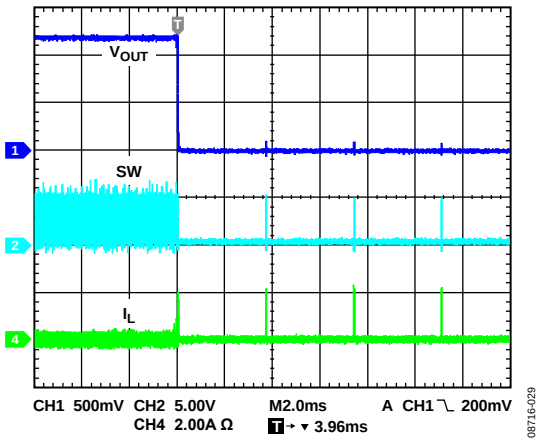

Figure 29. Output Short (ADP2120)

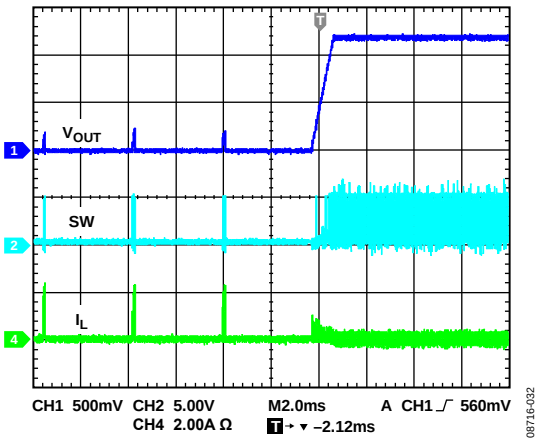

Figure 32. Output Short Recovery (ADP2120)

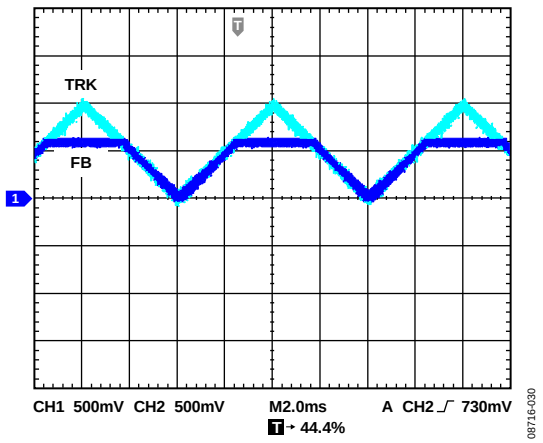

Figure 30. Tracking Function

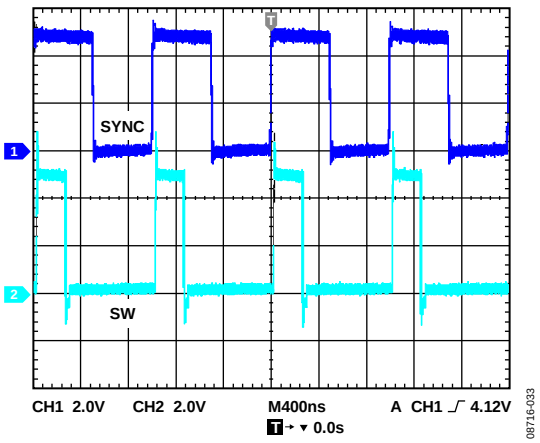

Figure 33. Synchronized to 1 MHz

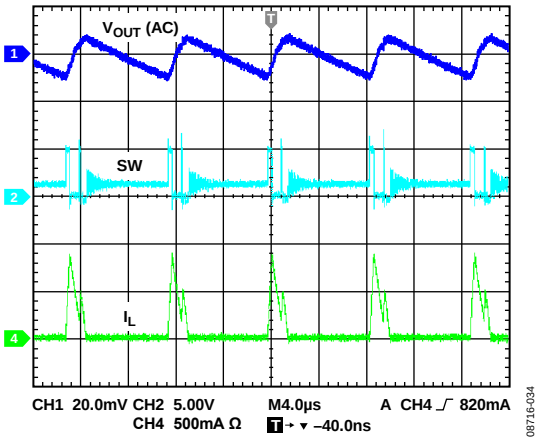

Figure 34. PFM Mode

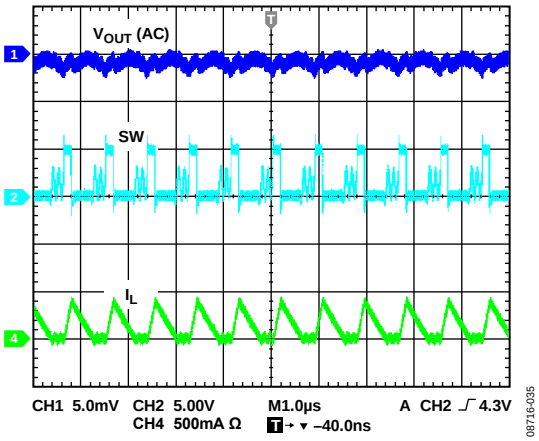

Figure 35. Discontinuous Conduction Mode (DCM)

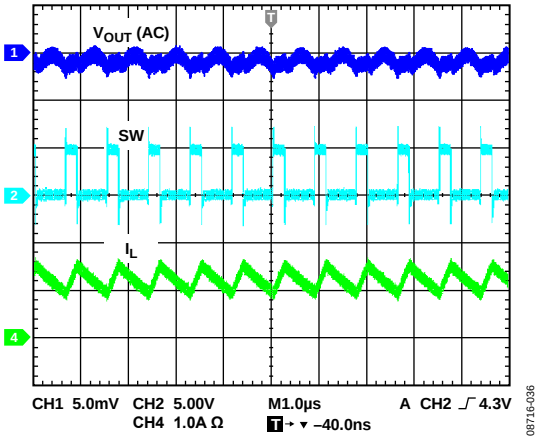

Figure 36. Continuous Conduction Mode (CCM)

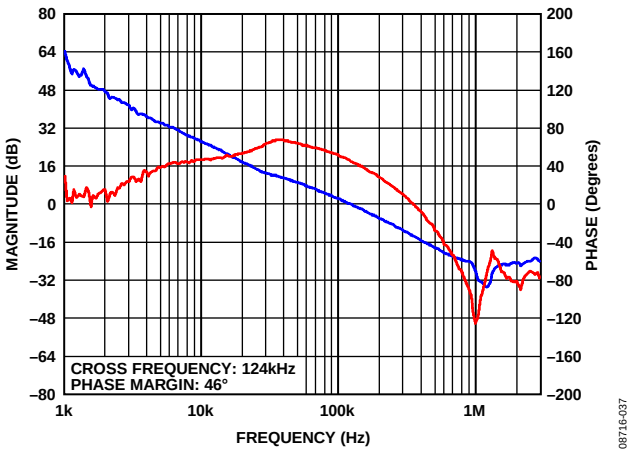

Figure 37. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.0 V, I_O = 2 A, L = 1 µH, C_{OUT} = 2 × 22 µF

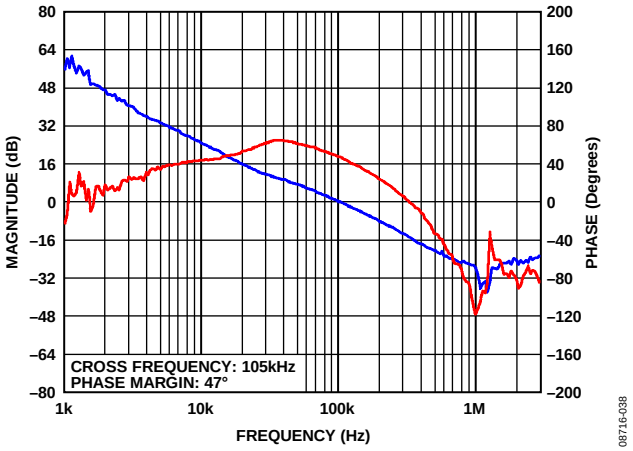

Figure 38. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.2 V, I_O = 2 A, L = 1.5 µH, C_{OUT} = 2 × 22 µF

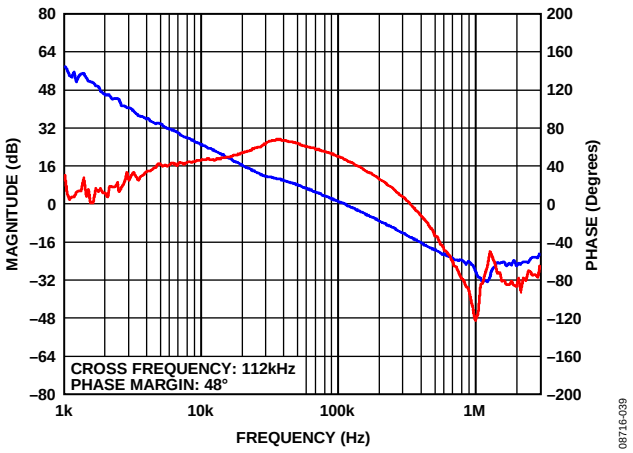

Figure 39. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.5 V, I_O = 2 A, L = 1.5 µH, C_{OUT} = 22 µF + 10 µF

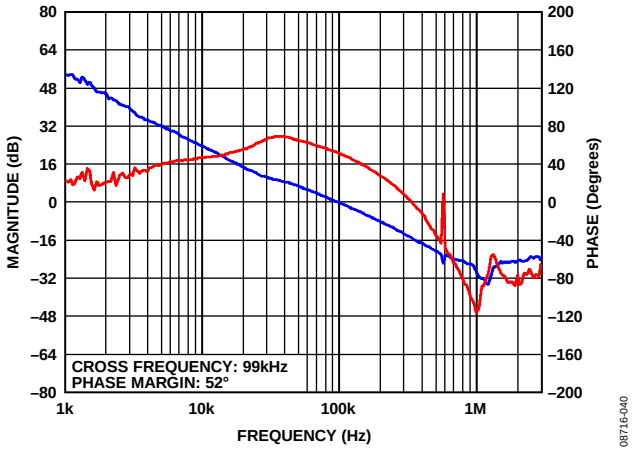

Figure 40. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.8 V, I_O = 2 A, L = 1.5 µH, C_{OUT} = 22 µF + 10 µF

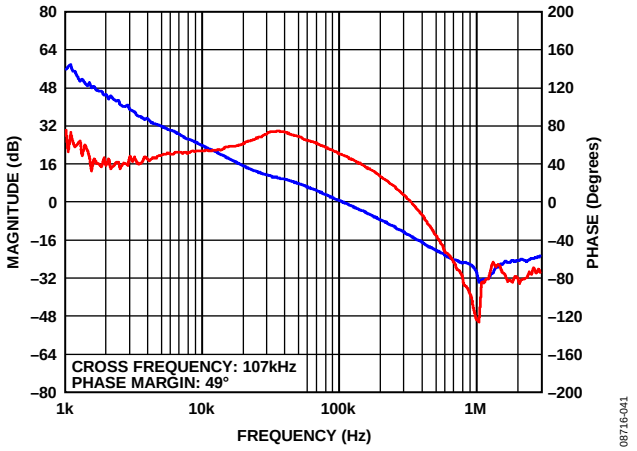

Figure 41. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 2.5 V, I_O = 2 A, L = 1.5 µH, C_{OUT} = 22 µF

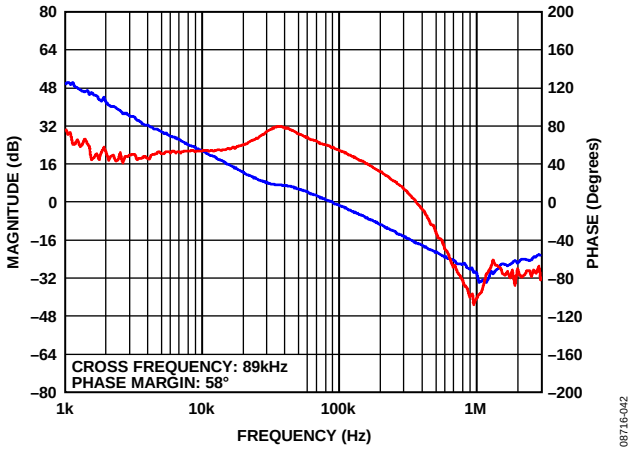

Figure 42. ADP2119 Bode Plot at V_{IN} = 5 V, V_{OUT} = 3.3 V, I_O = 2 A, L = 1.5 µH, C_{OUT} = 22 µF

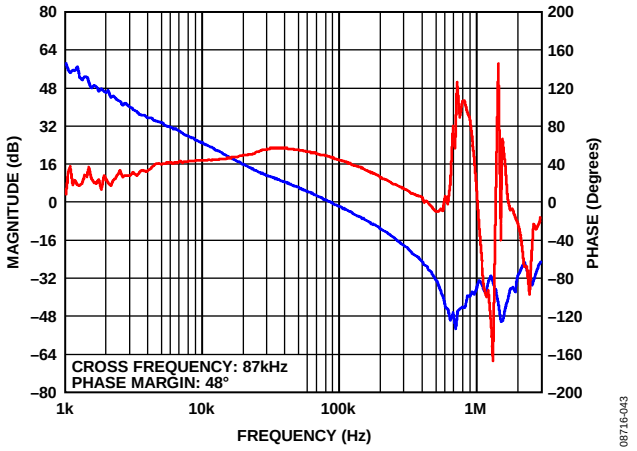

Figure 43. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.0 V, I_O = 1.25 A, L = 1.5 µH, C_{OUT} = 22 µF + 10 µF

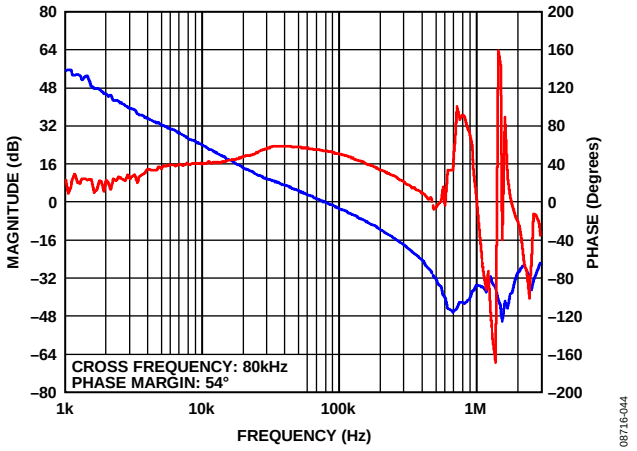

Figure 44. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.2 V, I_O = 1.25 A, L = 1.5 µH, C_{OUT} = 22 µF + 10 µF

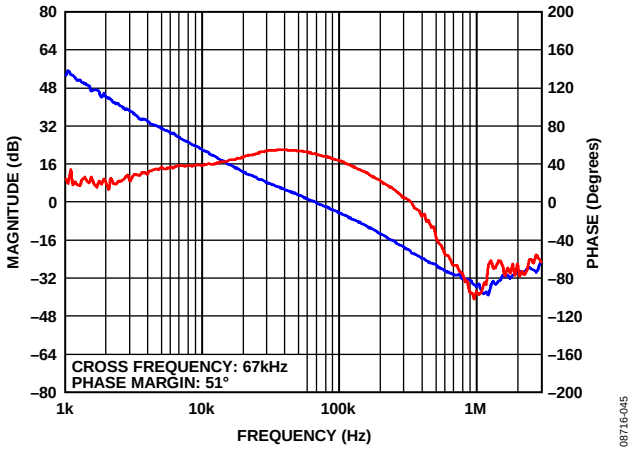

Figure 45. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.5 V, I_O = 1.25 A, L = 2.2 µH, C_{OUT} = 22 µF + 10 µF

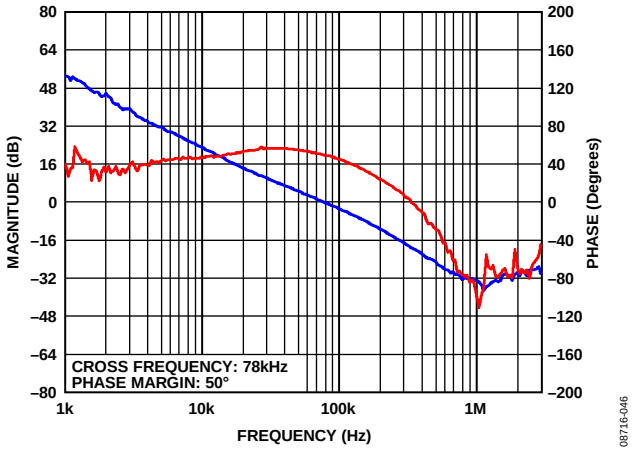

Figure 46. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.8 V, I_O = 1.25 A, L = 2.2 µH, C_{OUT} = 2 × 10 µF

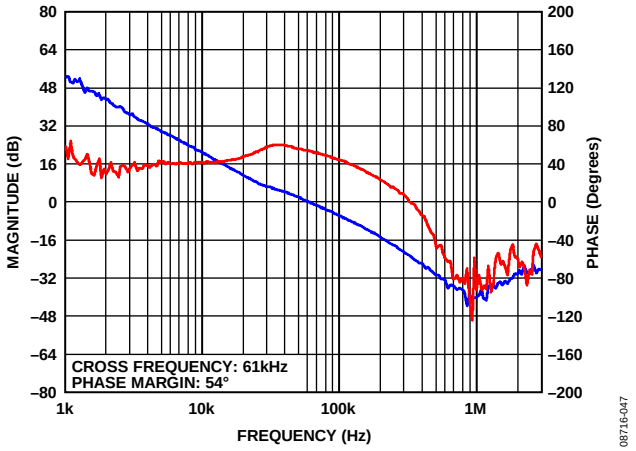

Figure 47. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 2.5 V, I_O = 1.25 A, L = 2.2 µH, C_{OUT} = 2 × 10 µF

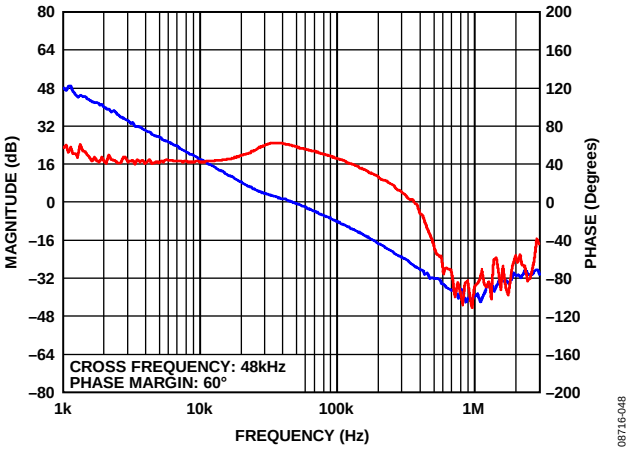

Figure 48. ADP2120 Bode Plot at V_{IN} = 5 V, V_{OUT} = 3.3 V, I_O = 1.25 A, L = 2.2 µH, C_{OUT} = 2 × 10 µF

FUNCTIONAL BLOCK DIAGRAM

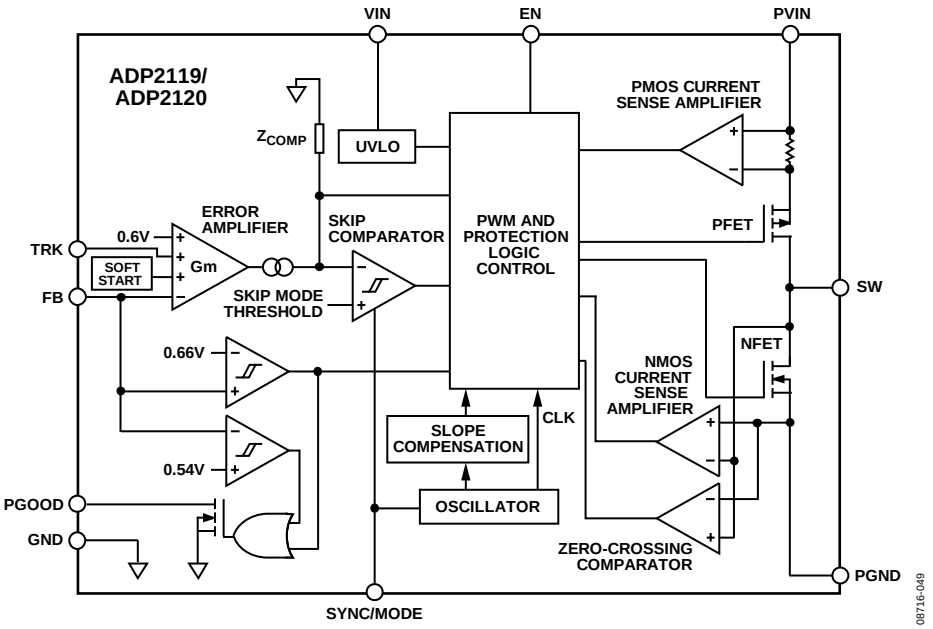

Figure 49. Functional Block Diagram

THEORY OF OPERATION

The ADP2119/ADP2120 are step-down, dc-to-dc regulators that use a fixed frequency, peak current mode architecture with integrated high-side switch and low-side synchronous rectifier. The high switching frequency and tiny 10-lead, 3 mm × 3 mm LFCSP_WD package provide a small step-down dc-to-dc regulator solution. The integrated high-side switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) yield high efficiency at medium-to-full loads while light load efficiency is improved using the PFM mode.

The ADP2119/ADP2120 support input voltages from 2.3 V to 5.5 V and regulate the output voltage down to 0.6 V. The ADP2119/ADP2120 are also available with preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

CONTROL SCHEME

The ADP2119/ADP2120 use a fixed frequency, peak current mode PWM control architecture and operate in PWM mode for medium-to-full loads but shift to PFM mode (if enabled) at light loads to maintain high efficiency. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage. When operating in PFM mode at light loads, the switching frequency is adjusted to regulate the output voltage.

The ADP2119/ADP2120 operate in PWM mode when the load current is greater than the pulse-skipping threshold current. At load currents below this value, the regulator smoothly transitions to the PFM mode of operation.

PWM MODE OPERATION

In PWM mode, the ADP2119/ADP2120 operate at a fixed frequency. At the start of each oscillator cycle, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level, turns off the P-channel MOSFET switch, and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle or until the inductor current reaches zero, which causes the zero-crossing comparator to turn off the N-channel MOSFET as well.

The peak inductor current level is set by V_{COMP}. V_{COMP} is the output of a transconductance error amplifier that compares the feedback voltage with an internal 0.6 V reference.

PFM MODE OPERATION

When PFM mode is enabled, the regulator smoothly transitions to the variable frequency PFM mode of operation when the load current decreases below the pulse-skipping threshold current. Switching continues only as necessary to maintain the output voltage within regulation. When the output voltage drops below regulation, the part enters PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

SLOPE COMPENSATION

Slope compensation stabilizes the internal current control loop of the ADP2119/ADP2120 when operating close to and beyond the 50% duty cycle to prevent subharmonic oscillations. Slope compensation is implemented by summing an artificial voltage ramp to the current sense signal during the on-time of the P-channel MOSFET switch. This voltage ramp depends on the output voltage. When operating at high output voltages, there is more slope compensation. The slope compensation ramp value determines the minimum inductor that can be used to prevent subharmonic oscillations.

ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.2 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.2 V, the regulator turns on, and when it falls below 1.1 V (typical), the regulator turns off. To force the part to automatically start when input power is applied, connect EN to VIN.

When the ADP2119/ADP2120 are shut down, the soft start capacitor is discharged. This causes a new soft start cycle to begin when the part is reenabled.

An internal pull-down resistor (1 MΩ) prevents an accidental enable if EN is left floating.

INTEGRATED SOFT START

The ADP2119/ADP2120 include integrated soft start circuitry to limit the output voltage rise time and reduce inrush current at startup. The soft start time is fixed at 1024 clock cycles.

If the output voltage is precharged prior to turn-on, the part prevents reverse inductor current (which would discharge the output capacitor) by keeping both MOSFETs turned off until the soft start voltage exceeds the voltage on the FB pin.

TRACKING

The ADP2119/ADP2120 have a tracking input, TRK, that allows the output voltage to track another voltage (master voltage). The tracking input is especially useful in core and I/O voltage tracking for FPGAs, DSPs, and ASICs.

The internal error amplifier includes three positive inputs: the internal reference voltage, the soft start voltage, and the TRK voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages. To track a master voltage, tie the TRK pin to a resistor divider from the master voltage. If the tracking function is not used, connect the TRK pin to VIN.

OSCILLATOR AND SYNCHRONIZATION

To synchronize the ADP2119/ADP2120, drive an external clock at the SYNC/MODE pin. The frequency of the external clock can be in the 1 MHz to 2 MHz range. During synchronization, the regulator operates in CCM mode only, and the switching frequency is in phase with the external clock.

CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2119/ADP2120 have a peak current limit protection circuit to prevent current runaway. When the inductor peak current reaches the current limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle starts. The overcurrent counter increments during this time. If the overcurrent counter count exceeds 10, the part enters hiccup mode and both the high-side MOSFET and low-side MOSFET are turned off. The part remains in this mode for 4096 clock cycles and then attempts to restart from soft start. If the current limit fault has cleared, the part resumes normal operation. Otherwise, it reenters hiccup mode again after counting 10 current limit violations.

OVERVOLTAGE PROTECTION (OVP)

The output voltage is continuously monitored by a comparator through the FB pin, which is at 0.6 V (typical) under normal operation. This comparator is set to activate when the FB voltage exceeds 0.66 V (typical), thus indicating an output overvoltage condition. If the voltage remains above this threshold for 16 clock cycles, the high-side MOSFET turns off and the low-side MOSFET turns on until the current through the low-side MOSFET reaches the limit (−0.6 A for forced continuous conduction mode and 0 A for PFM mode). Thereafter, both the MOSFETs are held in the off state until FB falls below 0.54 V (typical), at this point, the part restarts. The behavior of PGOOD under this condition is described in the Power Good section.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry is integrated in the ADP2119/ADP2120. If the input voltage drops below 2.1 V, the part shuts down and both the power switch and synchronous rectifier turn off. When the voltage rises again above 2.2 V, the soft start period is initiated, and the part is enabled.

THERMAL SHUTDOWN

If the ADP2119/ADP2120 junction temperatures rise above 150°C, the thermal shutdown circuit turns off the regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 25°C hysteresis is included so that if thermal shutdown occurs, the part does not return to operation until the on-chip temperature drops below 125°C. When coming out of thermal shutdown, soft start is initiated.

POWER GOOD (PGOOD)

PGOOD is an active high, open-drain output and requires a resistor to pull it up to a voltage. A high indicates that the voltage on the FB pin (and therefore the output voltage) is within ±10% of the desired value. A low on this pin indicates that the voltage on the FB pin is not within ±10% of the desired value. There is a 16 cycle waiting period after FB is detected as being out of bounds.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2119/ADP2120 are supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

This section describes the selection of the external components for the ADP2119/ADP2120. The typical application circuit for the ADP2119 is shown in Figure 50.

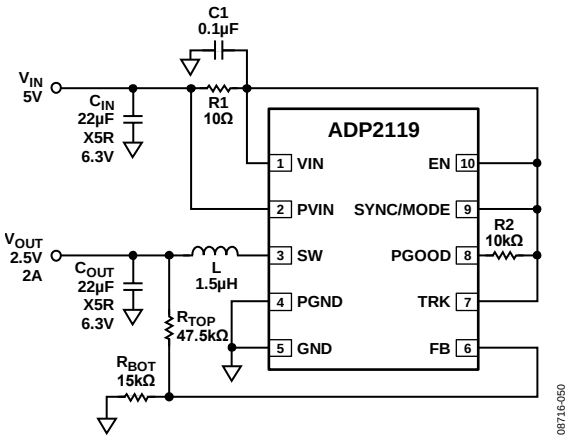

Figure 50. Typical Application Circuit

OUTPUT VOLTAGE SELECTION

The output voltage of the adjustable version can be set by an external resistive voltage divider, and the following equation calculates the output voltage.

$$V_{OUT} = 0.6 \times (1 + \frac{R_{TOP}}{R_{BOT}})$$

To limit the output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and ripple current. A small inductor value leads to a larger inductor current ripple and provides a faster transient response; however, it degrades efficiency. A large inductor value leads to a smaller current ripple and good efficiency but slows the transient response. As a guideline, the inductor current ripple, ΔI_L, is typically set to 1/3 of the maximum load current trade-off between the transient response and efficiency. The inductor value can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_S}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor current ripple.
D is the duty cycle. $D = V_{OUT}/V_{IN}$.

The regulator uses slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

The negative current limit (−0.6 A) also limits the minimum inductor value. The inductor current ripple (ΔI_L) calculated by the selected inductor should not exceed 1.2 A.

The peak inductor current should be kept below the peak current limit threshold value and can be calculated from

$$I_{PEAK} = I_O + \frac{\Delta I_L}{2}$$

Ensure that the rms current of the selected inductor is greater than the maximum load current and that its saturation current is greater than the peak current limit of the regulator.

OUTPUT CAPACITOR SELECTION

The output voltage ripple, load step transient, and loop stability determine the output capacitor selection.

The ESR and the capacitance determine the output ripple.

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_S} \right)$$

The load transient response depends on the inductor, the output capacitor, and the control loop.

The ADP2119/ADP2120 have integrated loop compensation to provide a simple power solution design. Table 5 and Table 6 show the typical recommended inductors and capacitors for the ADP2119/ADP2120. X5R or X7R ceramic capacitors are highly recommended.

Table 5. Recommended L and C_{OUT} Values for the ADP2119

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1	22 + 22
3.3	1.2	1	22 + 22
3.3	1.5	1	22 + 10
3.3	1.8	1	22
3.3	2.5	1	22
5	1.0	1	22 + 22
5	1.2	1.5	22 + 22
5	1.5	1.5	22 +10
5	1.8	1.5	22 +10
5	2.5	1.5	22
5	3.3	1.5	22

Table 6. Recommended L and C_{OUT} Values for the ADP2120

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1.5	22 + 10
3.3	1.2	1.5	22 + 10
3.3	1.5	1.5	22 + 10
3.3	1.8	1.5	10 + 10
3.3	2.5	1.5	10 + 10
5	1.0	1.5	22 + 10
5	1.2	1.5	22 + 10
5	1.5	2.2	22 + 10
5	1.8	2.2	10 + 10
5	2.5	2.2	10 + 10
5	3.3	2.2	10 + 10

Higher or lower inductor and output capacitor values can be used in the regulator, but the system stability and load transient performance need to be checked. The minimum output capacitor is 22 µF for the ADP2119 and 10 µF for the ADP2120, and the inductor range is 1 µH to 3.3 µH.

Table 7. Recommended Inductors

Manufacturer	Part Number
Sumida	CDRH5D18BHPNP, CDR6D23MNNP
TOKO	DE4518C, D62LCB
Coilcraft	LPS5030, LPS5015

Table 8. Recommended Capacitors

Manufacturer	Part Number	Description
Murata	GRM31CR60J226KE19	22 µF, 6.3 V, X5R, 1206
Murata	GRM319R60J106KE19	10 µF, 6.3 V, X5R, 1206
TDK	C3216X5R0J226M	22 µF, 6.3 V, X5R, 1206
TDK	C3216X5R0J106M	10 µF, 6.3 V, X5R, 1206

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A 10 µF or 22 µF ceramic capacitor is recommended. The rms current rating of the input capacitor should be larger than calculated by the following equation:

$$I_{RMS} = I_O \times \sqrt{D \times (1 - D)}$$

VOLTAGE TRACKING

The ADP2119/ADP2120 include a tracking feature that allows the output (slave voltage) to be configured to track an external voltage (master voltage), as shown in Figure 51.

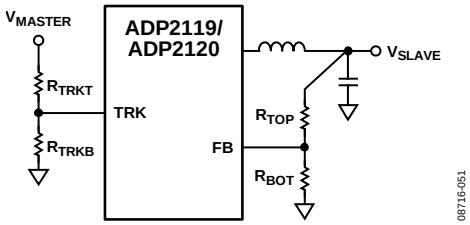

Figure 51. Voltage Tracking

A common application is coincident tracking (see Figure 52). Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the TRK pin to a resistor divider from the master voltage. For coincident tracking, set $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$.

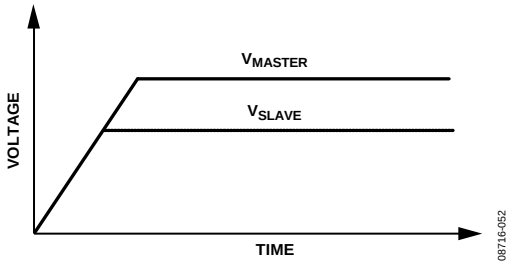

Figure 52. Coincident Tracking

Ratiometric tracking is shown in Figure 53. The slave output is limited to a fraction of the master voltage. In this application, the slave and master voltages reach the final value at the same time. The ratio of the slave output voltage to the master voltage is a function of the two dividers (see the following equation).

$$\frac{V_{SLAVE}}{V_{MASTER}} = \frac{1 + \frac{R_{TOP}}{R_{BOT}}}{1 + \frac{R_{TRKT}}{R_{TRKB}}}$$

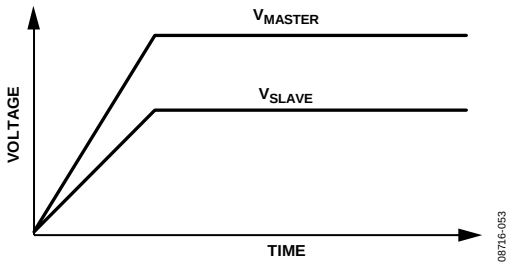

Figure 53. Ratiometric Tracking

TYPICAL APPLICATION CIRCUITS

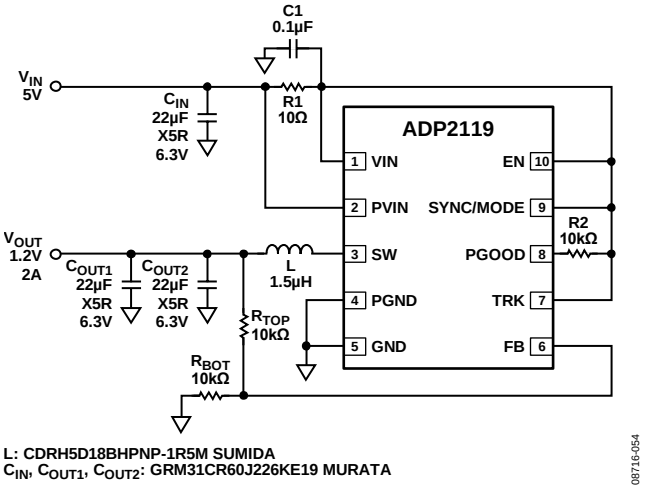

Figure 54. 1.2 V, 2 A, Step-Down Regulator, Forced Continuous Conduction Mode (ADP2119)

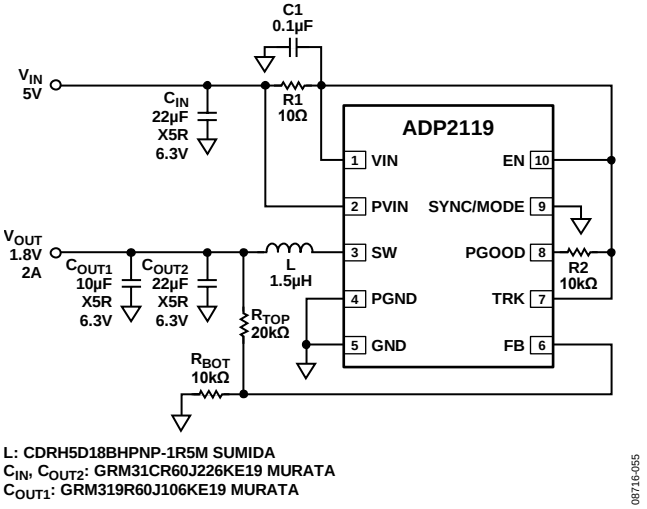

Figure 55. 1.8 V, 2 A, Step-Down Regulator, Enable PFM Mode (ADP2119)

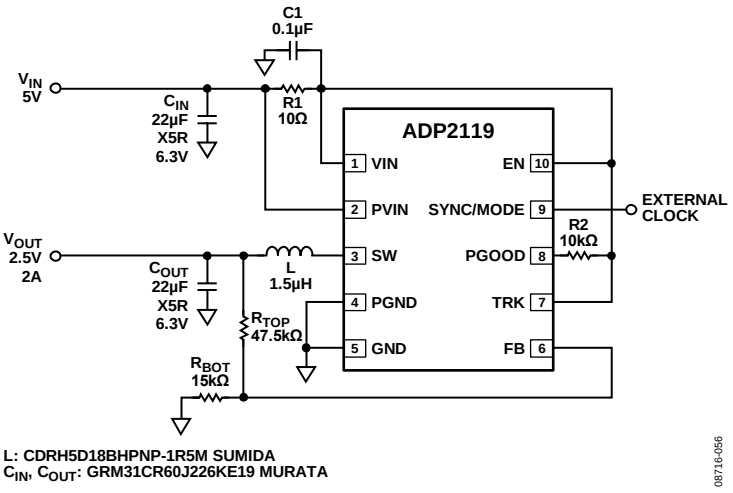

Figure 56. 2.5 V, 2 A, Step-Down Regulator, Synchronized to External Clock (ADP2119)

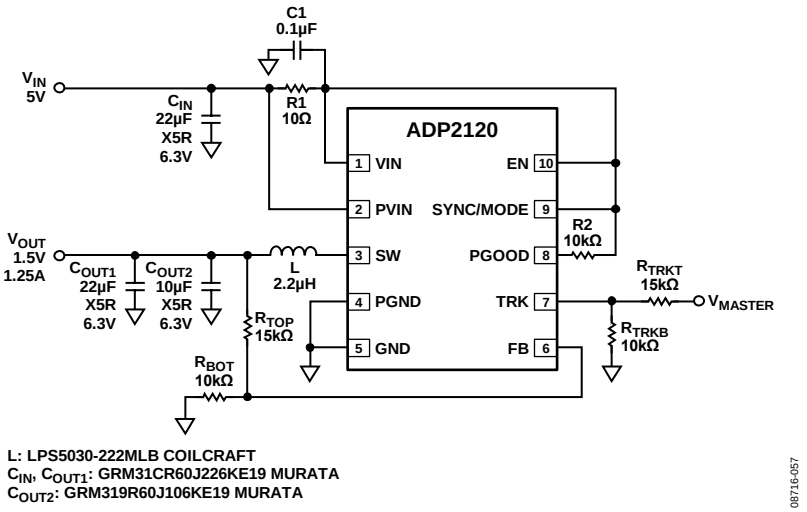

Figure 57. 1.5 V, 1.25 A, Step-Down Regulator, Tracking Mode (ADP2120)

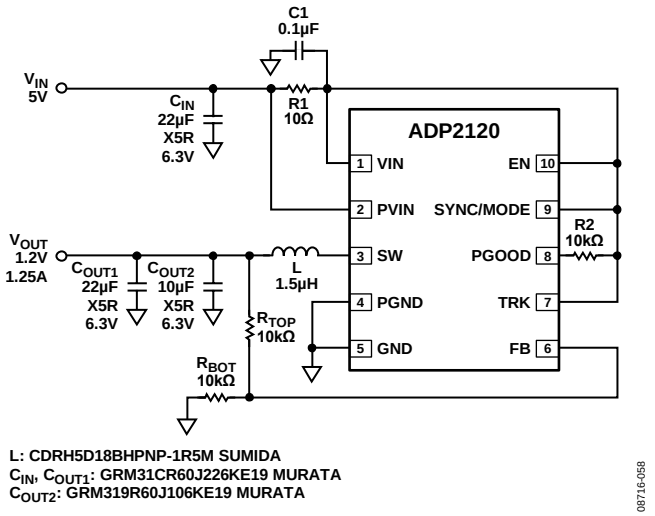

Figure 58. 1.2 V, 1.25 A, Step-Down Regulator, Forced Continuous Conduction Mode (ADP2120)

OUTLINE DIMENSIONS

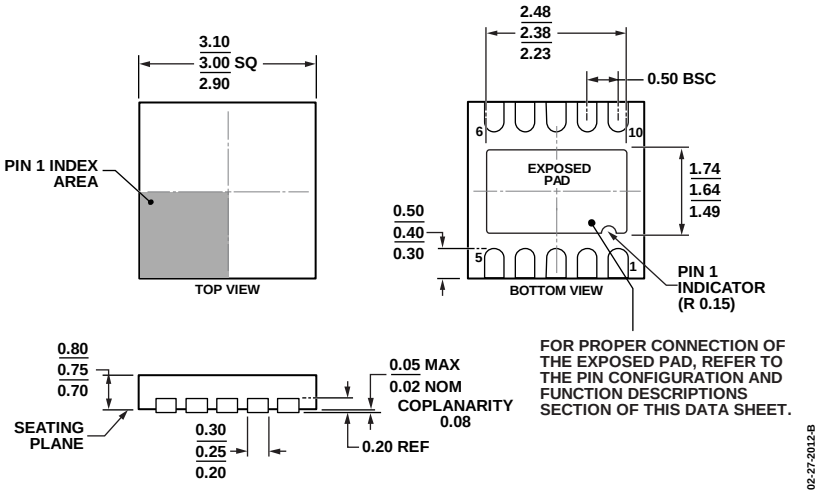

Figure 59. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Current	Temperature Range	Output Voltage	Package Description	Package Option	Branding
ADP2119ACPZ-R7	2 A	−40°C to +125°C	ADJ	10-Lead LFCSP_WD	CP-10-9	LFL
ADP2119ACPZ-1.0-R7	2 A	−40°C to +125°C	1.0 V	10-Lead LFCSP_WD	CP-10-9	LEV
ADP2119ACPZ-1.2-R7	2 A	−40°C to +125°C	1.2 V	10-Lead LFCSP_WD	CP-10-9	LFK
ADP2119ACPZ-1.5-R7	2 A	−40°C to +125°C	1.5 V	10-Lead LFCSP_WD	CP-10-9	LFM
ADP2119ACPZ-1.8-R7	2 A	−40°C to +125°C	1.8 V	10-Lead LFCSP_WD	CP-10-9	LFN
ADP2119ACPZ-2.5-R7	2 A	−40°C to +125°C	2.5 V	10-Lead LFCSP_WD	CP-10-9	LFP
ADP2119ACPZ-3.3-R7	2 A	−40°C to +125°C	3.3 V	10-Lead LFCSP_WD	CP-10-9	LFR
ADP2120ACPZ-R7	1.25 A	−40°C to +125°C	ADJ	10-Lead LFCSP_WD	CP-10-9	LEW
ADP2120ACPZ-1.0-R7	1.25 A	−40°C to +125°C	1.0 V	10-Lead LFCSP_WD	CP-10-9	LFS
ADP2120ACPZ-1.2-R7	1.25 A	−40°C to +125°C	1.2 V	10-Lead LFCSP_WD	CP-10-9	LFT
ADP2120ACPZ-1.5-R7	1.25 A	−40°C to +125°C	1.5 V	10-Lead LFCSP_WD	CP-10-9	LFU
ADP2120ACPZ-1.8-R7	1.25 A	−40°C to +125°C	1.8 V	10-Lead LFCSP_WD	CP-10-9	LFV
ADP2120ACPZ-2.5-R7	1.25 A	−40°C to +125°C	2.5 V	10-Lead LFCSP_WD	CP-10-9	LFW
ADP2120ACPZ-3.3-R7	1.25 A	−40°C to +125°C	3.3 V	10-Lead LFCSP_WD	CP-10-9	LFX
ADP2119-EVALZ				Evaluation Board		
ADP2120-EVALZ				Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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