



# STS12N3LLH5

N-channel 30 V, 0.0068  $\Omega$ , 12 A, SO-8  
STripFET™ V Power MOSFET

Datasheet — production data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS12N3LLH5	30 V	< 0.0075 $\Omega$	12 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Application

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

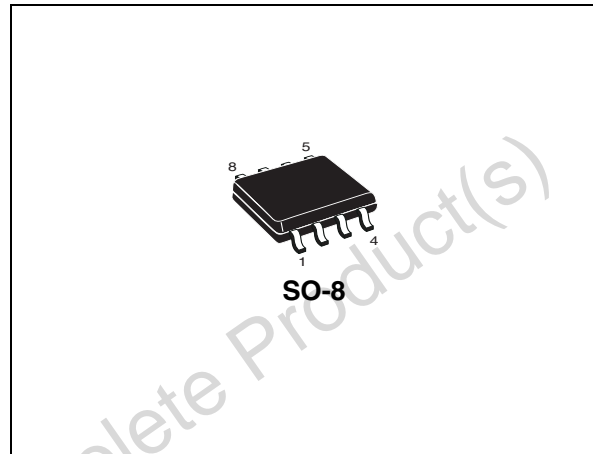


Figure 1. Internal schematic diagram

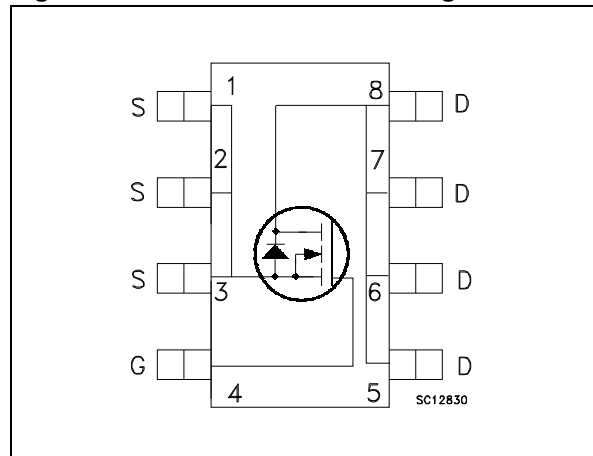


Table 1. Device summary

Order code	Marking	Package	Packaging
STS12N3LLH5	12D3L	SO-8	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	+22/-20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	12	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	8.75	A
$I_{DM}^{(2)}$	Drain current (pulsed)	48	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ °C}$	2.7	W
	Derating factor	0.02	W/°C
$T_J$	Operating junction temperature	-55 to 150	°C
$T_{stg}$	Storage temperature		

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	47	°C/W

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating},$ $V_{DS} = \text{max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = +22/-20 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 6 A$ $V_{GS} = 4.5 V, I_D = 6 A$		0.0068 0.0084	0.0075 0.0092	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	1290		pF
$C_{oss}$	Output capacitance			240		pF
$C_{rss}$	Reverse transfer capacitance			32		pF
$Q_g$	Total gate charge	$V_{DD} = 15 V, I_D = 12 A$ $V_{GS} = 4.5 V$ <i>Figure 14</i>	-	8		nC
$Q_{gs}$	Gate-source charge			3.6		nC
$Q_{gd}$	Gate-drain charge			3.4		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15 V, I_D = 6 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ <i>Figure 13</i>	-	8.6		ns
$t_r$	Rise time			11.2		ns
$t_{d(off)}$	Turn-off delay time			32.4		ns
$t_f$	Fall time			6		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12 \text{ A}, V_{GS}=0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 25 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	22		ns
$Q_{rr}$	Reverse recovery charge		-	15		nC
$I_{RRM}$	Reverse recovery current		-	1.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

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## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

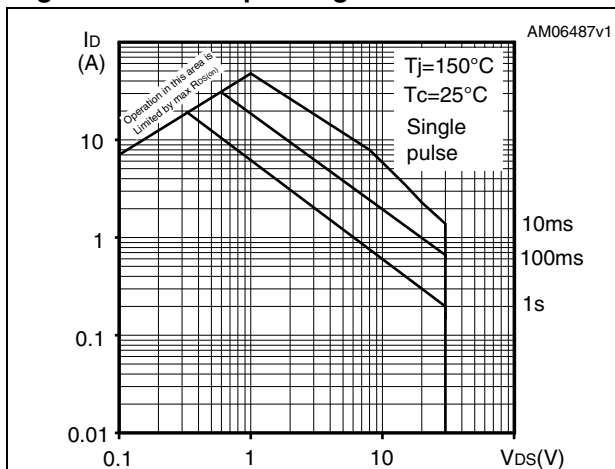


Figure 3. Thermal impedance

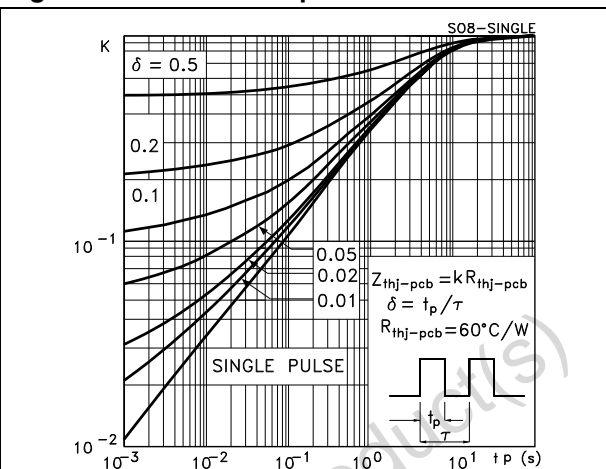


Figure 4. Output characteristics

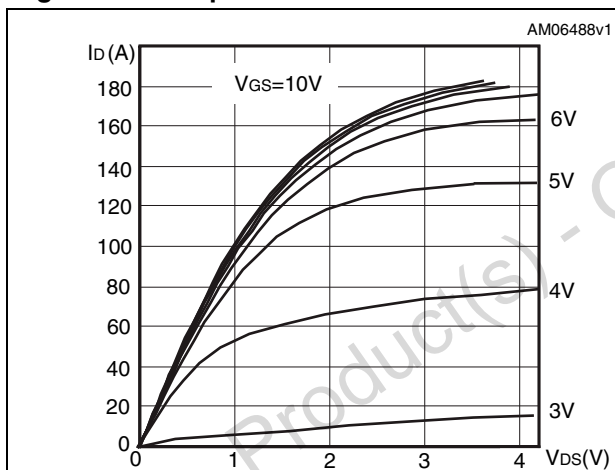


Figure 5. Transfer characteristics

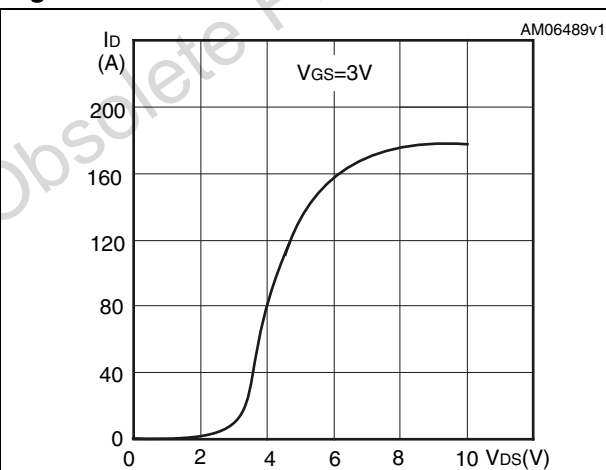


Figure 6. Normalized BV<sub>DSS</sub> vs temperature

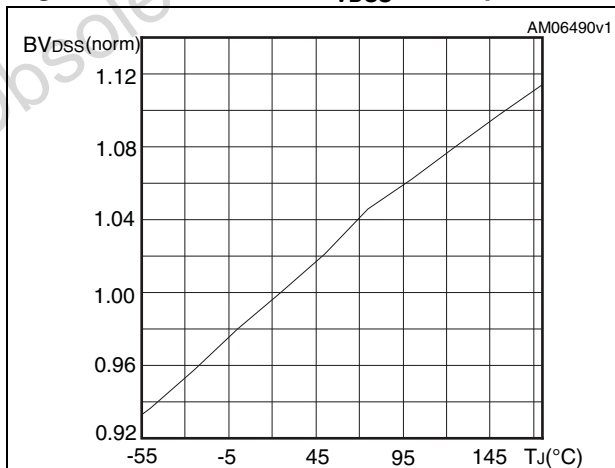


Figure 7. Static drain-source on-resistance

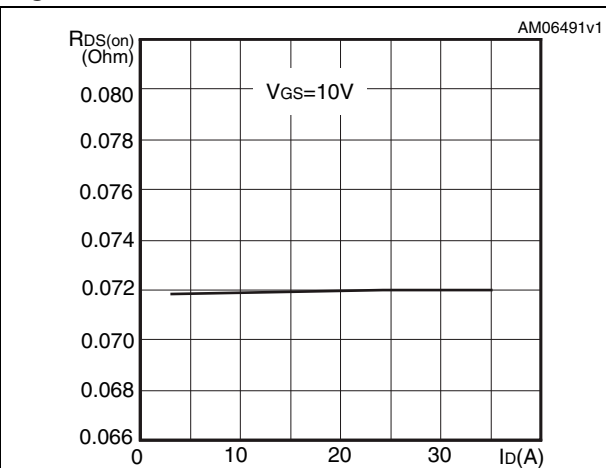


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

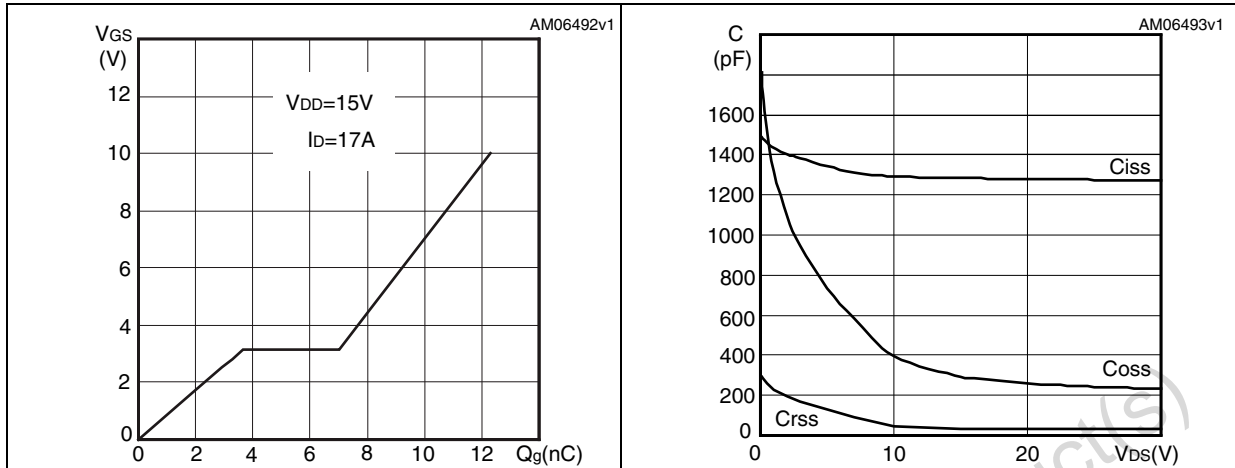


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

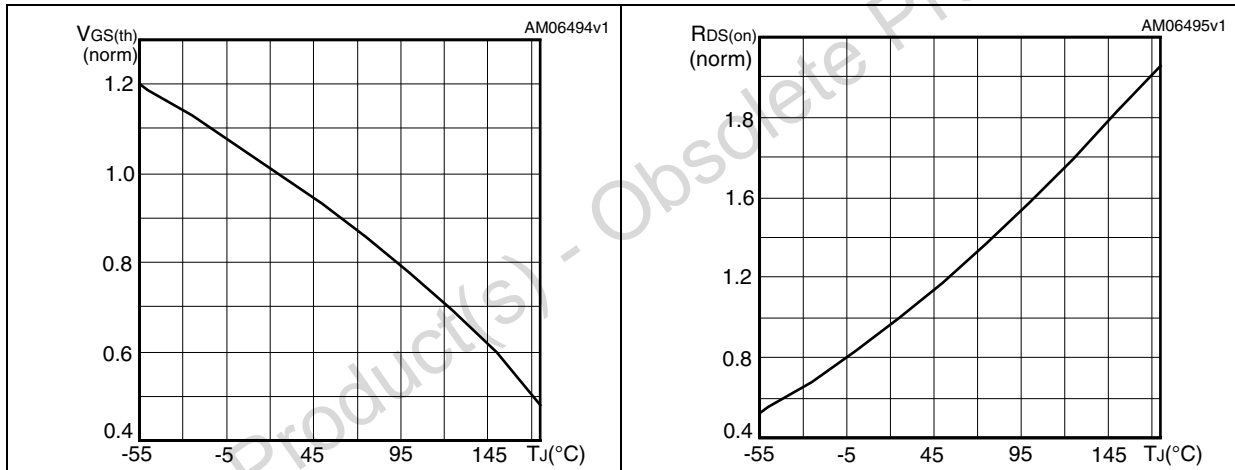
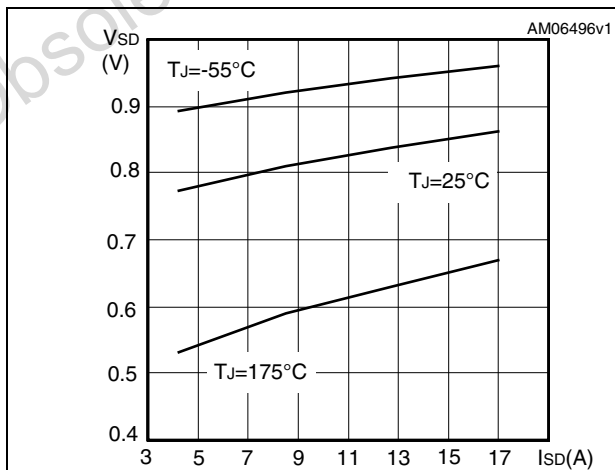
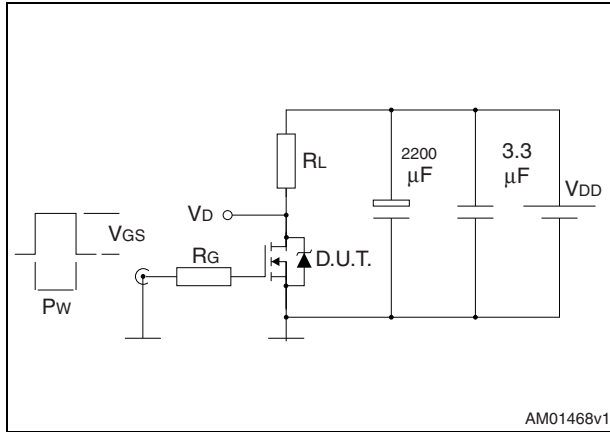


Figure 12. Source-drain diode forward characteristics

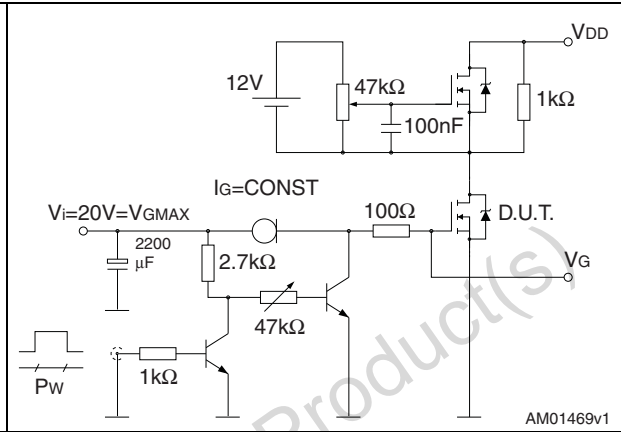


### 3 Test circuits

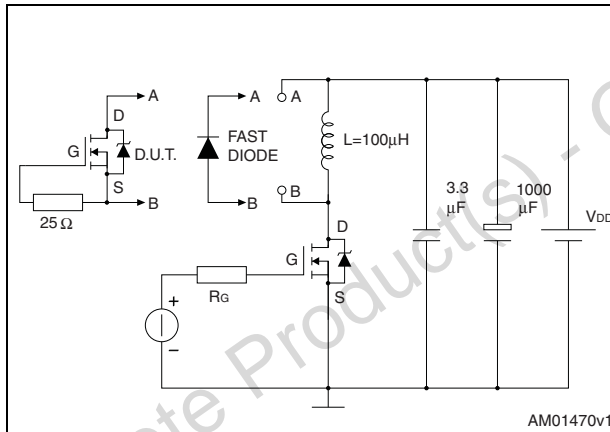
**Figure 13. Switching times test circuit for resistive load**



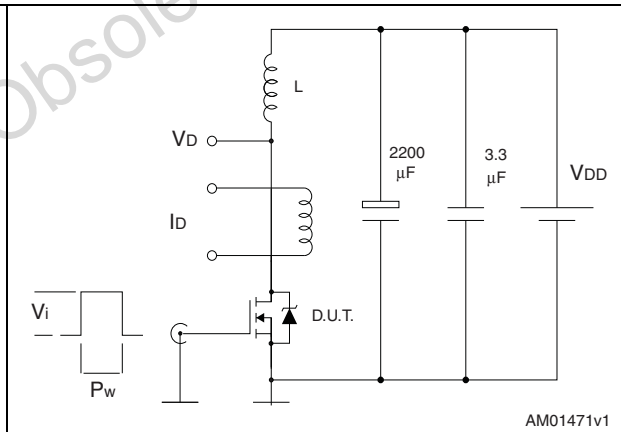
**Figure 14. Gate charge test circuit**



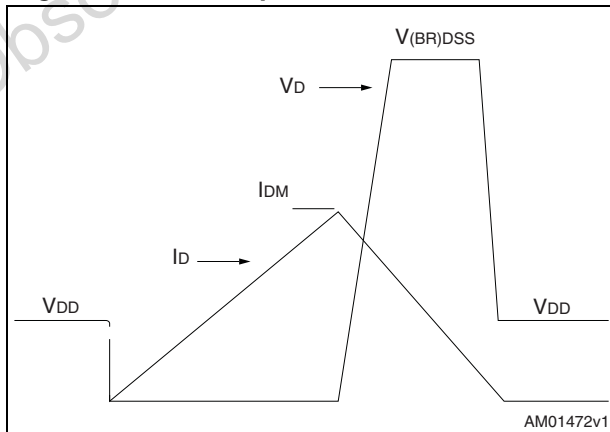
**Figure 15. Test circuit for inductive load switching and diode recovery times**



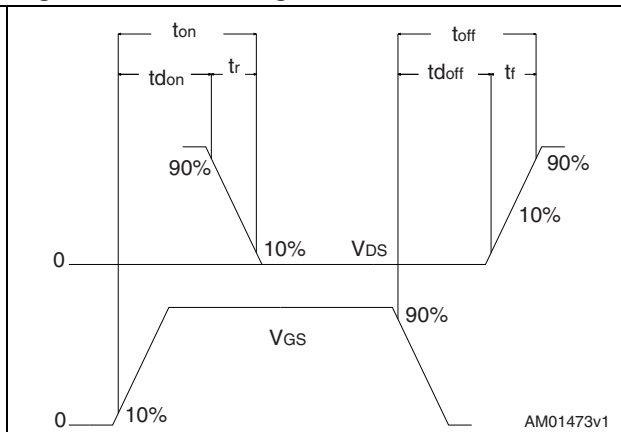
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package mechanical data

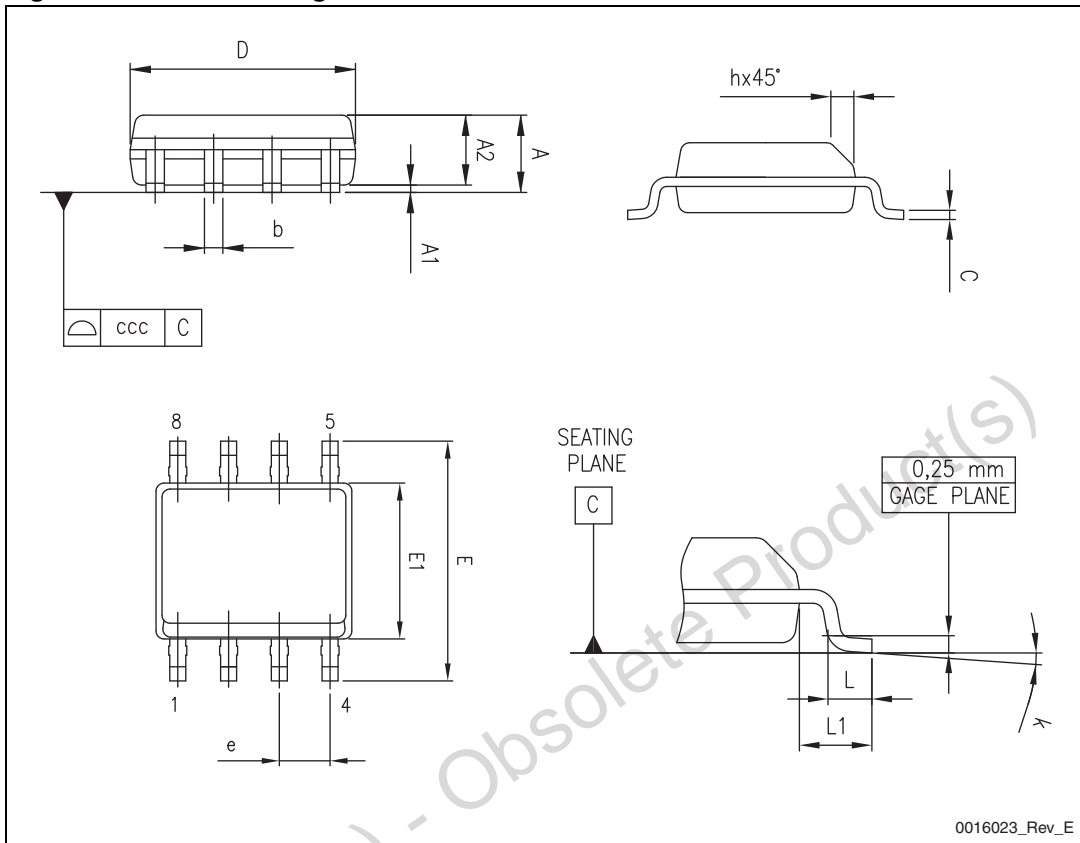
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Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 19. SO-8 drawing



0016023\_Rev\_E

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
19-Feb-2010	1	First release.
01-Jul-2011	2	Datasheet status promoted from preliminary data to datasheet. Modified: <a href="#">Table 2</a> and <a href="#">4</a> .
07-Jun-2012	3	Updated mechanical data. Minor text changes.

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