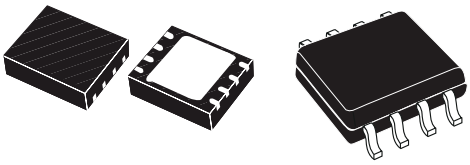
ST1S31

3 A DC step-down switching regulator

Datasheet - production data



VFDFPN 3 x 3 - 8L **SO8**

Features

- 3 A DC output current
- 2.8 V to 5.5 V input voltage
- Output voltage adjustable from 0.8 V
- 1.5 MHz switching frequency
- Internal soft-start and enable
- Integrated 60 mΩ and 45 mΩ power MOSFETs
- All ceramic capacitor
- Power Good (POR)
- Cycle-by-cycle current limiting
- Current foldback short-circuit protection
- VFDFPN 3 x 3 - 8L, SO8 packages

Applications

- µP/ASIC/DSP/FPGA core and I/O supplies
- Point of load for: STB, TVs, DVDs
- Optical storage, hard disk drive, printers, audio/graphic cards

Description

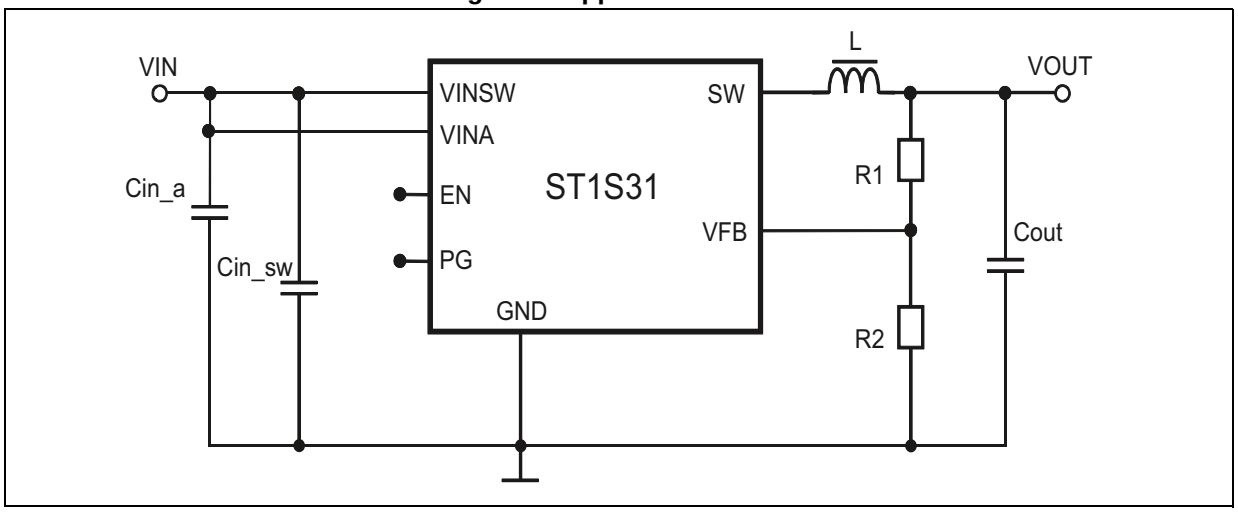
The ST1S31 device is an internally compensated 1.5 MHz fixed-frequency PWM synchronous step-down regulator. The ST1S31 operates from 2.8 V to 5.5 V input, while it regulates an output voltage as low as 0.8 V and up to V_{IN}.

The ST1S31 integrates a 60 mΩ high-side switch and a 45 mΩ synchronous rectifier allowing very high efficiency with very low output voltages.

The peak current mode control with internal compensation delivers a very compact solution with a minimum component count.

The ST1S31 device is available in 3 mm x 3 mm, 8 lead VFDFPN and SO8 packages.

Figure 1. Application circuit



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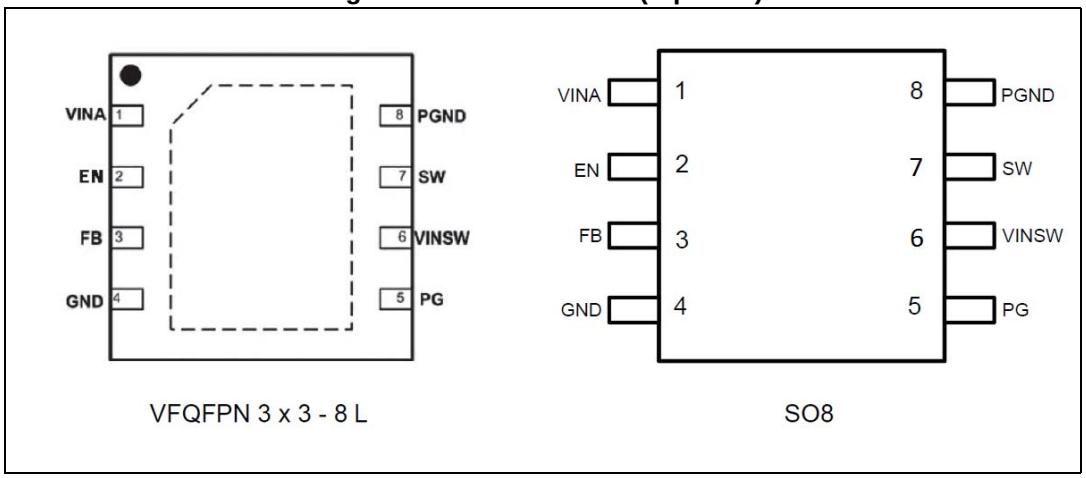
Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Type	Description
1	VINA	Unregulated DC input voltage
2	EN	Enable input. With EN higher than 1.5 V the device is ON and with EN lower than 0.5 V the device is OFF.
3	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from V_{OUT} to the FB pin.
4	AGND	Ground
5	PG	Open drain Power Good (POR) pin. It is released (open drain) when the output voltage is higher than 0.92 * V_{OUT} with a delay of 170 µs. If the output voltage is below 0.92 * V_{OUT}, the POR pin goes to low impedance immediately. If not used, it can be left floating or to GND.
6	VINSW	Power input voltage
7	SW	Regulator output switching pin
8	PGND	Power ground
	ePAD	(VFDFPN package only) exposed pad connected to ground assuring electrical contact and heat conduction.

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to 7	V
V_{EN}	Enable voltage	-0.3 to V_{IN}	
V_{SW}	Output switching voltage	-1 to V_{IN}	
V_{PG}	Power-on reset voltage (Power Good)	-0.3 to V_{IN}	
V_{FB}	Feedback voltage	-0.3 to 1.5	
P_{TOT}	Power dissipation at T_A < 60 °C	1.5 (VFDFPN) 0.9 (SO8)	W
T_{OP}	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient(1)	VFDFPN	50	°C/W
		SO8	100	

1. Package mounted on demonstration board.

3 Electrical characteristics

T_J = 25 °C, V_{IN} = 5 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{IN}	Operating input voltage range	(1)	2.8		5.5	V
V_{INON}	Turn-on V_{CC} threshold	(1)		2.4		
V_{INOFF}	Turn-off V_{CC} threshold	(1)		2.0		
R_{DSON}-P	High-side switch ON-resistance	I_{SW} = 300 mA		60		mΩ
R_{DSON}-N	Low-side switch ON-resistance	I_{SW} = 300 mA		45		mΩ
I_{LIM}	Maximum limiting current	(2)	4.0			A
Oscillator						
F_{SW}	Switching frequency		1.2	1.5	1.9	MHz
D_{MAX}	Maximum duty cycle	(2)	95		100	%
	Dynamic characteristics					
V_{FB}	Feedback voltage		0.792	0.8	0.808	V
		Io = 10 mA to 4 A(1)	0.776	0.8	0.824	
$\%V_{OUT}/\Delta I_{OUT}$	Reference load regulation	Io = 10 mA to 4 A(2)		0.2	0.6	%
$\%V_{OUT}/\Delta V_{IN}$	Reference line regulation	V_{IN} = 2.8 V to 5.5 V(2)		0.2	0.3	%
DC characteristics						
I_Q	Quiescent current	Duty cycle = 0, no load V_{FB} = 1.2 V		630	1200	µA
I_{QST-BY}	Total standby quiescent current	OFF			1	µA
Enable						
V_{EN}	EN threshold voltage	Device ON level	1.5			V
		Device OFF level			0.5	
I_{EN}	EN current				0.1	µA
Power Good						
PG	PG threshold			92		$\%V_{FB}$
	PG hystereris		30	50		mV
	PG output voltage low	Isink = 6 mA open drain			400	
	PG rise delay			170		µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
Soft-start						
T_{SS}	Soft-start duration			400		µs
Protection						
T_{SHDN}	Thermal shutdown			150		°C
	Hystereris			20		

1. Specification referred to T_J from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

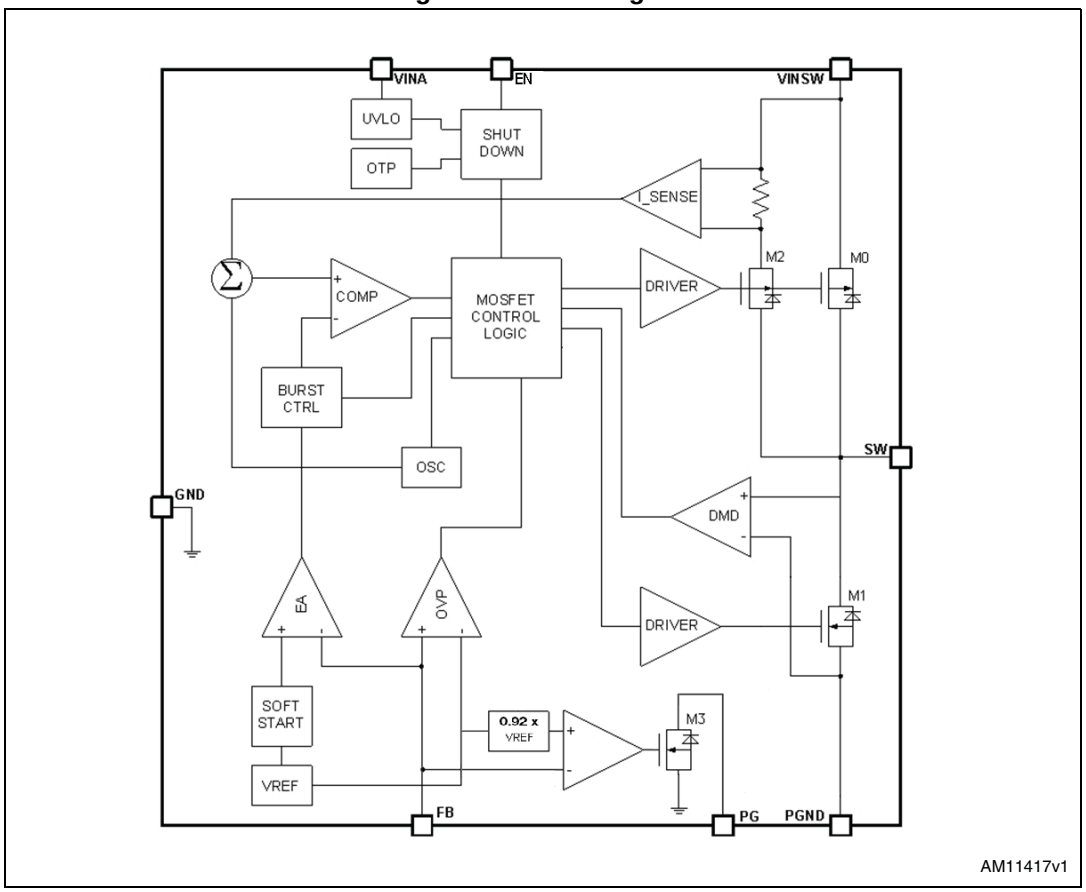
4 Functional description

The ST1S31 device is based on a “peak current mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.8 V) providing an error signal that, compared to the output of the current sense amplifier, controls the ON and OFF time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides the internal clock and the ramp for the slope compensation avoiding sub-harmonic instability
- The soft-start circuitry to limit inrush current during the startup phase
- The transconductance error amplifier
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switches
- The drivers for embedded P-channel and N-channel power MOSFET switches
- The high-side current sensing block
- The low-side current sense to implement diode emulation
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages
- A thermal shutdown block, to prevent thermal runaway.

Figure 3. Block diagram



4.1 Output voltage adjustment

The error amplifier reference voltage is 0.8 V typical. The output voltage is adjusted according to the following formula (see *Figure 1 on page 1*):

Equation 1

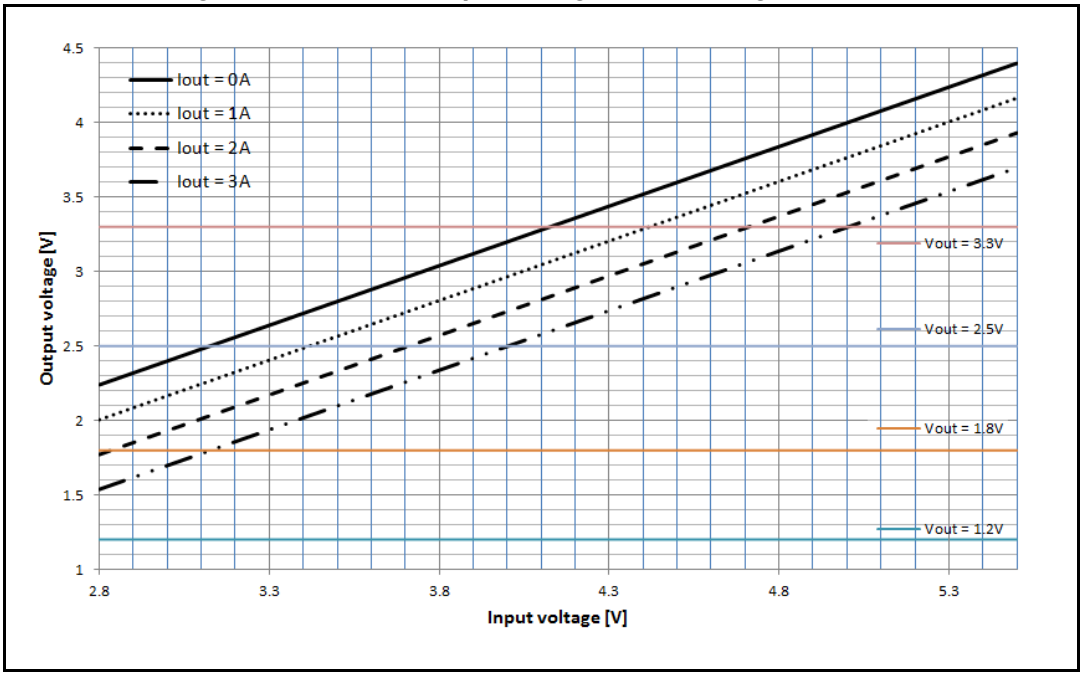
$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

The internal architecture of the device requires a minimum off time, cycle-by-cycle, for the output voltage regulation. The minimum off time is typically equal to 94 ns.

The control loop compensates for conversion losses with duty cycle control. Since the power losses are proportional to the delivered output power, the duty cycle increases with the load current request.

Figure 4 shows the maximum regulated output voltage over the input voltage range at different loading conditions.

Figure 4. Maximum output voltage over loading conditions



4.2 Soft-start

The soft-start is essential to assure the correct and safe startup of the step-down converter. It avoids inrush current surge and makes the output voltage rise monotonically.

The soft-start is managed by ramping the reference of the error amplifier from 0 V to 0.8 V. The internal soft-start capacitor is charged with a resistor to 0.8 V, then the FB pin follows the reference so that the output voltage is regulated to rise to the set value monotonically.

4.3 Error amplifier and control loop stability

The error amplifier provides the error signal to be compared with the high-side switch current through the current sense circuitry. The non inverting input is connected with the internal 0.8 V reference, while the inverting input is the FB pin. The compensation network is internal and connected between the E/A output and GND.

The error amplifier of the ST1S31 device is a transconductance operational amplifier, with high bandwidth and high output impedance.

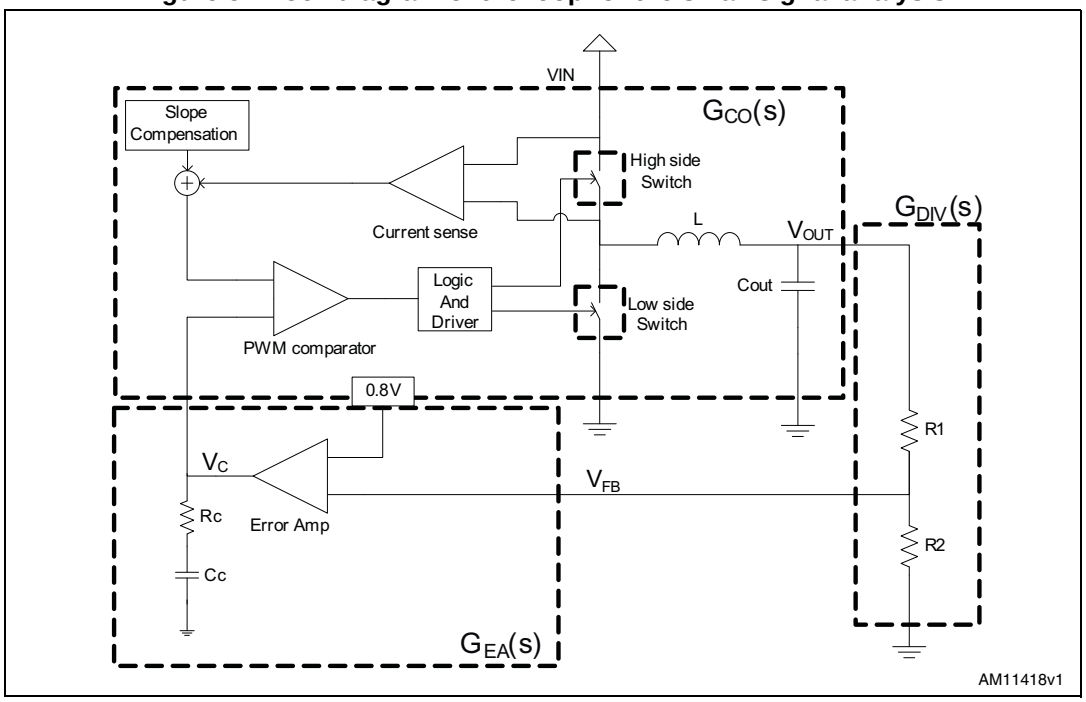
Table 5. Characteristics of the uncompensated error amplifier

Description	Value
DC gain	94 dB
gm	238 µA/V
Ro	96 MΩ

The ST1S31 device embeds the compensation network that assures the stability of the loop in the whole operating range. All the tools needed to check the loop stability are shown on the next pages of this section.

In *Figure 5* the simple small signal model for the peak current mode control loop is shown.

Figure 5. Block diagram of the loop for the small signal analysis



Three main terms can be identified to obtain the loop transfer function:

1. From control (output of E/A) to output, $G_{CO}(s)$
2. From output (V_{OUT}) to the FB pin, $G_{DIV}(s)$
3. From the FB pin to control (output of E/A), $G_{EA}(s)$.

The transfer function from control to output $G_{CO}(s)$ results:

Equation 2

$$G_{CO}(s) = \frac{R_{LOAD}}{R_i} \cdot \frac{1}{1 + \frac{R_{out} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_{LOAD} represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry (0.369 Ω), ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts for the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 3

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 4

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 5

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the ON-time slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak-to-peak amplitude - 0.535 V) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 6

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 7

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

and

Equation 8

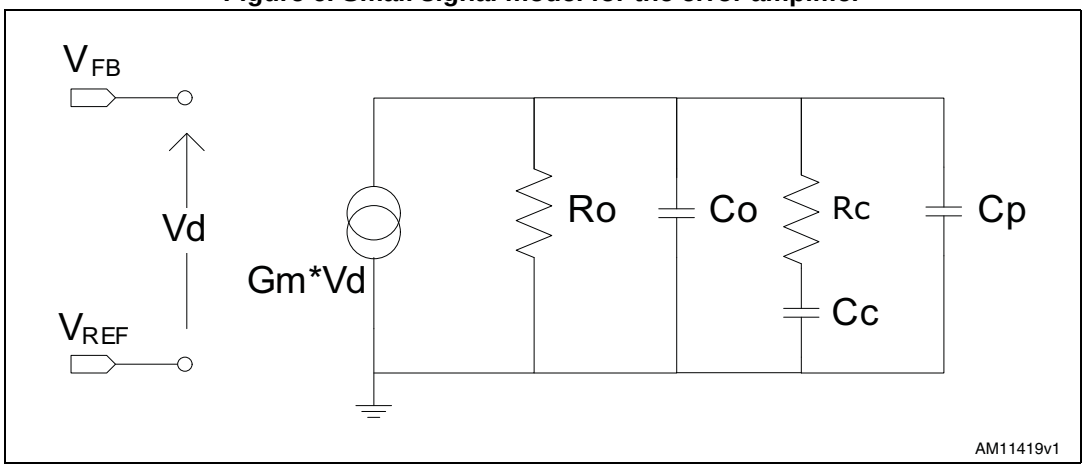
$$\omega_n = \pi \cdot f_{SW}$$

The resistor to adjust the output voltage that gives the term from output voltage to the FB pin. $G_{DIV}(s)$ is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

The transfer function from FB to Vc (output of E/A) introduces the singularities (poles and zeroes) to stabilize the loop. The small signal model of the error amplifier with the internal compensation network can be seen in *Figure 6*.

Figure 6. Small signal model for the error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability and can be neglected.

So $G_{EA}(s)$ results:

Equation 9

$$G_{EA}(s) = \frac{G_{EA0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

where $G_{EA} = G_m \cdot R_o$.

The poles of this transfer function are (if $C_c >> C_0+C_P$):

Equation 10

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 11

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 12

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C = 80 kΩ, C_C = 55 pF while C_P and C_O can be considered as negligible. The error amplifier output resistance is 96 MΩ so the relevant singularities are:

Equation 13

$$f_Z = 36,2\ kHz \qquad f_{P\,LF} = 30\ Hz$$

So closing the loop, the loop gain $G_{LOOP}(s)$ is:

Equation 14

$$G_{LOOP}(s) = G_{CO}(s) \cdot G_{DIV}(s) \cdot G_{EA}(s)$$

Example 1:

V_{IN} = 5 V, V_{OUT} = 1.2 V, I_{omax} = 3 A, L = 1.0 µH, C_{ou}t = 47 µF (MLCC), R1 = 10 kΩ, R2 = 20 kΩ (see *Section 5.2* and *Section 5.3* for inductor and output capacitor selection guidelines).

The module and phase bode plot are reported in *Figure 7* and *Figure 8*.

The bandwidth is 117 kHz and the phase margin is 63 degrees.

Figure 7. Module bode plot

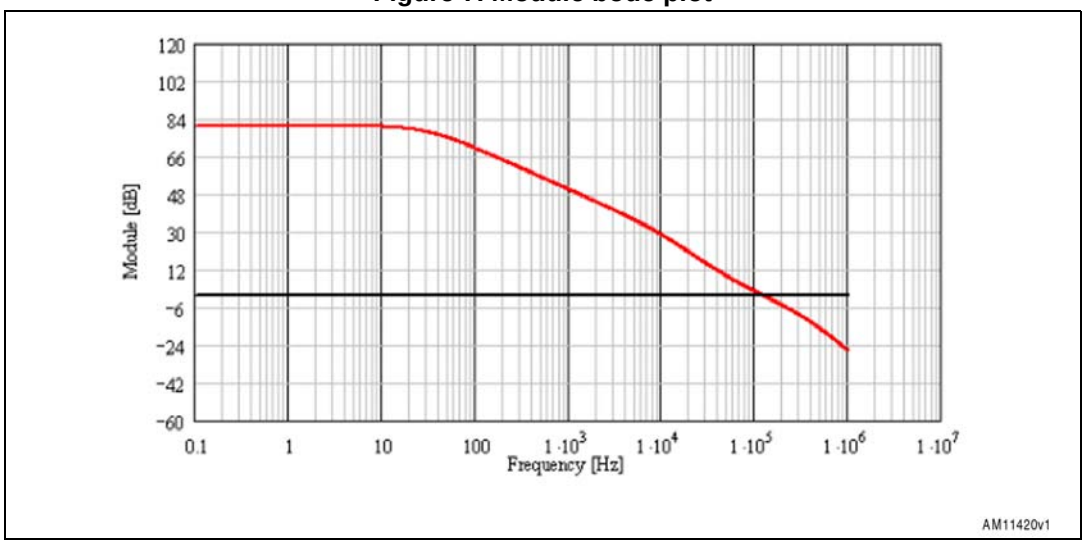
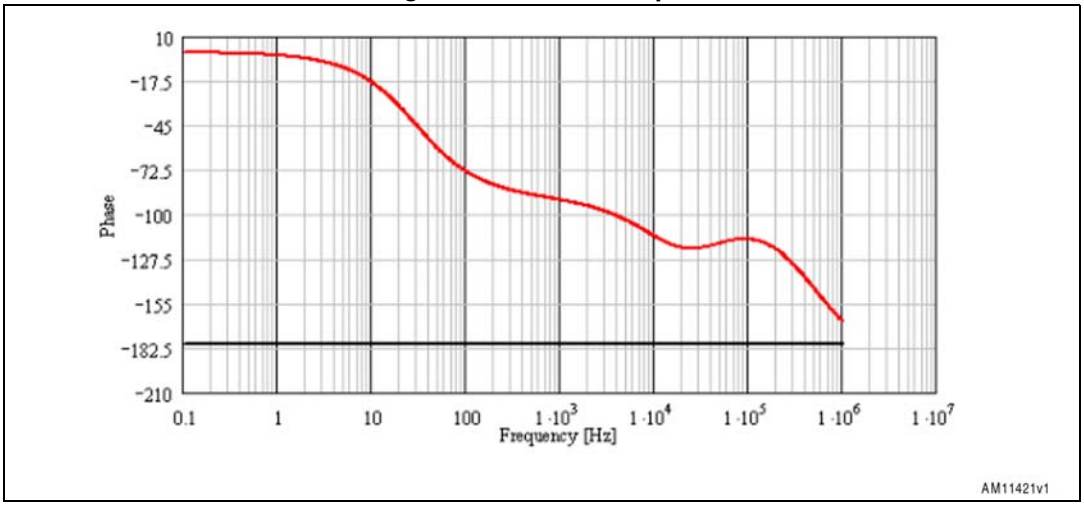


Figure 8. Phase bode plot



4.4 Overcurrent protection

The ST1S31 device implements overcurrent protection sensing the current flowing through the high-side current switch.

If the current exceeds the overcurrent threshold the high-side is turned off, implementing a cycle-by-cycle current limitation. Since the regulation loop is no longer fixing the duty cycle, the output voltage is unregulated and the FB pin falls accordingly to the new duty cycle.

If the FB falls below 0.2 V, the peak current limit is reduced to around 2.3 A and the switching frequency is reduced to assure that the inductor current is properly limited below the above mentioned value and above 1.2 A. This strategy is called “current foldback”.

The mechanism to adjust the switching frequency during the current foldback condition exploits the low-side current sense circuitry. If FB is lower than 0.2 V, the high-side power MOSFET is turned off when the current reaches the current foldback threshold (2.3 A), then, after a proper deadtime that avoids the cross conduction, the low-side is turned on until the low-side current is lower than a valley threshold (1.2 A). Once the low-side is turned off, the high-side is immediately turned on. In this way the frequency is adjusted to keep the inductor current ripple between the current foldback value (2.3 A) and valley threshold (1.2 A), so properly limiting the output current in case of overcurrent or short-circuit.

It should be noted that in some cases, mainly with very low output voltages, the hard overcurrent can cause the FB to find the new equilibrium just over the current foldback threshold (0.2 V). In this case no frequency reduction is enabled, then the inductor current may diverge. This means that the ripple current during the minimum ON-time is higher than the ripple current during the OFF-time (the switching period minus the minimum ON-time), so pulse-by-pulse, the average current is rising, exceeding the current limit.

In order to avoid too high current, a further protection is activated when the high-side current exceeds a further current threshold (OCP2) slightly over the current limit (OCP1). If the current triggers the second threshold, the converter stops switching, the reference of the error amplifier is pulled down and then it restarts with a soft-start procedure. If the overcurrent condition is still active, the current foldback with frequency reduction properly limits the output current to 2.3 A.

4.5 Enable function

The enable feature allows the device to be put into standby mode. With the EN pin is lower than 0.4 V, the device is disabled and the power consumption is reduced to less than 10 µA. With the EN pin higher than 1.2 V, the device is enabled. If the EN pin is left floating, an internal pull-down ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{IN} compatible.

4.6 Light load operation

With peak current mode control loop the output of the error amplifier is proportional to the load current. In the ST1S31 device, to increase light load efficiency when the output of the error amplifier falls below a certain threshold, the high-side turn-on is prevented.

This mechanism reduces the switching frequency at light load in order to save the switching losses.

4.7 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature goes back to about 130 °C, the device restarts in normal operation.

5 Application information

5.1 Input capacitor selection

The capacitor connected to the input must be capable of supporting the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 15

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where *Io* is the maximum DC output current, *D* is the duty cycle, and η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and is equal to Io/2.

The peak-to-peak voltage across the input capacitor can be calculated as:

Equation 16

$$V_{PP} = \frac{I_O}{C_{IN} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

where *ESR* is the equivalent series resistance of the capacitor.

Given the physical dimension, ceramic capacitors can well meet the requirements of the input filter sustaining a higher input RMS current than electrolytic / tantalum types. In this case the equation of C_{IN} as a function of the target peak-to-peak voltage ripple (V_{PP}) can be written as follows:

Equation 17

$$C_{IN} = \frac{I_O}{V_{PP} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

neglecting the small ESR of ceramic capacitors.

Considering $\eta = 1$, this function has its maximum in D = 0.5, therefore, given the maximum peak-to-peak input voltage (V_{PP_MAX}), the minimum input capacitor (C_{IN_MIN}) value is:

Equation 18

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot F_{SW}}$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage ripple in the order of 1% of V_{INMAX}.

The placement of the input capacitor is very important to avoid noise injection and voltage spikes on the input voltage pin. So the C_{IN} must be placed as close as possible to the VIN_SW pin. In *Table 6* some multilayer ceramic capacitors suitable for this device are given.

Table 6. Input MLCC capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)
Murata	GRM21	10	10
TDK	C3225	10	25
	C3216	10	16
TAIYO YUDEN	LMK212	22	10

A ceramic bypass capacitor, as close as possible to the VINA pin so that additional parasitic ESR and ESL are minimized, is suggested in order to prevent instability on the output voltage due to noise. The value of the bypass capacitor can go from 330 nF to 1 µF.

5.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value to have the expected current ripple must be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current.

In continuous current mode (CCM), the inductance value can be calculated by *Equation 19*:

Equation 19

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

where T_{ON} is the conduction time of the high-side switch and T_{OFF} is the conduction time of the low-side switch (in CCM, $F_{SW} = 1/(T_{ON} + T_{OFF})$). The maximum current ripple, given the V_{OUT}, is obtained at maximum T_{OFF}, that is, at minimum duty cycle (see previous section to calculate minimum duty). So by fixing ΔI_L = 20% to 30% of the maximum output current, the minimum inductance value can be calculated:

Equation 20

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SWMIN}}$$

where F_{SWMIN} is the minimum switching frequency, according to *Table 4*. The slope compensation, to prevent the sub-harmonic instability in the peak current control loop, is internally managed and so fixed. This implies a further lower limit for the inductor value. To assure sub-harmonic stability:

Equation 21

$$L > V_{out} / (2 \cdot V_{pp} \cdot f_{sw})$$

where V_{PP} is the peak-to-peak value of the slope compensation ramp. The inductor value selected based on *Equation 20* must satisfy *Equation 21*. The peak current through the inductor is given by *Equation 22*:

Equation 22

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

In *Table 7* some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XAL50xx	1.2 to 3.3	6.3 to 9
	XAL60xx	2.2 to 5.6	7.4 to 11
	MSS1048	1.0 to 3.8	6.5 to 11
Würth	WE-HCI 7030	1.5 to 4.7	7 to 14
	WE-PD type L	1.5 to 3.5	6.4 to 10
Coiltronics	DR73	1.0 to 2.2	5.5 to7.9
	DR74	1.5 to 3.3	5.4 to 8.35

5.3 Output capacitor selection

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 23

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor the opposite is true.

As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop.

The equations of *Section 5.2* help to check loop stability given the application conditions, the value of the inductor and of the output capacitor.

In *Table 8* some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
Murata	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
Panasonic	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
Sanyo	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

5.4 Thermal dissipation

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) conduction losses due to the on-resistance of high-side switch (R_{HS}) and low-side switch (R_{LS}); these are equal to:

Equation 24

$$P_{COND} = R_{HS} \cdot I_{OUT}^2 \cdot D + R_{LS} \cdot I_{OUT}^2 \cdot (1 - D)$$

where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but it is actually slightly higher to compensate the losses of the regulator.

b) switching losses due to high-side power MOSFET turn-on and turn-off; these can be calculated as:

Equation 25

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (V_{DS}) and the current flowing into it during the turn-on and turn-off phases, as shown in *Figure 9*. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

c) Quiescent current losses, calculated as:

Equation 26

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current (I_Q = 1.2 mA maximum).

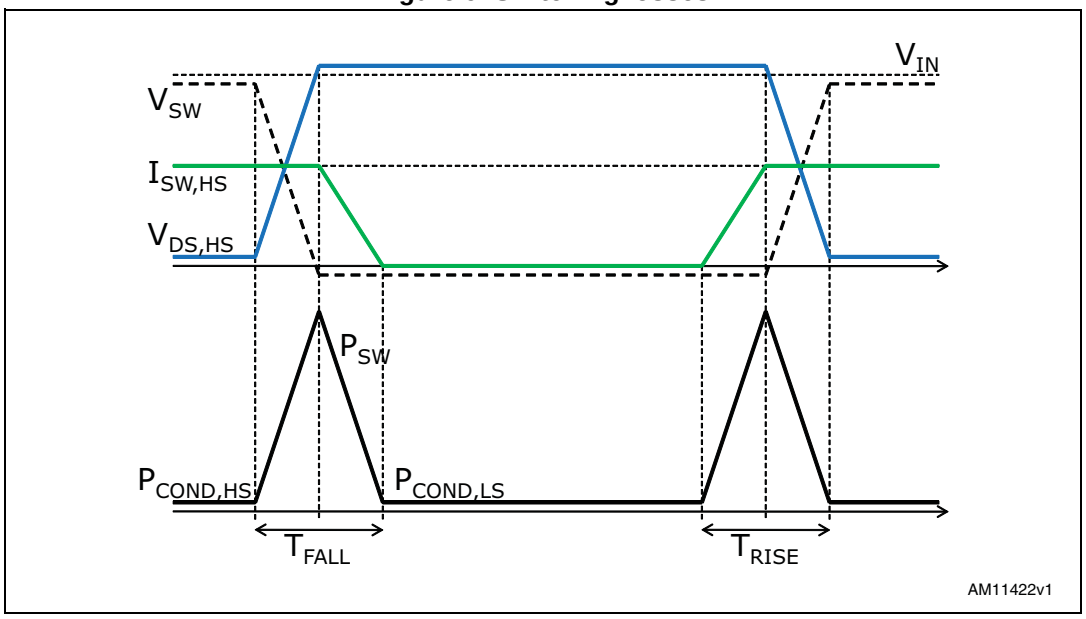
The junction temperature T_J can be calculated as:

Equation 27

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen. Rth_{JA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The Rth_{JA} measured on the demonstration board described in *Section 5.5* is about 50 °C/W for the VFDFPN and 100 °C/W for the SO8 package.

Figure 9. Switching losses



5.5 Layout consideration

The PC board layout of the switching DC-DC regulator is very important to minimize the noise injected in high impedance nodes, to reduce interference generated by the high switching current loops and to optimize the reliability of the device.

In order to avoid EMC problems, the high switching current loops must be as short as possible. In the buck converter there are two high switching current loops: during the on-time, the pulsed current flows through the input capacitor, the high-side power switch, the inductor and the output capacitor; during the off-time, through the low-side power switch, the inductor and the output capacitor.

The input capacitor connected to VINSW must be placed as close as possible to the device, to avoid spikes on VINSW due to the stray inductance and the pulsed input current.

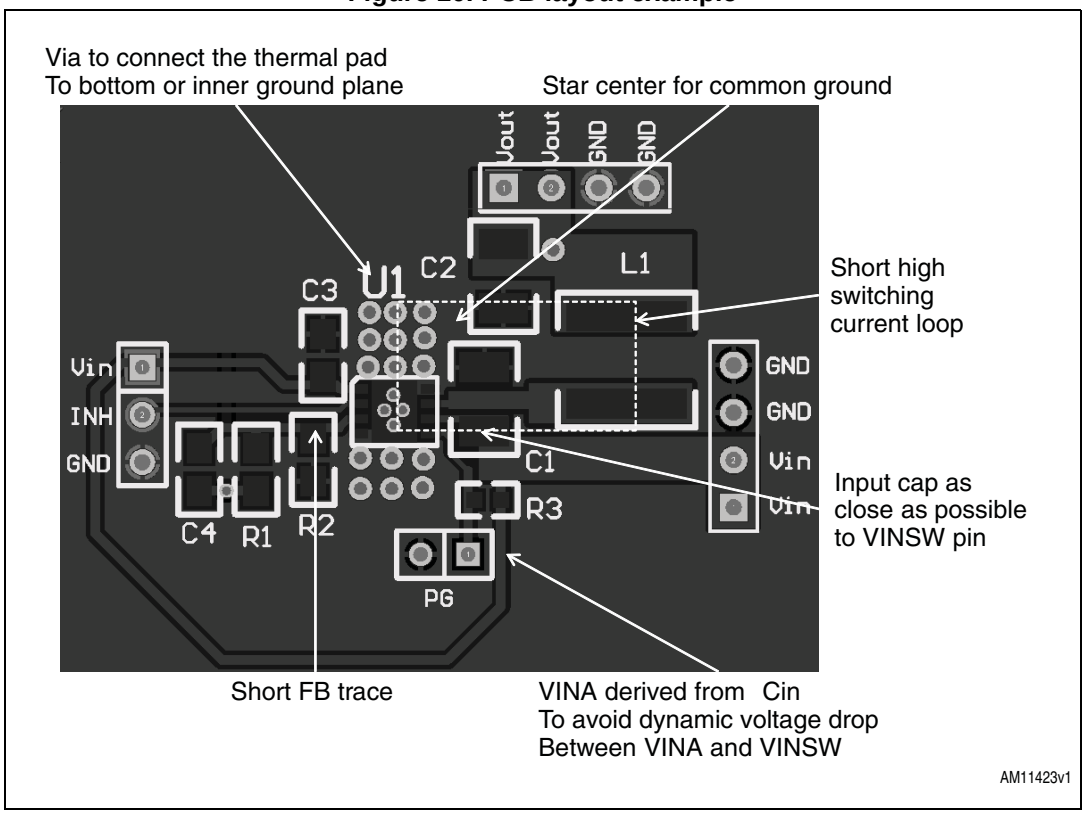
In order to prevent dynamic unbalance between VINSW and VINA, the trace connecting the VINA pin to the input must be derived from VINSW.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by routing the feedback node with a very short trace and as far as possible from the high current paths.

A single point connection from signal ground to power ground is suggested.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane, soldered to the exposed pad, enhances the thermal performance of the converter allowing high power conversion.

Figure 10. PCB layout example



6 Demonstration board

Figure 11. Demonstration board schematic

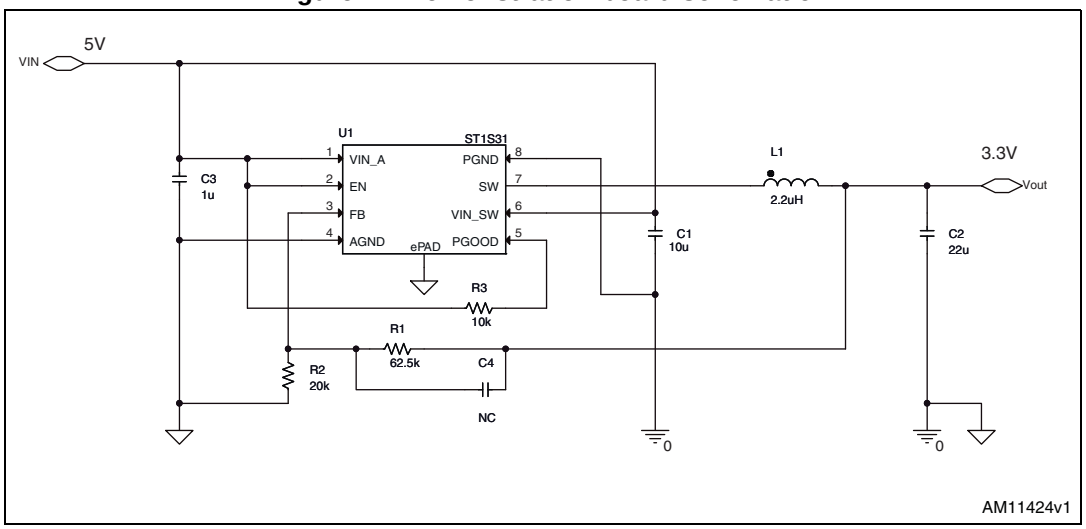


Table 9. Component list

Reference	Part number	Description	Manufacturer
U1	ST1S31		ST
L1	DR73 2R2	2.2 µH, Isat = 5.5 A	Coiltronics
C1	C3225X7RE106K	10 µF 25 V X7R	TDK
C2	C3225X7R1C226M	22 µF 16 V X7R	TDK
C3		1 µF 25 V X7R	
C4		NC	
R1		62.5 kΩ	
R2		20 kΩ	
R3		10 kΩ	

Figure 12. Demonstration board PCB top and bottom, DFN package

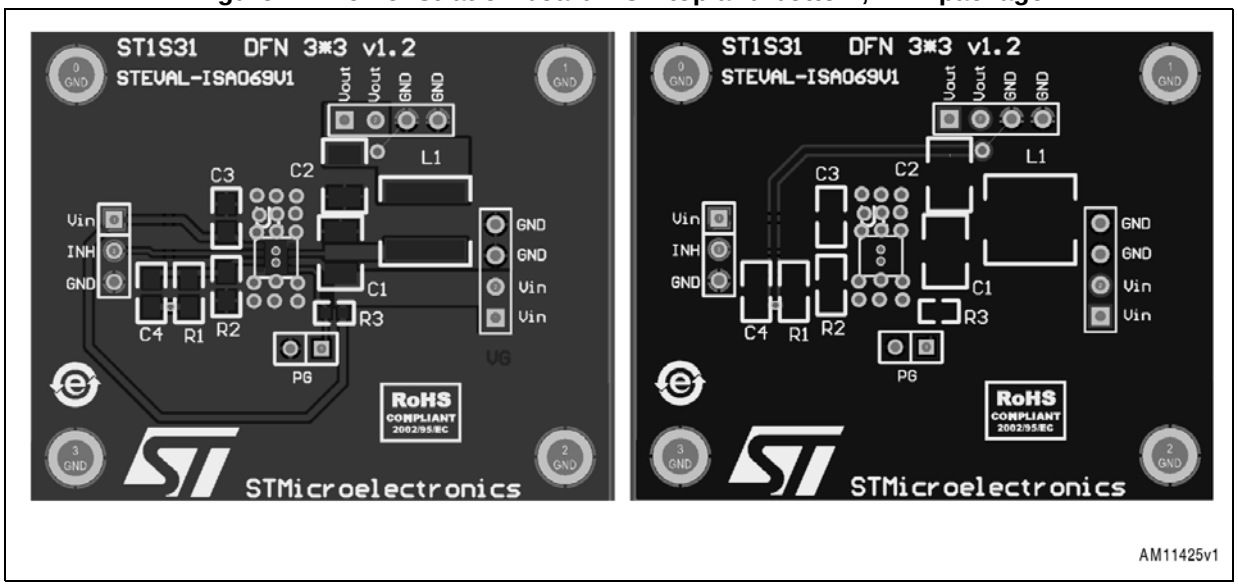
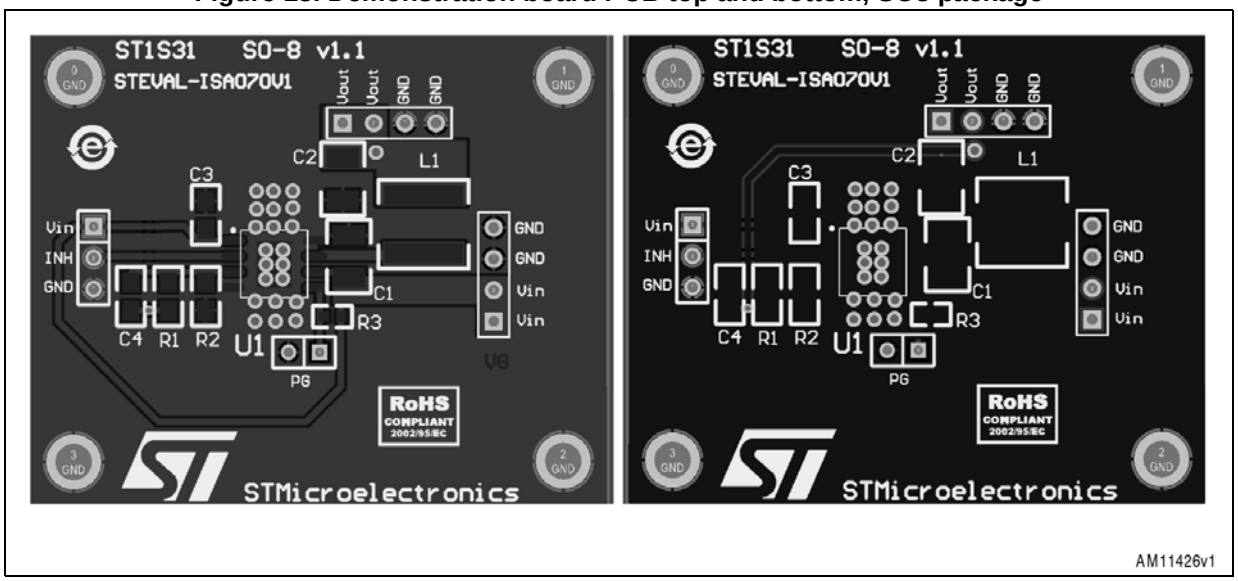


Figure 13. Demonstration board PCB top and bottom, SO8 package



7 Typical characteristics

Figure 14. Efficiency curves: V_{IN} = 3.3 V

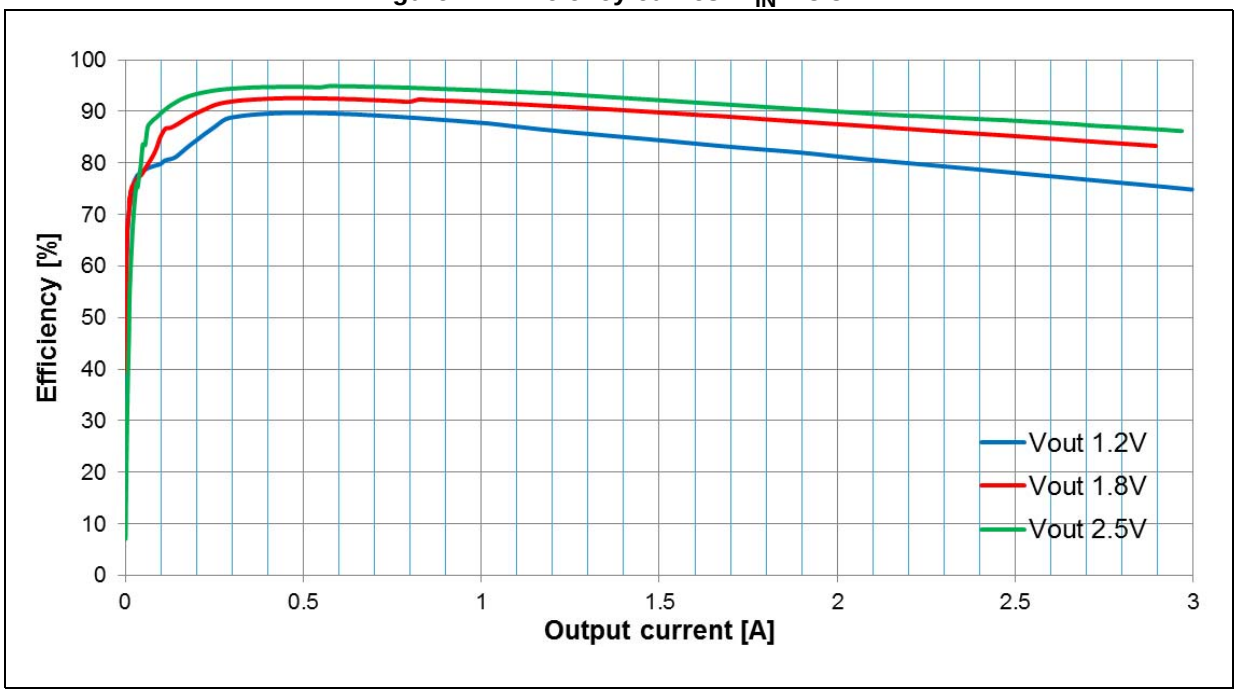


Figure 15. Efficiency curves: V_{IN} = 3.3 V (log scale)

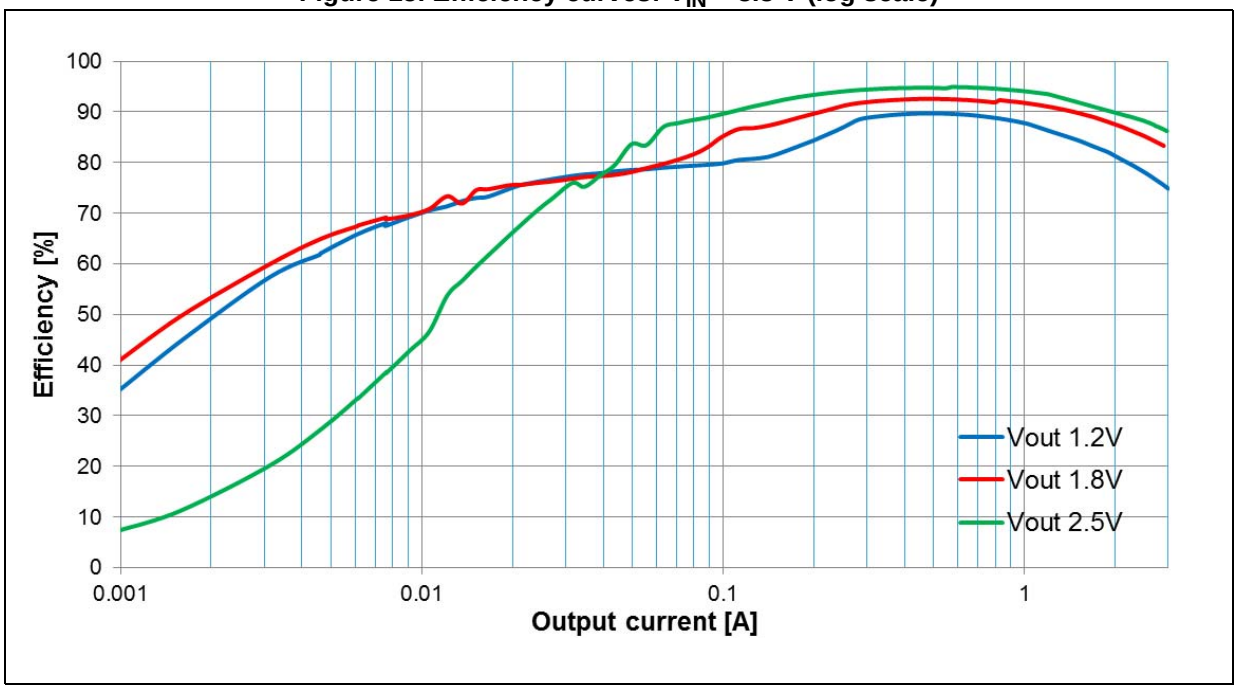


Figure 16. Load regulation (V_{IN} = 3.3 V)

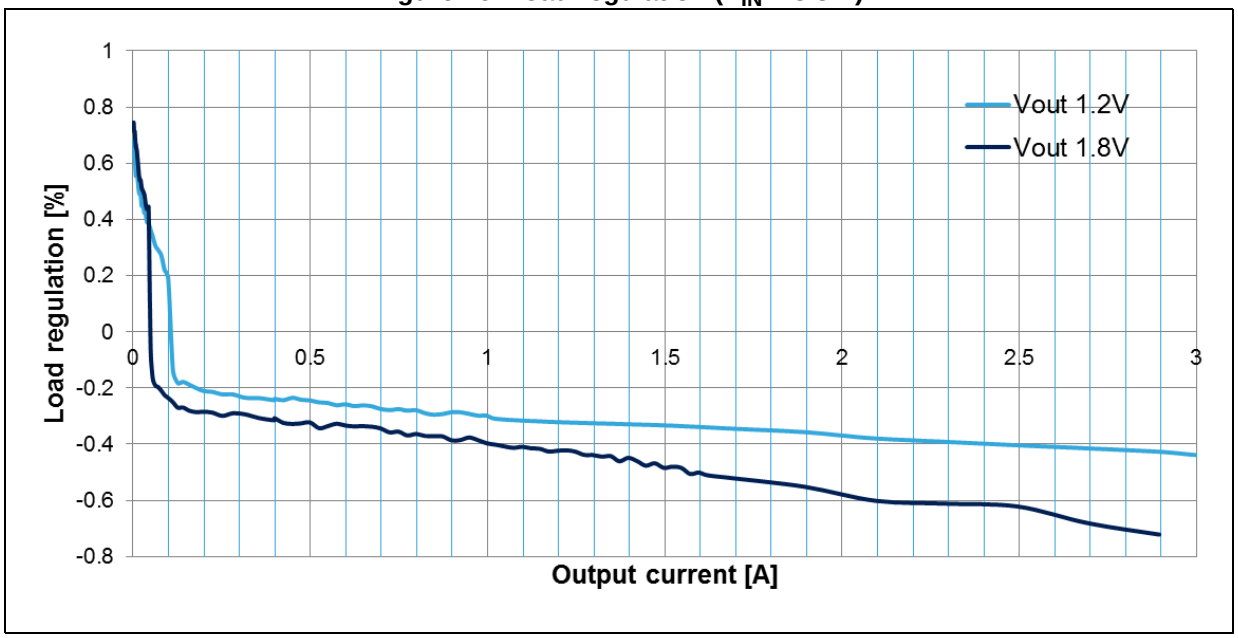


Figure 17. Efficiency curves: V_{IN} = 4.0 V

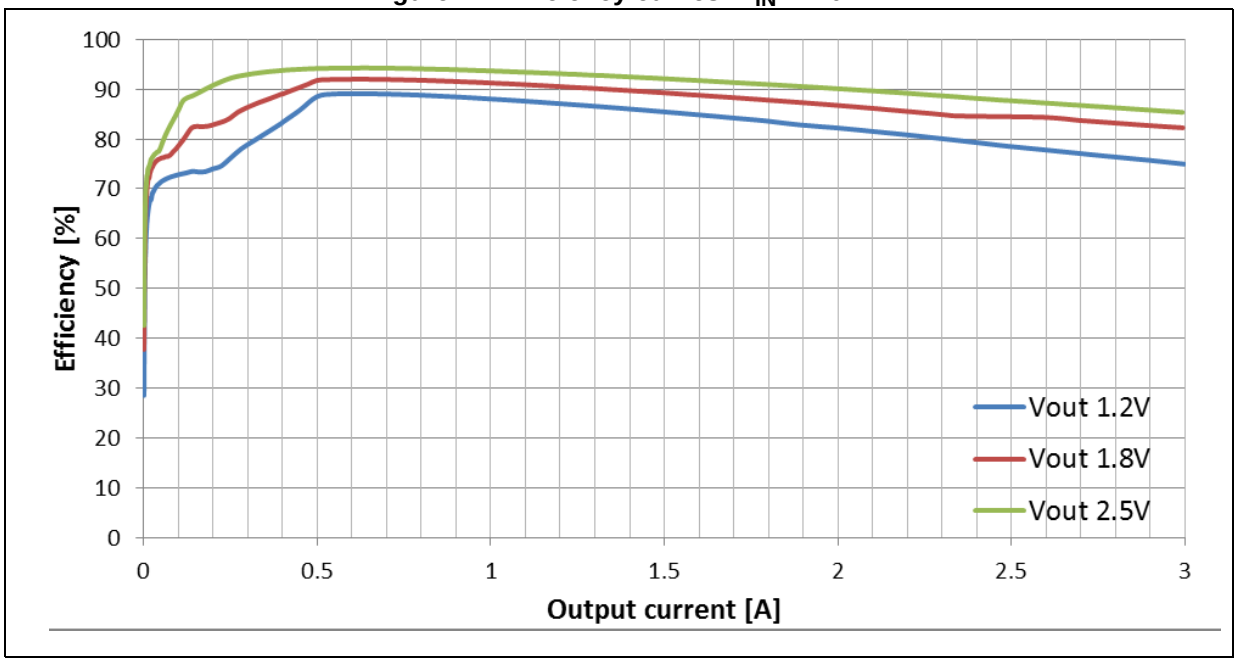


Figure 18. Efficiency curves: V_{IN} = 4.0 V (log scale)

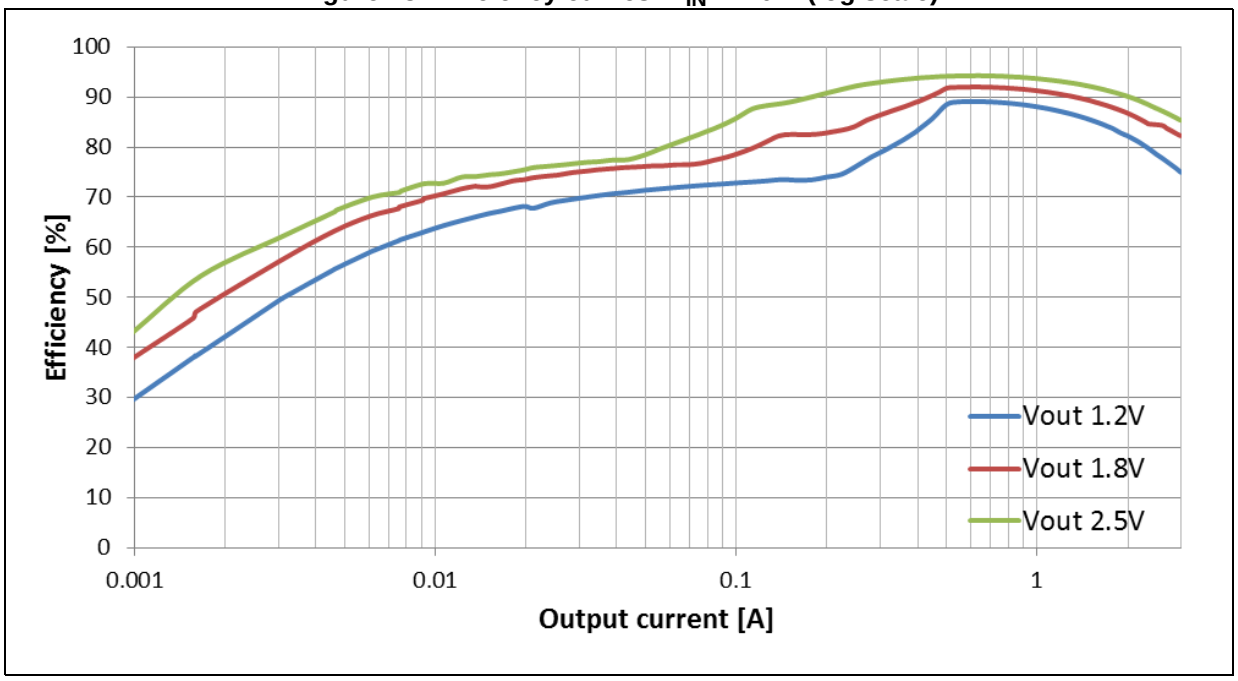


Figure 19. Load regulation (V_{IN} = 4.0 V)

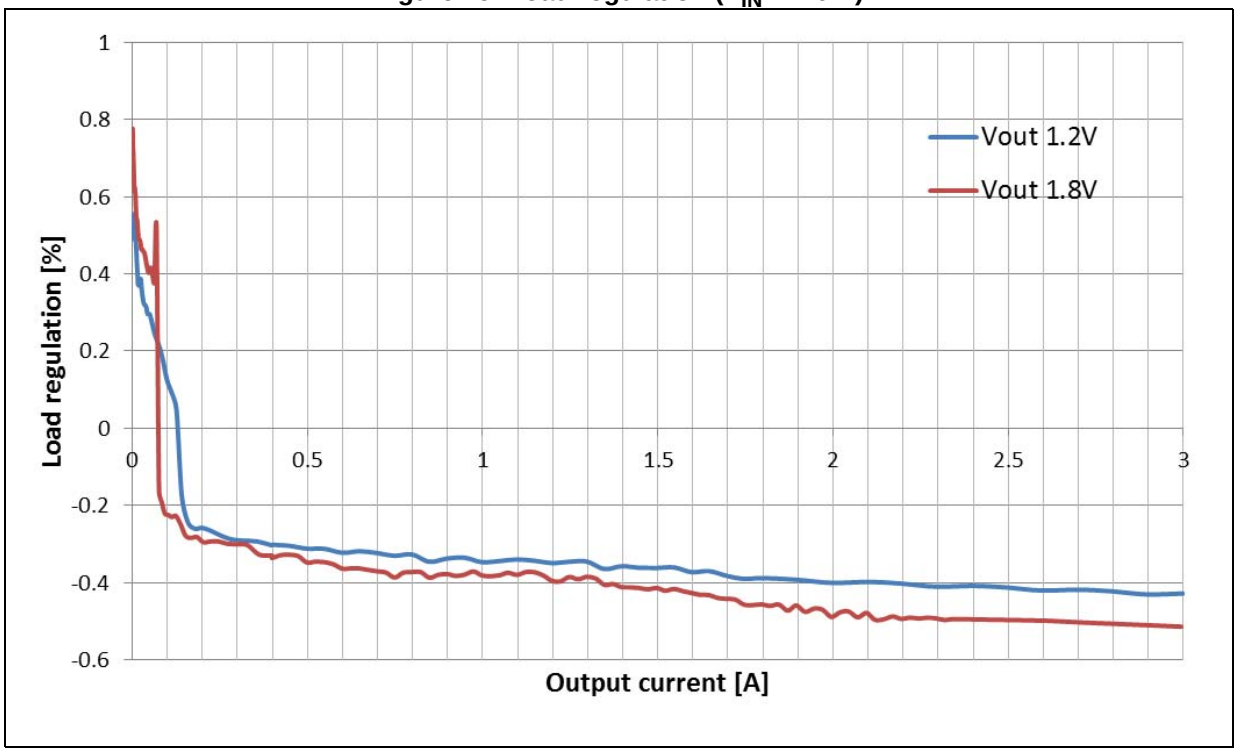


Figure 20. Efficiency curves: V_{IN} = 5.0 V

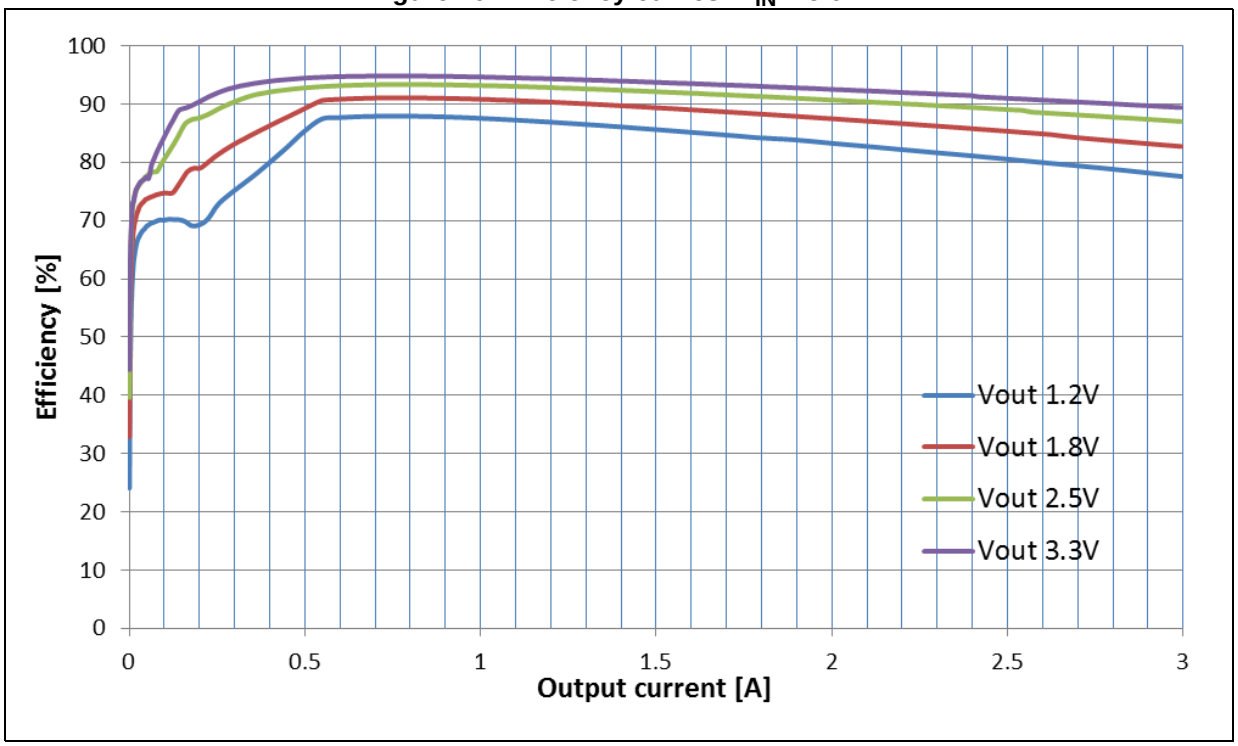


Figure 21. Efficiency curves: V_{IN} = 5.0 V (log scale)

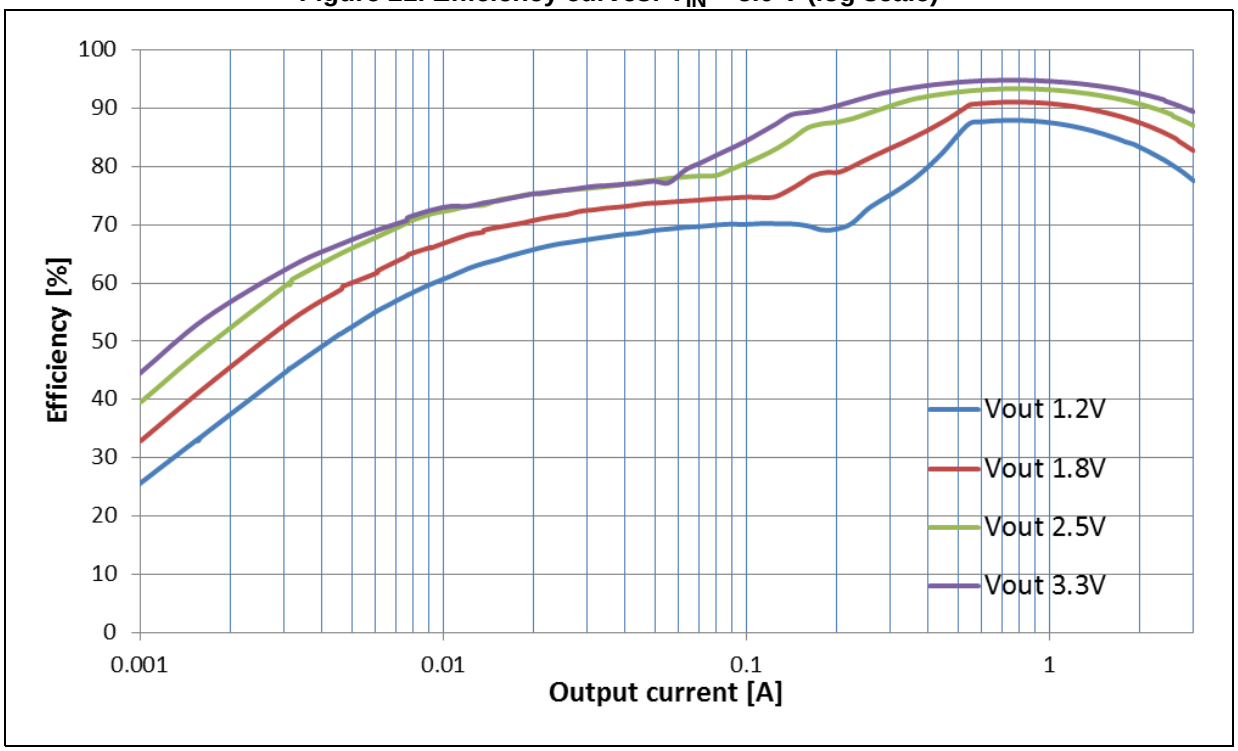


Figure 22. Load regulation (V_{IN} = 5.0 V)

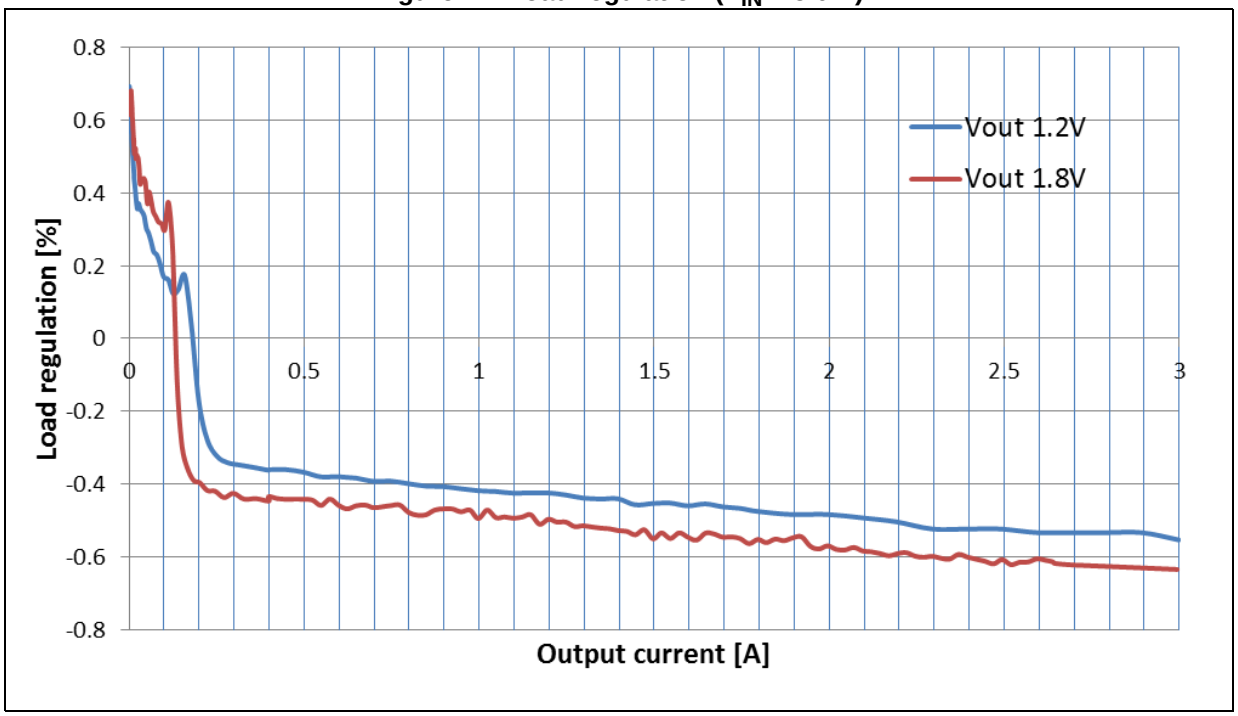
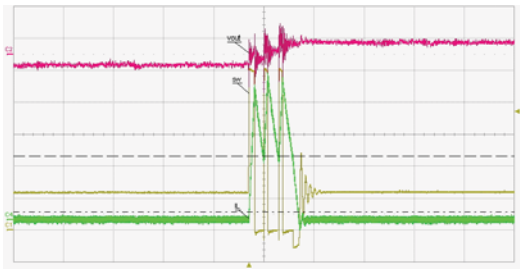


Figure 23. Zero load operation

V_{IN} =5V, V_{OUT} =1.2V, I_O=0A



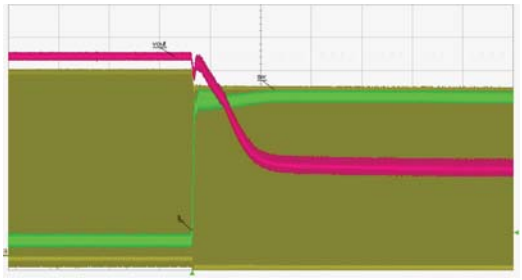
Green: IL (100mA/div)
Yellow: SW (1V/div)
Red: V_{OUT} (20mV/div)

Timescale 2us/div

AM11429v1

Figure 24. Overcurrent protection

V_{IN} =5.5V , V_{OUT} =1.2V, I_{LOAD} =0.5A -> 4.8A



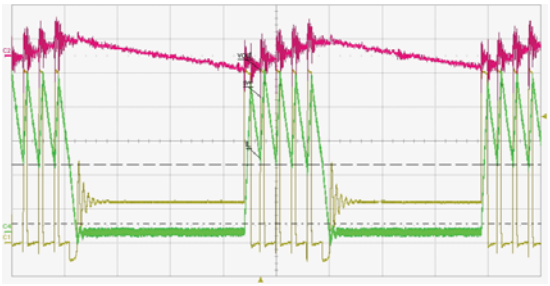
Green: IL (1A/div)
Yellow: SW (1V/div)
Red: V_{OUT} (200mV/div)

Timescale 100us/div

AM11430v1

Figure 25. 100 mA operation

V_{IN} =5V, VOUT=1.2V, IO=100mA



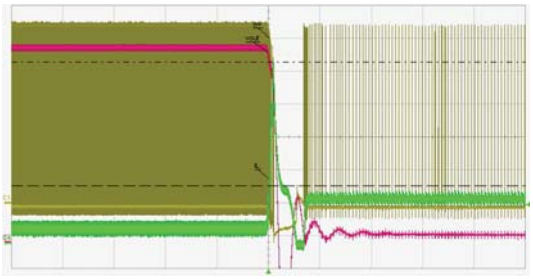
Green: IL (100mA/div)
Yellow: SW (1V/div)
Red: V_{OUT} (20mV/div)

Timescale 2us/div

AM11431v1

Figure 26. Short-circuit protection

V_{IN}=5.5V, V_{OUT}=1.2V



Green: IL (1A/div)
Yellow: SW (1V/div)
Red: V_{OUT} (200mV/div)

Timescale 50us/div

AM11430v1

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 VFDFPN 3 x 3 - 8L package information

Figure 27. VFDFPN 3 x 3 - 8L package outline

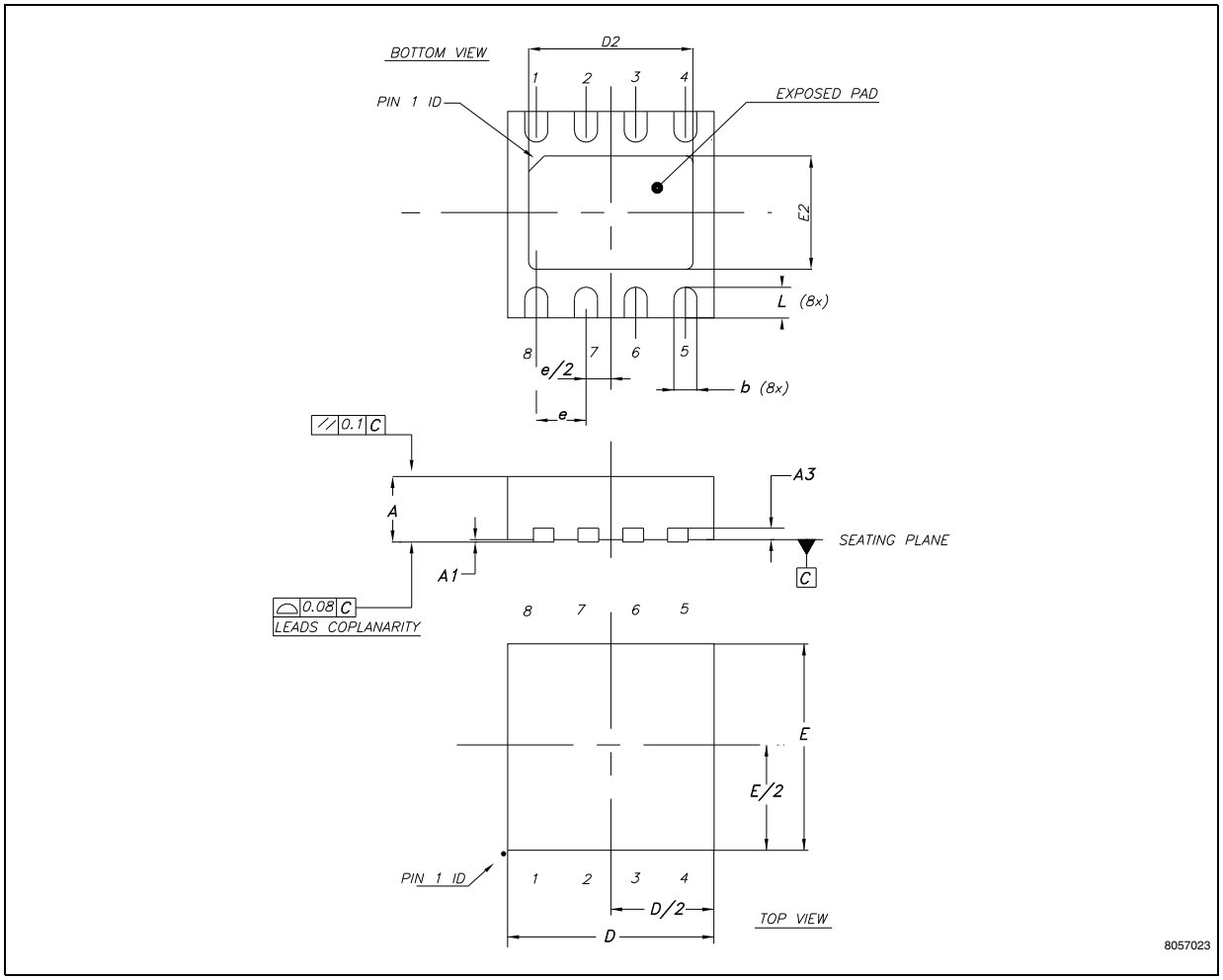
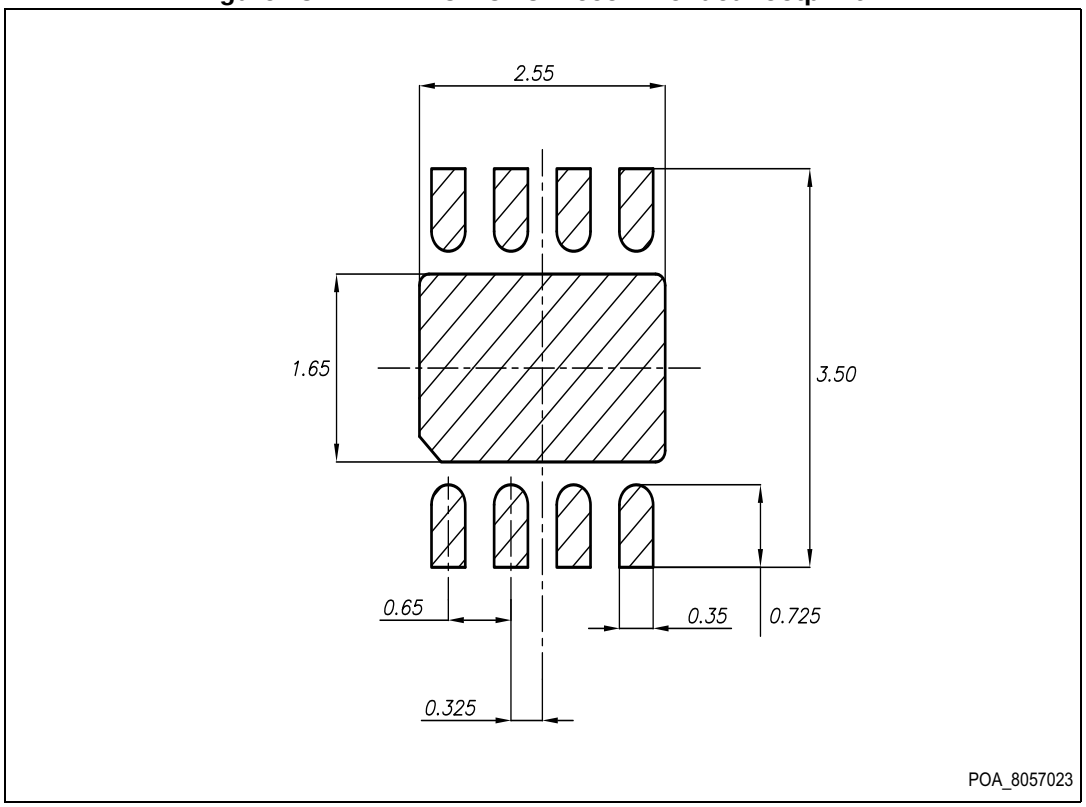


Table 10. VFDFPN 3 x 3 - 8L package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.0		0.05
b	0.25	0.30	0.35
D		3.00	
D2	2.234	2.384	2.484
E		3.00	
E2	1.496	1.646	1.746
e		0.65	
L	0.30	0.40	0.50

Figure 28. VFDFPN 3 x 3 - 8L recommended footprint(1)



1. Dimensions are in mm.

8.2 SO8 package information

Figure 29. SO8 package outline

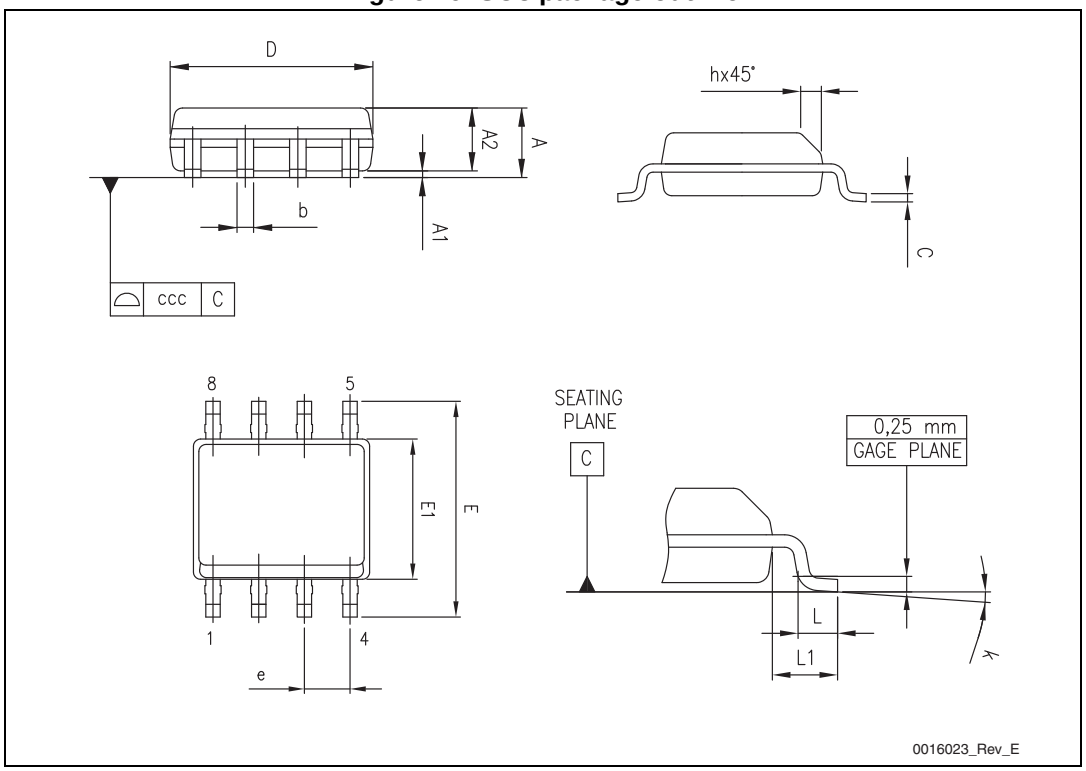


Table 11. SO8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

9 Order codes

Table 12. Ordering information

Order codes	Package
ST1S31PUR	VFDFPN 3 x 3 - 8 L
ST1S31D-R	SO8

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
12-Nov-2014	3	Updated Figure 2: Pin connection (top view) on page 3 (replaced by new figure). Minor modifications throughout document.
03-Mar-2016	4	Updated value in Table 3 on page 5 and Section 5.4 on page 19 (replaced 40 °C/W by 50 °C/W). Added Section 4.1 on page 9. Updated Section 7 on page 24 [added Figure 14 on page 24 to Figure 22 on page 28 (replaced figures 13 and 14)]. Minor modifications throughout document.
03-Aug-2018	5	Updated *Figure 1: Application circuit* on the cover page.