To : Mouser

Specification number:EQM08-1KC-E205K25

Date of issue: May 21, 2020

Multilayer ceramic Chip capacitor specification

Product Part No

CM03, CM05, CM105, CM21
(Refer to Part No.)

(Recipient stamp column)

Please send back with recipient stamp or signature here.

This specification would be invalidated unlesse sent back within a year after issue date of this specification.

RoHS Compliant

Kyocera Corporation
Capacitor Division

KYOCERA

No.	Date	Contents	PREPD.	CHKD.	CHKD.	APPD.
1	2020/05/21	NEW				

[Part No]

Characteristic	K/C Supplier Part No	Remarks
X5R	CM03X5R475M06AH055	
X6S	CM03X6S105M10AH	
X6S	CM03X6S105M06AH039	
X6S	CM03X6S105M04AH039	
X5R	CM05X5R226M06AH080	
X6S	CM05X6S226M04AH080	
X7S	CM05X7S105M04AH-HE	
X6T	CM105X6T475M16AT	
X6S	CM105X6S106M10AT	
X6T	CM105X6T226M04AT	
X6S	CM21X6S226M10AT	

1.Scope

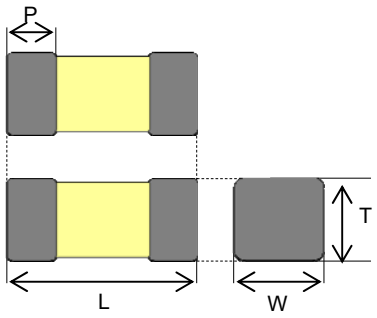
This specification sheet shall be applied to multilayer ceramic chip capacitors;Kyocera CM series.

2.Nomenclature

CM	□□	□□	□□□	□	□□	A	□	□□□
Series	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

(1) : Size
(2) : Temperature Characteristics
(3) : Capacitance
(4) : Tolerance
(5) : Rated Voltage
(6) : External Electrode
(7) : Packaging
(8) : Option (Thickness or Kyocera's Control Code)

(1)External Dimensions(Size)



External Dimension for Taping or Bulk (unit:mm)

Type	L	W	T	P
03	0.60±0.09	0.30±0.09	0.30±0.09	0.13~0.23
	0.60±0.09	0.30±0.09	0.50±0.05	0.13~0.23
05	1.00±0.05	0.50±0.05	0.50±0.05	0.15~0.35
	1.00±0.20	0.50±0.20	0.80MAX.	0.15~0.35
105	1.60±0.20	0.80±0.20	0.80±0.20	0.20~0.60
	1.60±0.25	0.80±0.25	0.80±0.25	0.20~0.60
21	2.00±0.20	1.25±0.20	1.25±0.20	0.20~0.75

(2)Temperature Characteristics

Characteristics	Applied voltage	Change in capacitance	Operating temperature range	Reference
X5R	No applied voltage	Within +/-15%	-55°C~+85°C	25°C
X6S	No applied voltage	Within +/-22%	-55°C~+105°C	25°C
X6T	No applied voltage	Within +22% / -33%	-55°C~+105°C	25°C
X7S	No applied voltage	Within +/-22%	-55°C~+125°C	25°C

(3)Capacitance Value

Capacitance is indicated by three numbers and a letter (see example as follows). The first and second digits indicate the first two significant figures,and the final digit is a base 10 logarithmic multiplier in picofarads.

(Ex.)

Code	Capacitance
105	1,000,000pF
106	10,000,000pF

(4)Tolerance

Code	M
Tolerance	±20%

(5)Rated Voltage

Code	04	06	10	16
Voltage	4Vdc	6.3Vdc	10Vdc	16Vdc

(6)Termination (External Electrode)

A: Nickel Barrier / Tin

(7)Packaging Configuration

Code	Packaging Configuration	Applying Size
H	Taping(2mm Pitch. Φ180 Reel)	Refer to Taping specification (CM03, CM05 size)
T	Taping(4mm Pitch. Φ180 Reel)	Refer to Taping specification

(8)Option

039 : 0.30±0.09mm *Apply to CM03X6S105M06AH039 and CM03X6S105M04AH039.
055 : 0.50±0.05mm *Apply to CM03X5R475M06AH055.
080 : 0.80mm MAX. *Apply to CM05X5R226M06AH080 and CM05X6S226M04AH080.
-HE : Kyocera's Control Code *Apply to CM05X7S105M04AH-HE.

3.Operating temperature range

Refer to Item 2-(2)

4.Specifications and Test Methods

(Table 1-1)

Item		Specification X5R, X6S, X6T, X7S	Measuring Conditions
Capacitance		Within specified tolerance value	High Temperature Treatment (Table 2) C≤10μF Measuring frequency 1kHz±10% Measuring voltage Refer to (Table 3) C>10μF Measuring frequency 120Hz±10% Measuring voltage Refer to (Table 3)
tanδ		Refer to (Table 3)	
(*1)Insulation Resistance		Refer to (Table 3)	Measure after charging with the rated voltage within 1 minutes at room conditions.
(*1)Dielectric Strength		No problem observed	Applying 2.5 times of the rated voltage for 1 to 5 seconds.
Appearance		No serious defect	Under Microscope
End Termination adherence		No evidence of peeling on the end termination	After soldering chip capacitors on glass epoxy boards and applying *5N(0.5Kgf) as shown by the arrow mark in the sketch peeling or any sign of peeling should not be found on end terminations. *2N:CM03 size (Refer to Fig.1)
Resistance to Vibration	Appearance	No serious defect	Perform High Temperature Treatment (Table 2) , then measure the initial capacitance and tanδ. Vibration frequency:10 to 55 (Hz) Swing width :1.5mm Sweep :10→55→10 Hz/1min x,y,z axis 2 hours/each Total 6 hours (Refer to Fig.2)
	Capacitance Variation	Within specified tolerance value	
	tanδ	Satisfies initial specified value	
Resistance to Solder Leaching	Appearance	No serious defect	Perform High Temperature Treatment (Table 2) , then measure the initial capacitance and tanδ. After dipped molten solder, at 260±5°C for 10±0.5 seconds and kept at room conditions for 24±2 hours, measure and check the specifications. *Pre-heat before immersion 1st: 80°C to 100°C for 120sec. 2st:150°C to 200°C for 120sec.
	Capacitance Variation	Within ±7.5%	
	tanδ	Satisfies initial specified value	
	(*1)Insulation Resistance	Within specified tolerance value	
	(*1)Dielectric Strength	Resist without problem.	
Solderability		Coverage >= 90% Each termination end	Soaking Condition <Sn-3Ag-0.5Cu> 245±5°C 3±0.5sec. <Sn63 Solder> 235±5°C 2±0.5sec.

(Table 1-2)

Item		Specification X5R, X6S, X6T, X7S	Measuring Conditions
Temperature Cycling	Appearance	No serious defect	Perform High Temperature Treatment (Table 2) , then measure the initial capacitance and tanδ. <Cycle> Room temperature (3 minutes) - Lowest operating temperature (30 minutes) – Room temperature (3 minutes) – Highest operating temperature (30 minutes). After 5 cycles of the above, keep at 150+0/-10°C for 1 hour and then let sit for 24±2 hours at room temperature, then measure. (Refer to Fig.2)
	Capacitance Variation	Refer to (Table 4)	
	tanδ	Satisfies initial specified value	
	(*1)Insulation Resistance	Refer to (Table 4)	
	(*1)Dielectric Strength	Resist without problem	
Load Humidity Resistance	Appearance	No serious defect	Perform High Temperature Treatment (Table 2) , then measure the initial capacitance and tanδ. Apply rated voltage for 500+12/-0 hours in pre-condition at 40±2°C, humidity 90% to 95%RH. After test , keep at 150+0/-10°C for 1 hour and then let sit for 24±2 hours at room temperature, then measure.
	Capacitance Variation	Refer to (Table 4)	
	tanδ	Less than 2 times of the initial value	
	(*1)Insulation Resistance	Refer to (Table 4)	
High Temperature Life Test	Appearance	No serious defect	Perform High Temperature Treatment (Table 2) , then measure the initial capacitance and tanδ. Apply voltage (Magnification of Applied voltage × Rated voltage) for 1000+12/-0 hours in pre-condition at the highest temperature. * Magnification of Applied voltage: refer to (Table 4) After test , keep at 150+0/-10°C for 1 hour and then let sit for 24±2 hours at room temperature, then measure.
	Capacitance Variation	Refer to (Table 4)	
	tanδ	Less than 2 times of the initial value	
	(*1)Insulation Resistance	Refer to (Table 4)	
Bending Strength		No mechanical damage	Refer to Fig.3-1, Fig.3-2 The glass epoxy board is bent up 1mm in 10 sec.

(*1) Insulation Resistance/Dielectric Strength;Charging or discharging current for these tests Is limited under 50mA.

(Table 2)

Initial Treatment	High Temperature Treatment	Keep chip capacitor at 150°C +0/-10°C for 1 hour,Then leave chip capacitor at room temperature and normal humidity for 24±2 hours.

[Table3 Parts List]

Product Part No	Dimension [mm]			tanδ [%]max	IR (initial) min	Capacitance / tanδ Measuring voltage
	L	W	T			
CM03X5R475M06AH055	0.60±0.09	0.30±0.09	0.50±0.05	15.0%	50 MΩ•μF	0.5±0.1Vrms
CM03X6S105M10AH	0.60±0.09	0.30±0.09	0.30±0.09	20.0%	50 MΩ•μF	1.0±0.2Vrms
CM03X6S105M06AH039	0.60±0.09	0.30±0.09	0.30±0.09	20.0%	50 MΩ•μF	1.0±0.2Vrms
CM03X6S105M04AH039	0.60±0.09	0.30±0.09	0.30±0.09	20.0%	50 MΩ•μF	1.0±0.2Vrms
CM05X5R226M06AH080	1.00±0.20	0.50±0.20	0.80MAX.	12.5%	50 MΩ•μF	0.5±0.1Vrms
CM05X6S226M04AH080	1.00±0.20	0.50±0.20	0.80MAX.	12.5%	50 MΩ•μF	0.5±0.1Vrms
CM05X7S105M04AH-HE	1.00±0.05	0.50±0.05	0.50±0.05	12.5%	50 MΩ•μF	1.0±0.2Vrms
CM105X6T475M16AT	1.60±0.20	0.80±0.20	0.80±0.20	12.5%	50 MΩ•μF	1.0±0.2Vrms
CM105X6S106M10AT	1.60±0.20	0.80±0.20	0.80±0.20	15.0%	50 MΩ•μF	1.0±0.2Vrms
CM105X6T226M04AT	1.60±0.25	0.80±0.25	0.80±0.25	12.5%	50 MΩ•μF	0.5±0.1Vrms
CM21X6S226M10AT	2.00±0.20	1.25±0.20	1.25±0.20	12.5%	50 MΩ•μF	0.5±0.1Vrms

[Table4 test specifications]

Product Part No	Temperature Cycling		Load Humidity Resistance		High Temperature Life Test		
	Capacitance Variation	IR (Minimum value)	Capacitance Variation	IR (Minimum value)	Voltage Bias [%]	Capacitance Variation	IR (Minimum value)
CM03X5R475M06AH055	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM03X6S105M10AH	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM03X6S105M06AH039	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM03X6S105M04AH039	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM05X5R226M06AH080	±7.5%	20 MΩ•μF	±12.5%	5 MΩ•μF	100%	±12.5%	5 MΩ•μF
CM05X6S226M04AH080	±7.5%	20 MΩ•μF	±12.5%	5 MΩ•μF	100%	±12.5%	5 MΩ•μF
CM05X7S105M04AH-HE	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	150%	±12.5%	10 MΩ•μF
CM105X6T475M16AT	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM105X6S106M10AT	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	150%	±12.5%	10 MΩ•μF
CM105X6T226M04AT	±7.5%	20 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF
CM21X6S226M10AT	±7.5%	50 MΩ•μF	±12.5%	10 MΩ•μF	100%	±12.5%	10 MΩ•μF

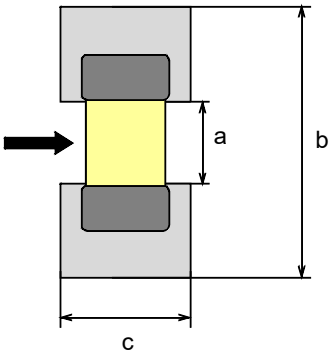


Fig.1 Substrate for adhesion strength test

type	a	b	c
03	0.26	0.92	0.32
05	0.4	1.4	0.5
105	1.0	3.0	1.2
21	1.2	4.0	1.65

glass epoxy board

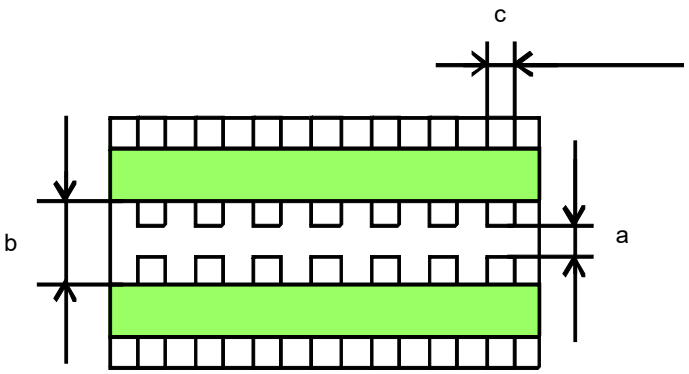
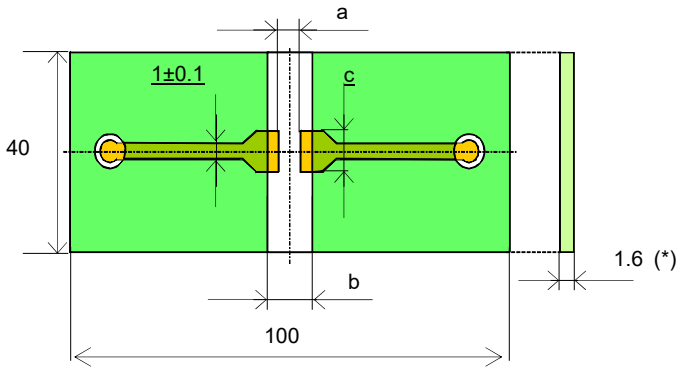


Fig.2 Substrate for temperature cycle test



* 0.8 : CM03,CM05 size

Fig.3-1 Substrate for bending test

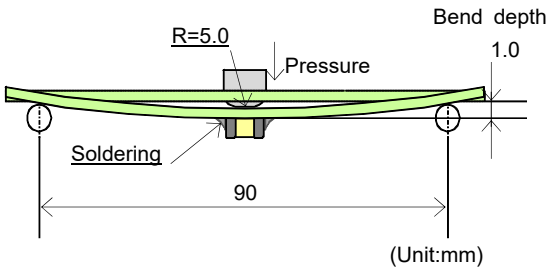
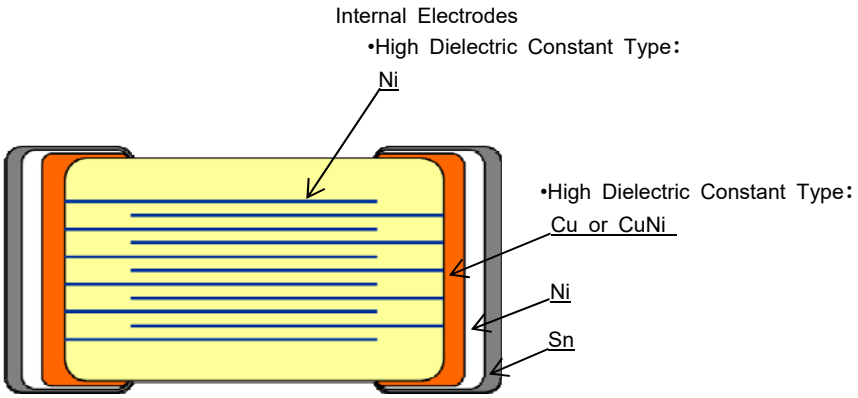


Fig.3-2 Testing status

[Structure]

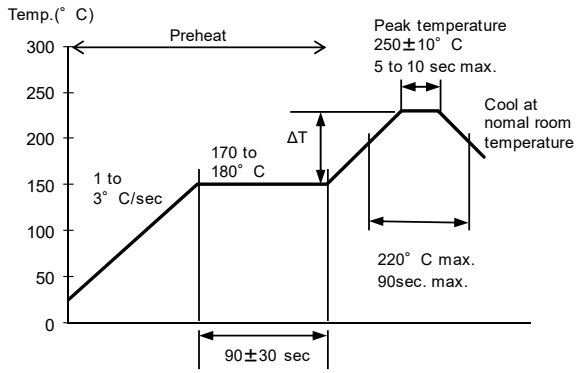


[Production facility]

Kagoshima Kokubu plant

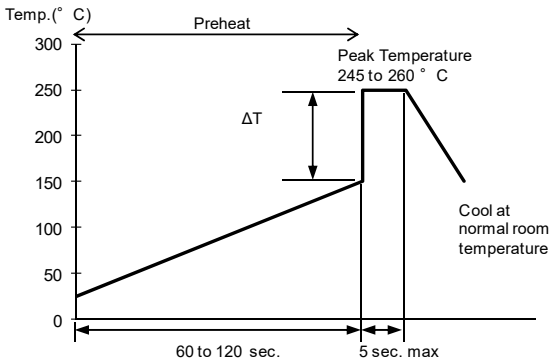
■For lead-free soldering　Recommended temperature profile

•Reflow porfile



(1) Minimize soldering time
(2) Ensure that the temperature difference does not exceed 150 °C.
(3) MLCC can withstand the above reflow conditions up to 3 times.
(4) Cool naturally after soldering.

•Flow profile



(1) Ensure that the chip capacitor is preheated adequately.
(2) Ensure that the temperature difference between a capacitor and the solder bath shall not exceed 150 °C.
(3) Cool naturally after soldering.
(4) Flow is not applicable for chips with size CM03, CM05.

Taping Specification

1.Application

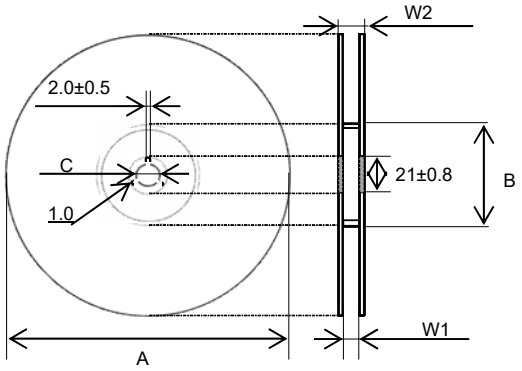
This specification applies to paper carrier tape of Kyocera multi-layer ceramic chip capacitor.

2.Packing unit

type	thickness (unit:mm)	material of carrier tape		width of carrier tape		Φ180 reel quantity per reel
		paper	Plastic	8mm	12mm	
03	0.30±0.09	○	-	○	-	15000
	0.50±0.05	○	-	○	-	10000
05	0.50±0.05	○	-	○	-	10000
	0.80 MAX.	○	-	○	-	10000
105	0.80±0.20	○	-	○	-	4000
	0.80±0.25	○	-	○	-	4000
21	1.25±0.20	-	○	○	-	3000

3.Shape and dimentions

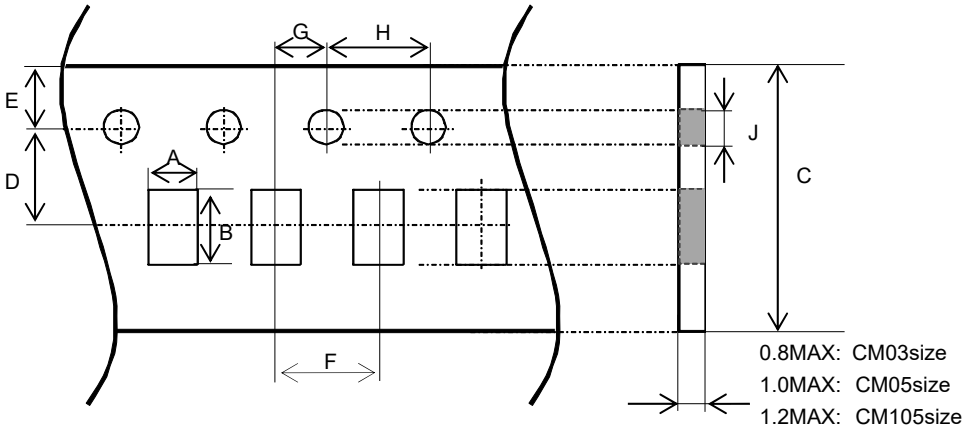
(1)Reel



[Dimension] Unit:mm

	A	B	C
Φ180 reel (Code:H,T)	Φ180+0/-2.0	Φ60min	Φ13.0±0.5
	W1	W2	
Φ180 reel (Code:H,T)	10.0±1.5	16.5max	

(2)-1 Carrier Tape

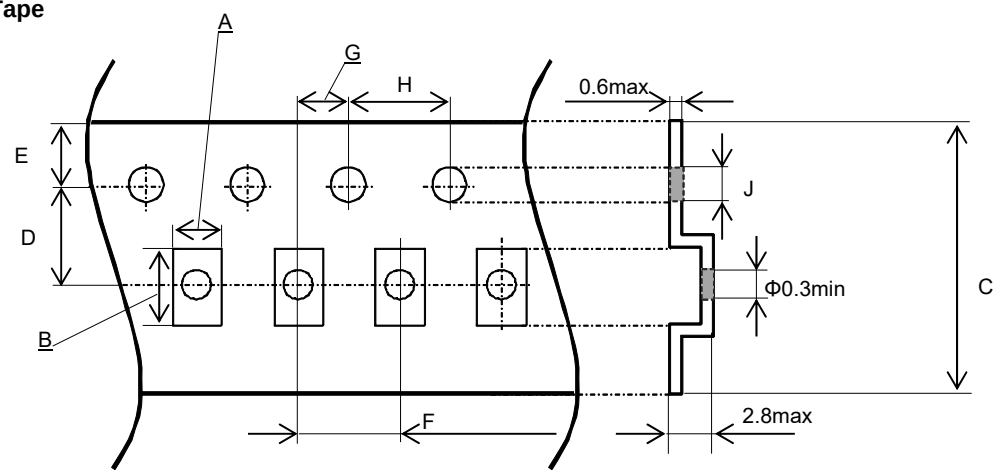


(unit:mm)

Code / Type \ Tolerance		A	B	C	D	E	F	G	H	J
		(*1)±0.03 (*2)±0.1 (*3)±0.2	(*1)±0.03 (*2)±0.1 (*3)±0.2	±0.3	±0.05	±0.1	±0.1	±0.05	±0.1	+0.1/-0
03	Thickness: 0.30±0.09mm	0.42	0.72	8.0	3.5	1.75	2.0	-	4.0	φ1.5
	Thickness: 0.50±0.05mm	0.44	0.74	8.0	3.5	1.75	2.0	-	4.0	φ1.5
05	Thickness: 0.50±0.05mm	0.65	1.15	8.0	3.5	1.75	2.0	-	4.0	φ1.5
	Thickness: 0.80mm MAX.	0.90	1.40	8.0	3.5	1.75	2.0	-	4.0	φ1.5
105	Thickness: 0.80±0.20mm	1.1	1.9	8.0	3.5	1.75	4.0	2.0	4.0	φ1.5
	Thickness: 0.80±0.25mm	1.2	2.0	8.0	3.5	1.75	4.0	2.0	4.0	φ1.5

(*1)Apply to CM03 size (except for CM03X5R475M06AH055).
(*2)Apply to CM03X5R475M06AH055 and CM05 size.
(*3)Apply to CM105 size.

(2)-2 Carrier Tape



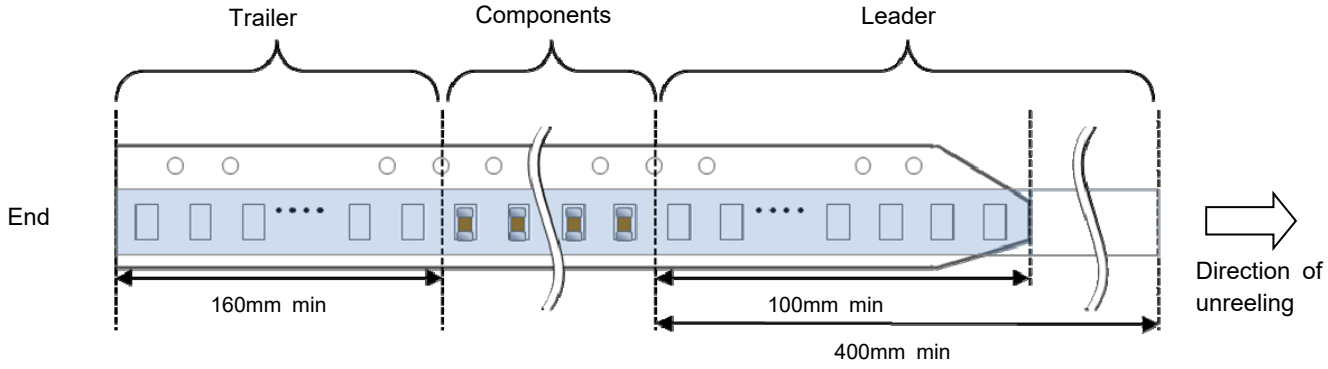
(unit:mm)

Code / Tolerance / Type	A	B	C	D	E	F	G	H	J
	±0.2	±0.2	±0.3	±0.05	±0.1	±0.1	±0.05	±0.1	+0.1/-0
21	1.5	2.3	8.0	3.5	1.75	4.0	2.0	4.0	φ1.5

4.Packing method

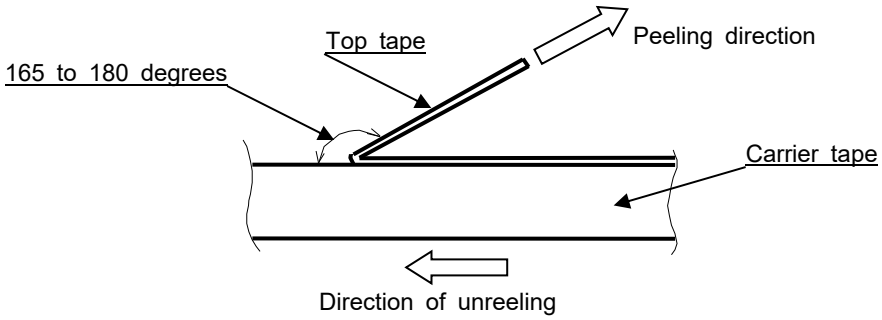
(1)Details of leader and trailer

①The tape will have a empty pocket at the leader and trailer of carrier tape.
②The tape end will not be stucked by glue in order to make it easier to peel off from reel.
③The feeding round hole will be on the right side against t leading direction.



(2)Heat pressure tape

①Peeling strength to be *0.1~0.7N when peeling off the top tape by following method.
②When peeling top tape off, the glue will be stuck to the top tape side.
③Chip capacitor will not stuck on heat pressure tape and will be free in the cavity.



The peel-off angle:165~180 degree against the surface of carrier tape.
The peel-off speed:300mm/min.

(3)Carrier tape

①Chip will not fall off from carrier tape or carrier tape will not be damaged by bending than within aradius of 25mm.
②The chip are inserted continuously without any empty pocket.
③Chip will not be mis-mounted because of too big clearance between components and cavity. Also the waste of carrier tape will not fill a nozzle hole of mouting machine.

5.Indication and packing

①There will be following indication on one side of the reel: “PART NUMBER”,”LOT NUMBER”, “QUANTITY”,”DATE OF MANUFACTURE”,”CUSTOMER’S NAME”
②There will be following indication on the reel box: “PART NUMBER”,”LOT NUMBER”, ”QUANTITY OF REEL”,”DATE OF MANUFACTURE”,”CUSTOMER’S NAME”
③We adequately pack the box to prevent chip capacitor from any mechanical damage during transportation.

Precautions

■ Handling

1) Cracks may occur unless otherwise avoiding excessive stress to the capacitors by the load of an adsorption nozzle,and bending of a substrate at the time of mounting.
2) Please arrange the capacitor position where they don't have too much stress of board bending after mounting.
3) Please design that the form and size of the land pattern has suitable solder amount.
Otherwise cracks may occur. The recommended fillet height shall be 1/2 to 1/3 of the thickness of capacitors.

■ Circuit Design

1) When AC voltage is superimposed on DC voltage, the zero-to-peak voltage shall not exceed the rated voltage. When the capacitor is to be employed in a circuit in which there is continuous application of a high frequency Voltage or a steep pulse voltage, even though it is within the rated voltage, please inquire to the manufacturer.
2) Please use the capacitor below the maximum temperature.
When using the capacitor in a self-heating AC circuit, please make sure the surface of the capacitor remains under the maximum temperature for usage. Also, please make certain temperature rises remain below 20 °C.

■ Resin coating

Please use the resin of low curing shrinkage type. (Otherwise cracks may occur).

■ Storage

1) When the components is stored in minimal packaging (a heat-sealed or chuck-type plastic bag), the bag should be kept closed. Once the bag has been opened, reseal it or store it in a desiccator.
2) Keep storage place temperature +5 to +40 °C, humidity 20 to 70% RH.
3) The storage atmosphere must be free of gas containing sulfur and chlorine. Also, avoid exposing the product to saline moisture. If the product is exposed to such atmospheres, the terminals will oxidize and solderability will be effected.
4) Precautions 1) to 3) apply to chip capacitors packaged in carrier tapes and bulk cases.
5) The solderability is assured for 6 months from our shipping date if the above storage precautions are followed.

■ Application Restriction

Please consult with us before using a capacitor in the equipment which requires a high degree reliability (medical equipment, aerospace applications, nuclear equipment.) Malfunctions in medical, space, nuclear power or other vital equipment may result in death or great social losses. Capacitors designed specially with high reliability are used for the equipment above.

■ Export regulation

When the applying products relate the strategic materials which are provided in Foreign Exchange and Foreign Trade Act and Foreign Trade Management Law, the export license based on these laws are required.

■ Disposal

Please dispose the capacitors according to the relating laws about the waste treatment and cleaning.
Safety application guideline and detailed information of electrical properties are also provided in Kyocera home page:
URL: http://www.kyocera.co.jp/electronic

Notice:

This specification shall guarantee only monolithic capacitors. Please make sure the performance of capacitors after mounted on the assembled product.
Any failures occurred being used out of this specification shall not be quaranteed.
This specification shall be applied to the products purchased through the regular sales routes, such as the sale offices, the subsidiaries and the distributors, etc.).