Si8239x-EVB User's Guide

The Si8239x isolated gate drivers are ideal for driving power switches used in a wide variety of power supply, inverter, and motor control applications, offering longer service life and dramatically higher reliability compared to opto-coupled gate drivers. The Si8239x isolated gate drivers utilize Silicon Laboratories' proprietary silicon isolation technology supporting up to 5 kVRMS withstand voltage per UL1577 and VDE0884. This technology enables industry-leading common-mode transient immunity (CMTI), tight timing specifications, reduced variation with temperature and age, better part-to-part matching, and very high reliability. It also offers unique features, such as driver shutdown on UVLO fault and precise dead time programmability. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage.

The extended range inputs (2.5 to 5.5 V) are available in individual control input (Si82390/1/5/6/7) or PWM input (Si82394/8) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

The Si8239x evaluation board allows designers to evaluate Silicon Lab's Si8239x family of ISOdrivers. Screw terminals are provided to allow for quick evaluation of the devices' key parameters. Test points are also included on each of the device's pins to accommodate direct connection to the designer's end system. In addition, jumpers are included to allow for manual setting of the devices input as well as the boot strap circuitry on the output if desired. The boards come populated with the Si82394 version of the family. However, JP2 (VIB) is still provided should the user wish to replace the Si82394 with one of the dual input versions of the device. For more ISOdriver information, visit Silicon Labs web site at www.silabs.com/isolation. The product data sheet and numerous application notes can be referenced to help facilitate designs.

KEY FEATURES

- Screw terminals for easy connection to power supplies
- Test points on each pin for easy connection to test equipment
- Boot strap circuitry selectable by jumper
- Jumpers for easy manual control of input signals

1. Kit Contents

The Si8239x Evaluation Kit contains the following items:
- Si8239x-based evaluation board shown in the figure below
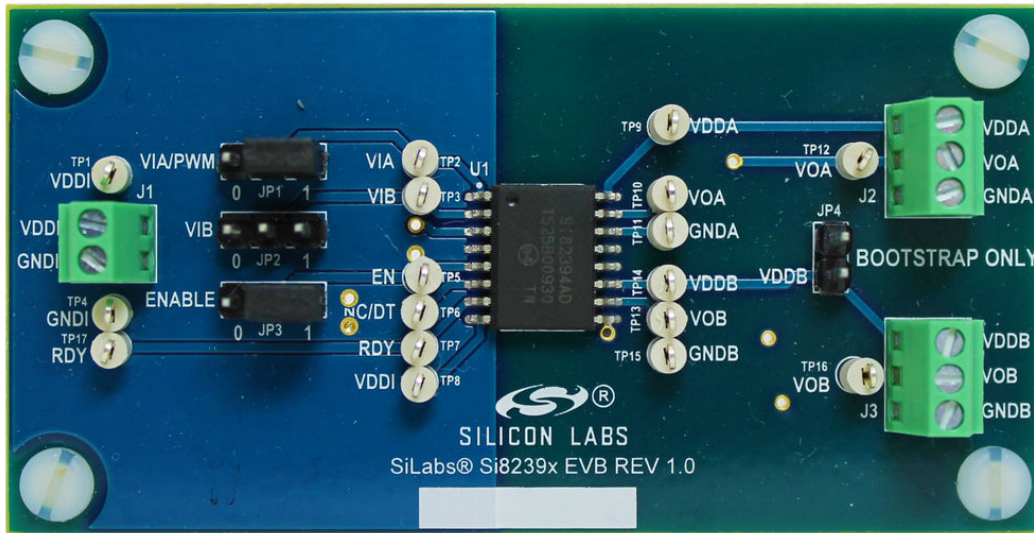- Si82394, PWM input, 4 A, 5 kVrms High-Side/Low-Side ISOdriver
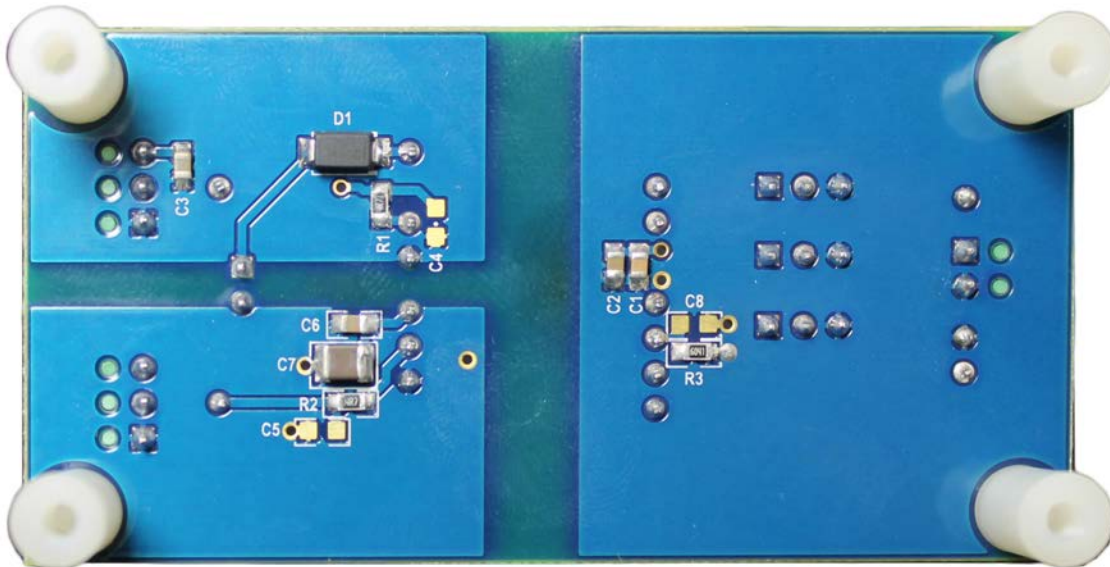
Figure 1.1. Si8239x Evaluation Board Front

Figure 1.2. Si8239x Evaluation Board Back

1.1 Required Equipment

The following equipment is required to demonstrate the evaluation board:
- 1 digital multimeter
- 1 dc power supply 15 Vdc, 0–100 mA or equivalent)
- 1 dc power supply 3.3 Vdc, 0–100 mA or equivalent)
- Si8239x Evaluation Board (board under test)
- Si8239x Evaluation Board Test Procedure (this document)

2. Si8239x ISOdriver Board Setup and Test

2.1 DC Supply Configuration

1. Verify the 3.3 V power supply output before connecting to EVB. Disable supply output before connecting to evaluation board.
2. Connect the positive rail of the 3.3 V supply to J1 pin 1 (labeled VDDI) or to TP1.
3. Connect the negative rail of the 3.3 V supply to J1 pin 2 (labeled GNDI) or TP4.
4. Turn ON the 3.3 V supply.
5. Verify the 15 V power supply output before connecting to EVB. Disable supply output before connecting to evaluation board.
6. Connect the positive rail of the 15 V supply to J2 pin 3 (labeled VDDA) or to TP9.
7. Connect the negative rail of the 15 V supply to J2 pin 1 (labeled GNDA) or TP11.
8. Turn ON the 15 V supply.

2.2 Test Channel A

1. Add shunt between pins 1 and 2 on JP1 and JP3.
2. Using the DMM verify a logic 1 on TP10 with respect to TP11 (POS on TP10, NEG on TP11).
3. Move shunt to pins 2 and 3 on JP1.
4. Using DMM, verify logic 0 on TP10 with respect to TP11.

2.3 Test Channel B

1. Turn off 15 V supply.
2. Move the 15 V positive rail to J3 pin 3 or TP14.
3. Move the 15 V negative rail to J3 pin 1 or TP15.
4. Turn on 15 V supply.
5. Using DMM, verify a logic 1 on TP13 with respect to TP15.
6. Move the shunt on JP1 back to pins 1–2.
7. Using DMM, verify a logic 0 on TP13 with respect to TP15.

Note: A signal generator can be used to supply a clock signal to JP1 pin 2 instead of using the shunt.

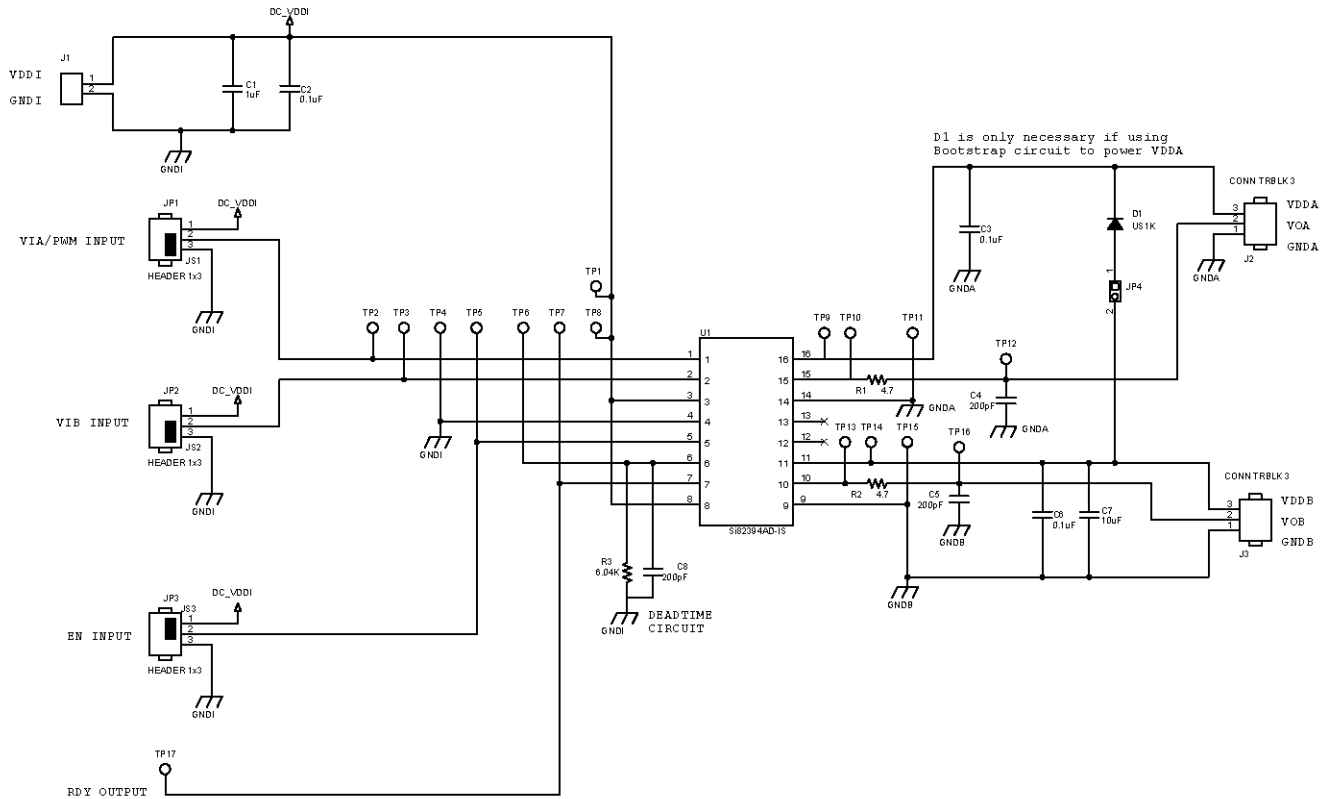# 3. Si8239x-EVB Schematics, Silkscreens, and Layout
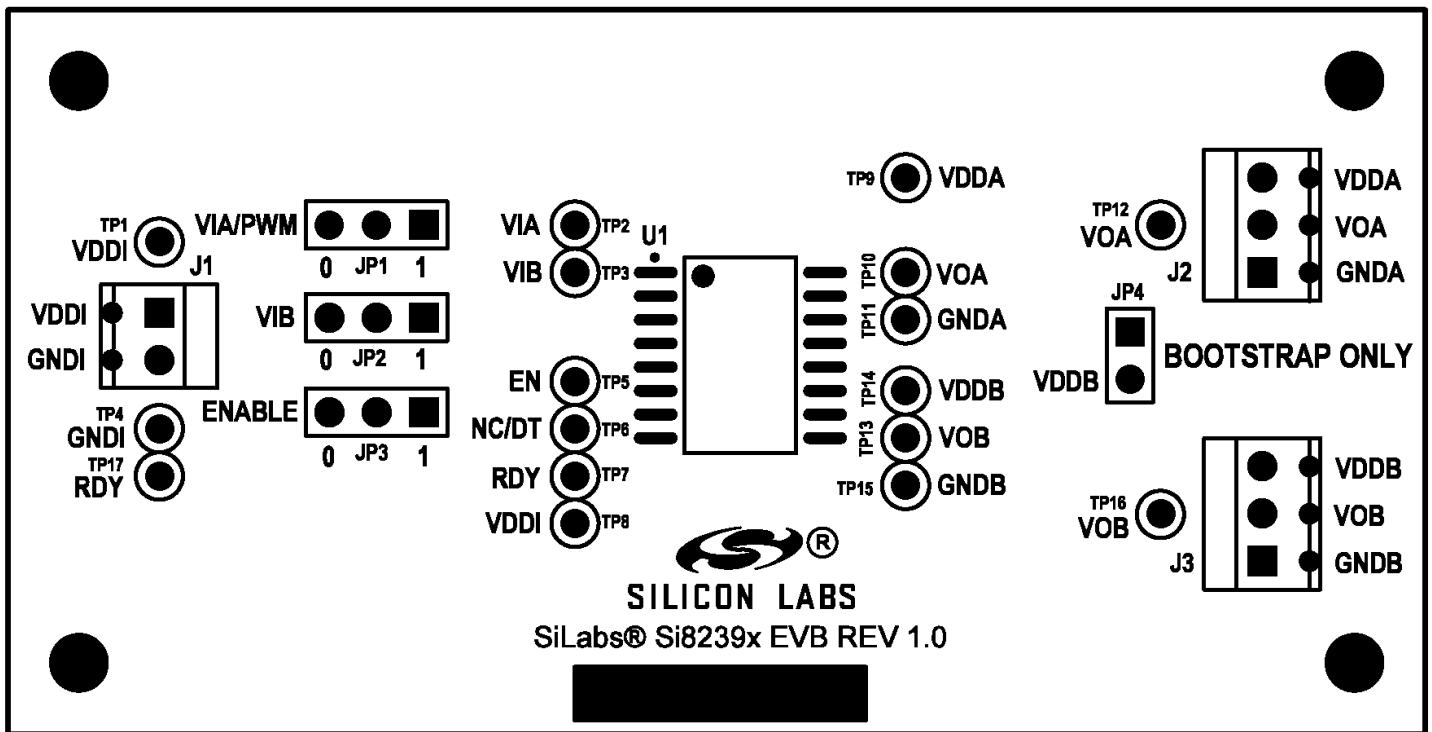

Figure 3.1. Si8239x Evaluation Board Schematic
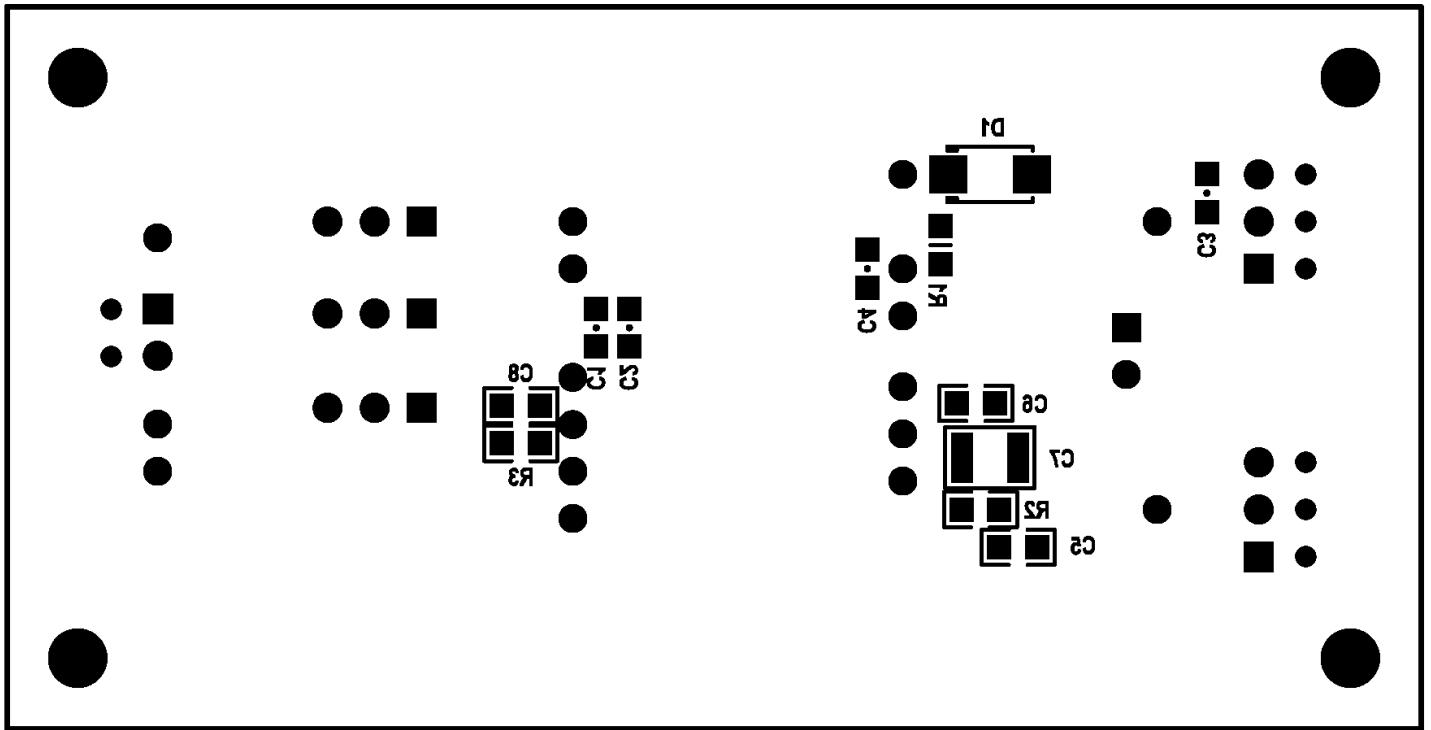

Figure 3.2. Si8239x-EVB Primary Silkscreen

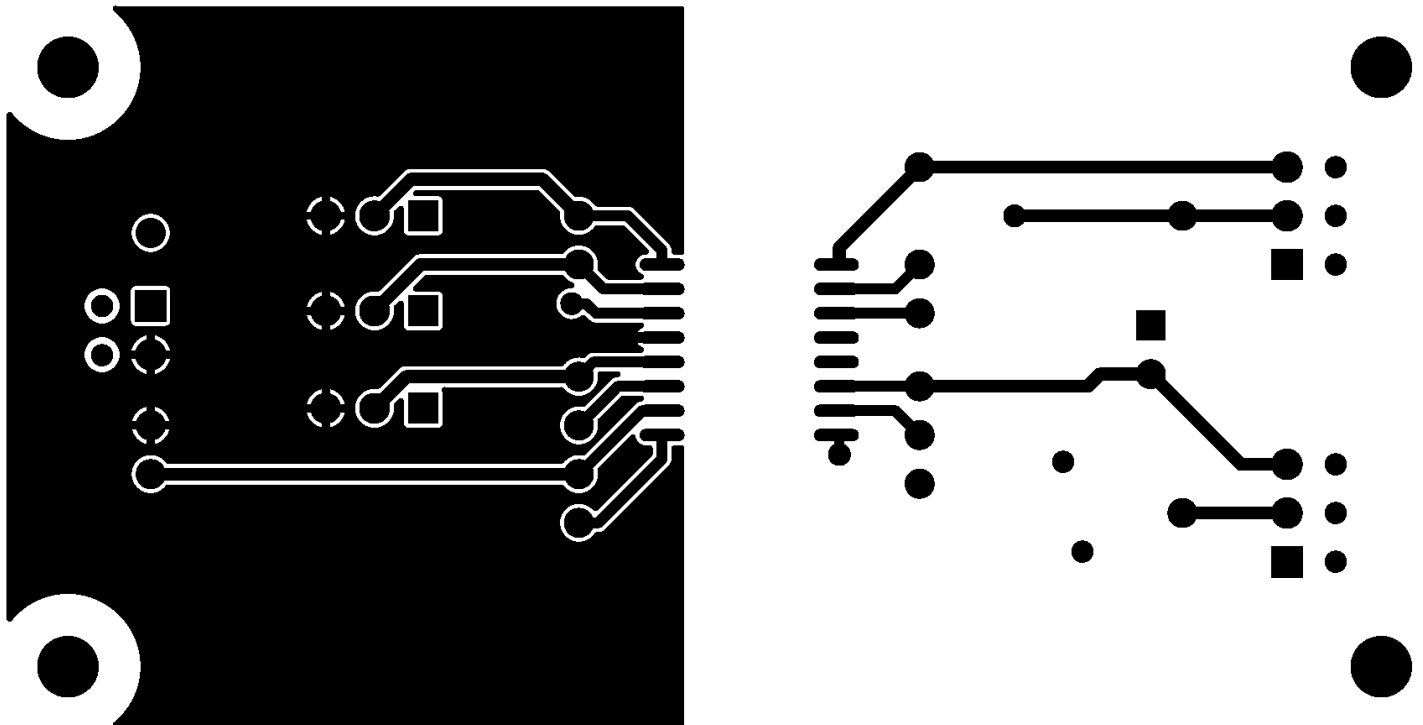**Figure 3.3. Si8239x-EVB Secondary Silkscreen**

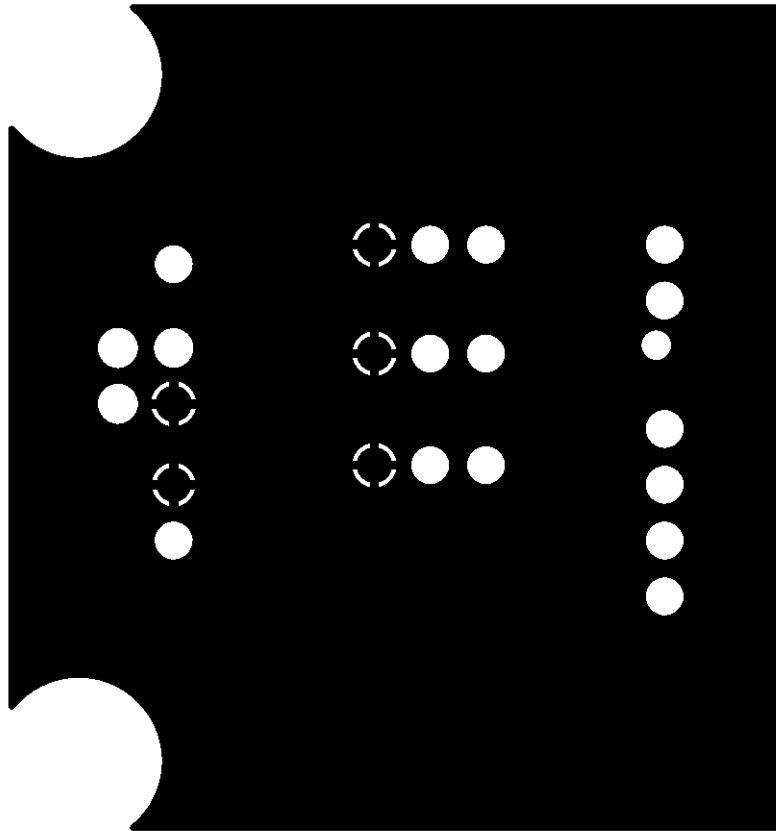
Figure 3.4. Si8239x-EVB Primary Side

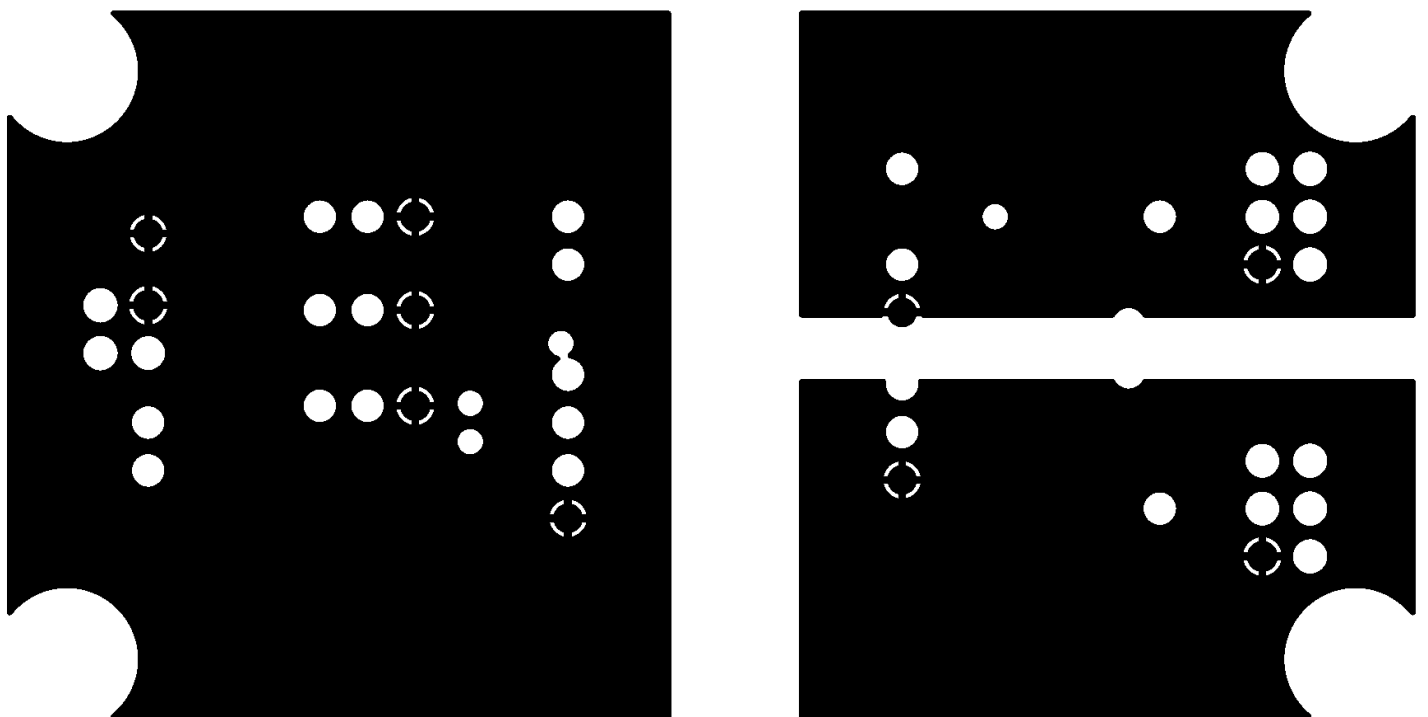**Figure 3.5. Si8239x-EVB Layer 2 Ground Plane**
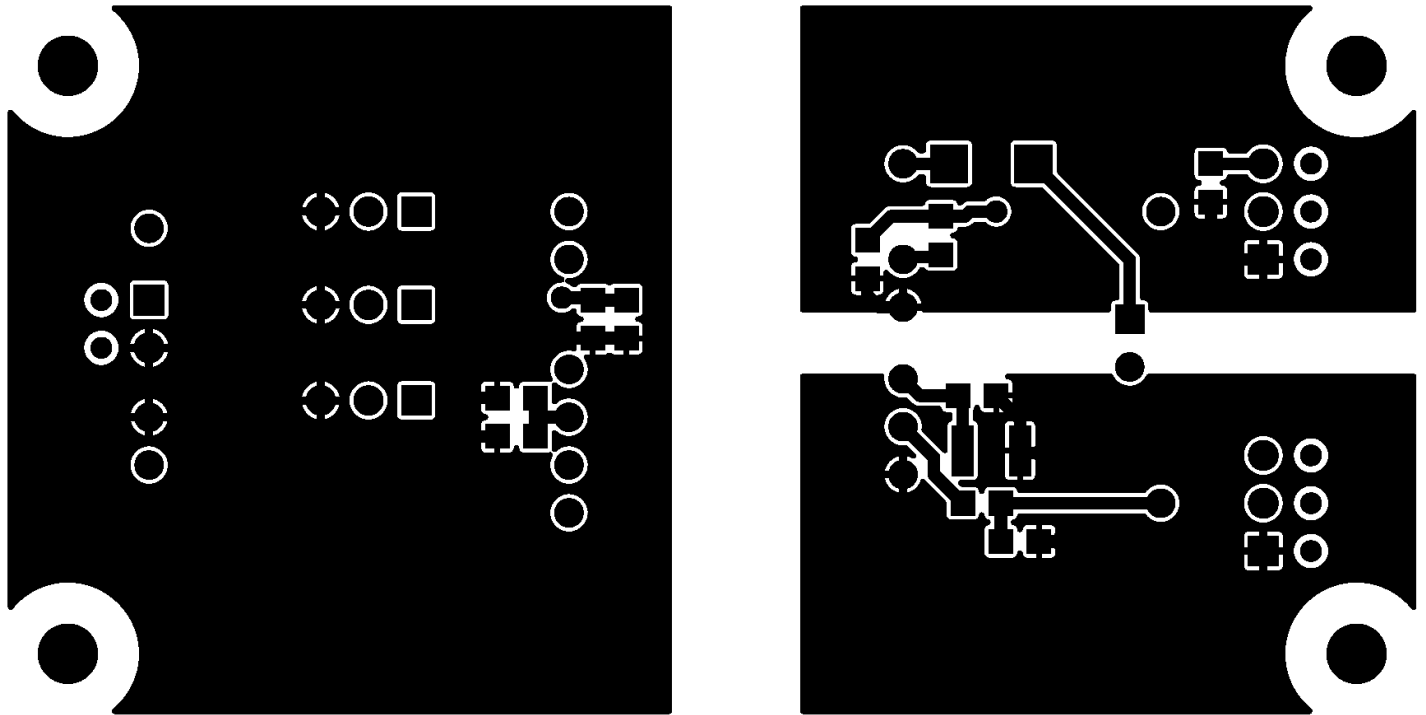

Figure 3.6. Si8239x-EVB Layer 3 Power Plane

Figure 3.7. Si8239x-EVB Secondary Side

4. Bill of Materials

Table 4.1. Si8239x-EVB Bill of Materials

Item Number	Quantity	Value	Part Number	Manufacturer
1	1	1 µF	C1	Samsung
2	3	0.1 µF	C2, C3, C6	Venkel
3	1	10 µF	C7	Murata Electronics North America
4	1	US1K	D1	Diodes Inc.
5	1	CONN TRBLK 2	J1	Phoenix Contact
6	2	CONN TRBLK 3	J2, J3	Phoenix Contact
7	3	Header 1x3	JP1, JP2, JP3	Samtec
8	1	Jumper	JP4	Samtec
9	3	Jumper Shunt	JS1, JS2, JS3	Samtec
10	4	Screw/Standoff	MH1, MH2, MH3, MH4	Various
11	1	Si8239x_EVB Rev 1.0	PCB1	SiLabs
12	2	4.7 W	R1, R2	Venkel
13	1	6.04 kW	R3	Venkel
14	17	White	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17	Kobiconn
15	1	Si82394AD-IS	U1	Silicon Labs
Not Installed				
16	3	200 pF	C4, C5, C8	Venkel
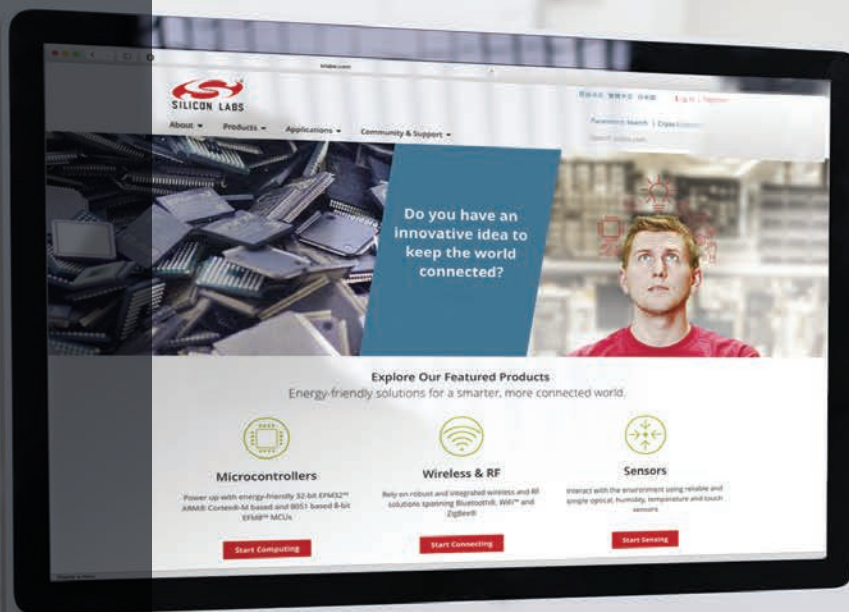
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Connected.
Energy-Friendly**

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