AiP74HC/HCT595
8-bit Serial-in, Serial or Parallel-out Shift Register with Output Latches; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2019-06-A1	2019-06	New
2021-09-A2	2021-09	Modify Ordering Information

1、General Description

The AiP74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For AiP74HC595: CMOS level
  For AiP74HCT595: TTL level
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- Specified from -40℃ to +85℃
- Packaging information: DIP16/SOP16/TSSOP16

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Ordering Information:

Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
AiP74HC595DA.TB	DIP16	74HC595	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT595DA.TB	DIP16	74HCT595	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC595SA.TB	SOP16	74HC595	50 PCS/tube	200 tube/box	10000 PCS/box	5 box/pack	50000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HCT595SA.TB	SOP16	74HCT595	50 PCS/tube	200 tube/box	10000 PCS/box	5 box/pack	50000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC595TA.TB	TSSOP16	74HC595	92 PCS/tube	100 tube/box	9200 PCS/box	10 box/pack	92000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT595TA.TB	TSSOP16	74HCT595	92 PCS/tube	100 tube/box	9200 PCS/box	10 box/pack	92000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Type number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Packing quantity	Notes
AiP74HC595SA.TR	SOP16(1)	74HC595	2500 PCS/reel	5000 PCS/box	20000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HCT595SA.TR	SOP16(1)	74HCT595	2500 PCS/reel	5000 PCS/box	20000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HC595SA.TR	SOP16(2)	74HC595	2500 PCS/reel	2500 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HCT595SA.TR	SOP16(2)	74HCT595	2500 PCS/reel	2500 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HC595TA.TR	TSSOP16	74HC595	2500 PCS/reel	5000 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
AiP74HCT595TA.TR	TSSOP16	74HCT595	2500 PCS/reel	5000 PCS/box	40000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

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2、Block Diagram And Pin Description

2.1、Block Diagram

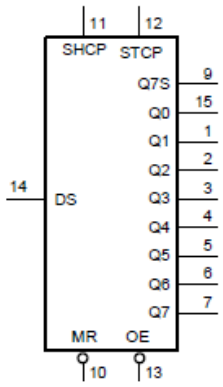


Figure 1. Logic symbol

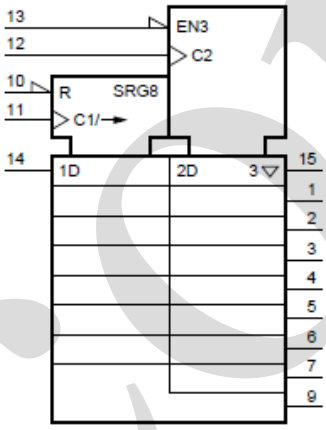


Figure 2. IEC logic symbol

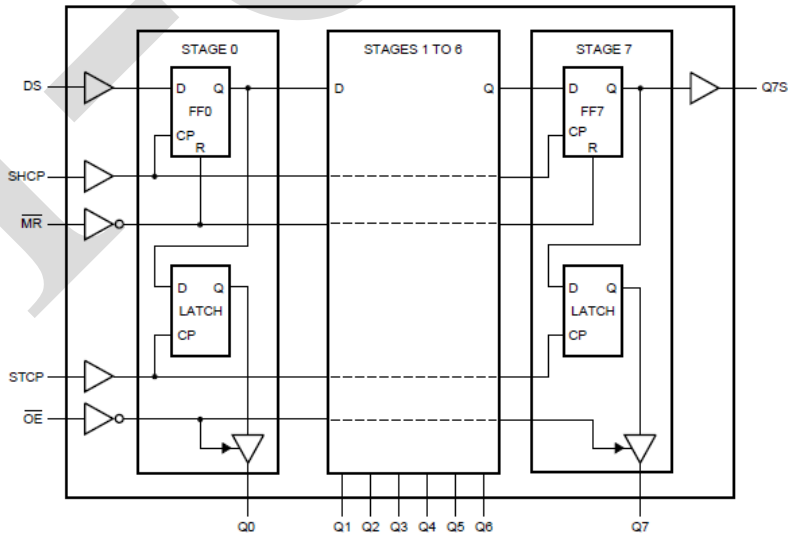


Figure 3. Logic diagram

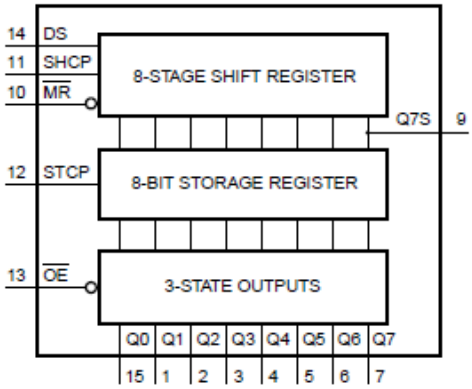
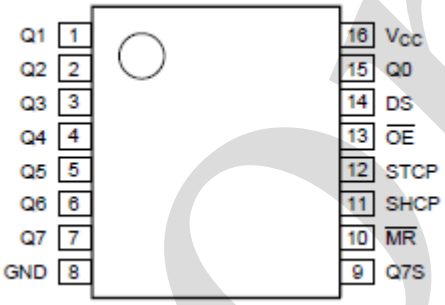


Figure 4. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0V)
9	Q7S	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SHCP	shift register clock input
12	STCP	storage register clock input
13	$\overline{OE}$	output enable input (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	supply voltage

2.4、Function Table

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;
↑=LOW-to-HIGH transition; X=don't care; NC=no change.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)	pin Q7S	-	±25	mA
			pins Qn	-	±35	mA
supply current	I_{CC}	-		-	70	mA
ground current	I_{GND}	-		-70	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

[1] For DIP16 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP16 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC595						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃
AiP74HCT595						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-	-40	-	+85	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC595							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs; I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			all outputs; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			all outputs; I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	-	V

LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
input capacitance	C_I	-		-	3.5	-	pF
AiP74HCT595							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}; V_{CC}=4.5V	all outputs; I_O=-20uA	4.4	4.5	-	V
			Q7S output; I_O=-4.0mA	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-6.0mA	3.7	4.32	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}; V_{CC}=4.5V	all outputs; I_O=20uA	-	0	0.1	V
			Q7S output; I_O=4.0mA	-	0.15	0.33	V
			Qn bus driver outputs; I_O=6.0mA	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	150	675	uA
			pin DS	-	25	113	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC595							
propagation delay	t_{pd}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	52	160	ns
			V_{CC}=4.5V	-	19	32	ns
			V_{CC}=6.0V	-	15	27	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	55	175	ns
			V_{CC}=4.5V	-	20	35	ns
			V_{CC}=6.0V	-	16	30	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	47	175	ns
			V_{CC}=4.5V	-	17	35	ns
			V_{CC}=6.0V	-	14	30	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 10	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=6.0V	-	14	26	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 10	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	27	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns
			V_{CC}=6.0V	13	5	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	75	11	-	ns
			V_{CC}=4.5V	15	4	-	ns
			V_{CC}=6.0V	13	3	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns
			V_{CC}=6.0V	13	5	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	50	11	-	ns
			V_{CC}=4.5V	10	4	-	ns
			V_{CC}=6.0V	9	3	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	75	22	-	ns
			V_{CC}=4.5V	15	8	-	ns
			V_{CC}=6.0V	13	7	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	50	-19	-	ns
			V_{CC}=4.5V	10	-7	-	ns
			V_{CC}=6.0V	9	-6	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	9	30	-	MHz
			V_{CC}=4.5V	30	91	-	MHz
			V_{CC}=6.0V	35	108	-	MHz
power dissipation capacitance	C_{PD}	all 9 outputs switching; f_i=1MHz; V_I=GND to V_{CC}		-	115	-	pF

AiP74HCT595; V_{CC}=4.5V to 5.5V						
propagation delay	t_{pd}	SHCP to Q7S; see Figure 6	-	25	42	ns
		STCP to Qn; see Figure 7	-	24	40	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	-	23	40	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 10	-	21	35	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 10	-	18	30	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	16	6	-	ns
		STCP HIGH or LOW; see Figure 7	16	5	-	ns
		$\overline{MR}$ LOW; see Figure 9	20	8	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	16	5	-	ns
		SHCP to STCP; see Figure 7	16	8	-	ns
DS to SHCP hold time	t_h	see Figure 8	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	10	-7	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	30	52	-	MHz
power dissipation capacitance	C_{PD}	all 9 outputs switching; f_i=1MHz; V_I=GND to V_{CC}-1.5V	-	130	-	pF

Note:

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.3、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC595							
propagation delay	t_{pd}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	34	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
power dissipation capacitance	C_{PD}	all 9 outputs switching; f_i=1MHz; V_I=GND to V_{CC}		-	-	-	pF

AiP74HCT595; V_{CC}=4.5V to 5.5V						
propagation delay	t_{pd}	SHCP to Q7S; see Figure 6	-	-	53	ns
		STCP to Qn; see Figure 7	-	-	50	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	-	-	50	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 10	-	-	44	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 10	-	-	38	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	20	-	-	ns
		STCP HIGH or LOW; see Figure 7	20	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	25	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	20	-	-	ns
		SHCP to STCP; see Figure 7	20	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	13	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	24	-	-	MHz
power dissipation capacitance	C_{PD}	all 9 outputs switching; f_i=1MHz; V_I=GND to V_{CC}-1.5V	-	-	-	pF

Note:

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

4、Testing Circuit

4.1、AC Testing Circuit

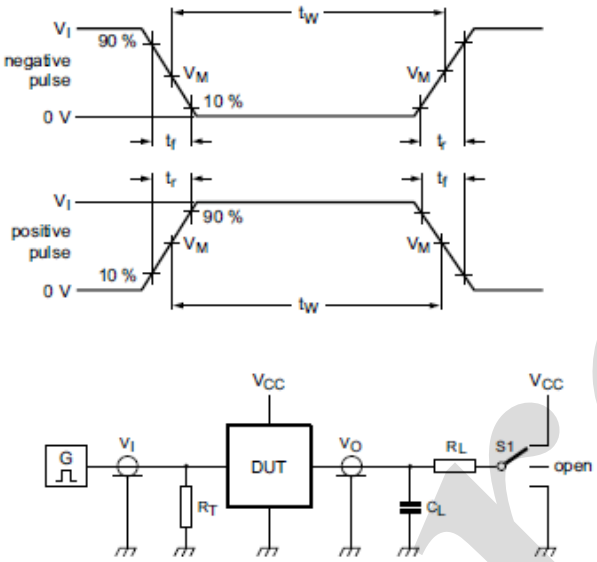


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

4.2、AC Testing Waveforms

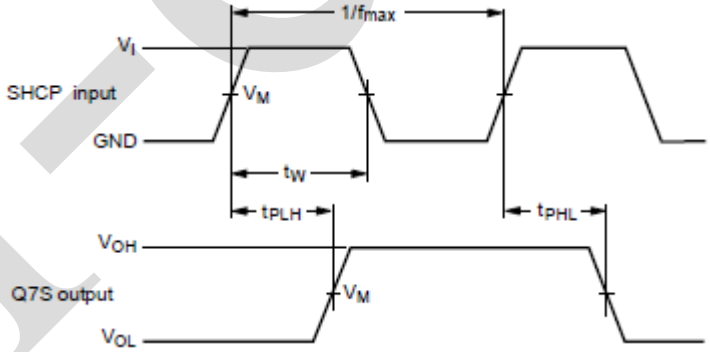


Figure 6. Shift clock pulse, maximum frequency and input to output propagation delays

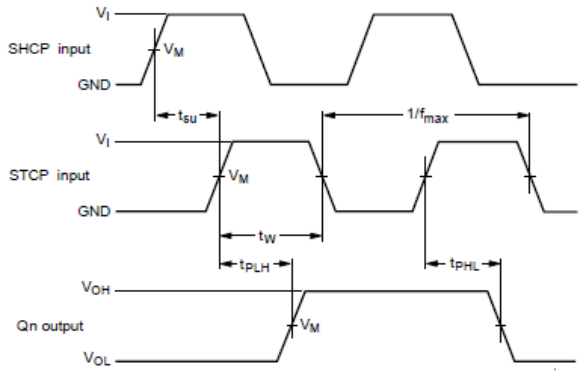


Figure 7. Storage clock to output propagation delays

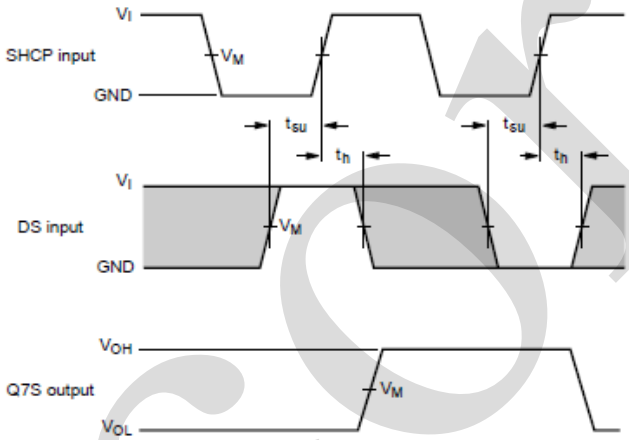


Figure 8. Data set-up and hold times

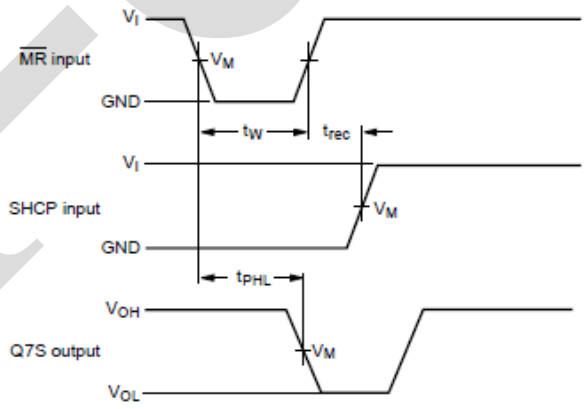


Figure 9. Master reset to output propagation delays

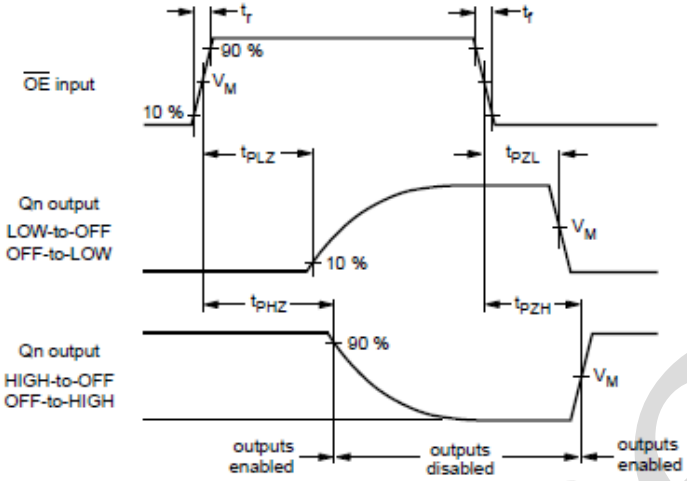


Figure 10. Enable and disable times

4.3、Measurement Points

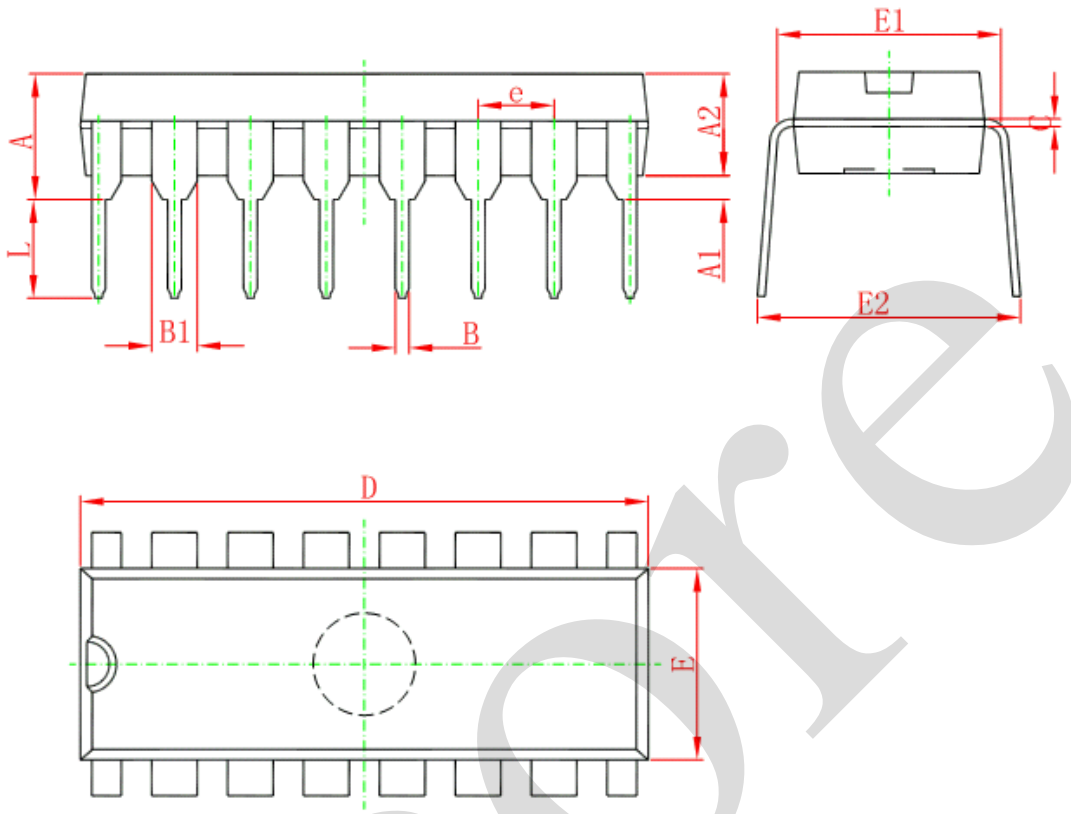
Type	Input	Output
	V_M	V_M
AiP74HC595	$0.5\times V_{CC}$	$0.5\times V_{CC}$
AiP74HCT595	1.3V	1.3V

4.4、Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
AiP74HC595	V_{CC}	6ns	50pF	1kΩ	open	GND	V_{CC}
AiP74HCT595	3V	6ns	50pF	1kΩ	open	GND	V_{CC}

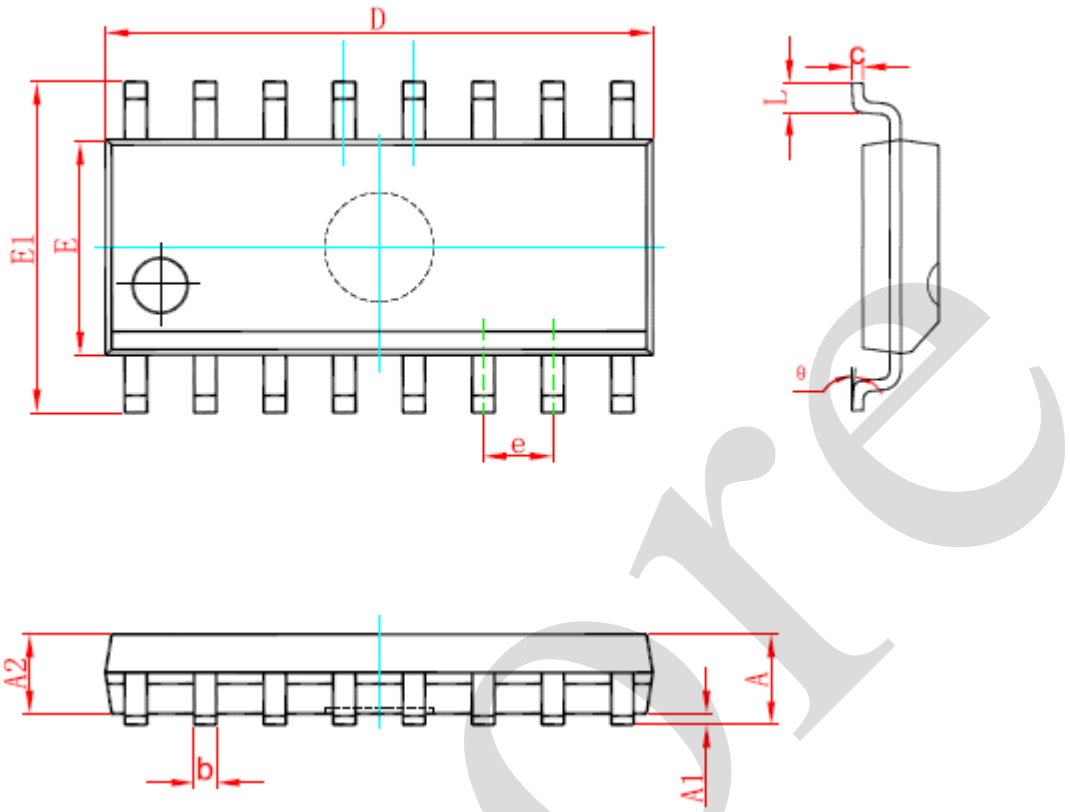
5、Package Information

5.1、DIP16



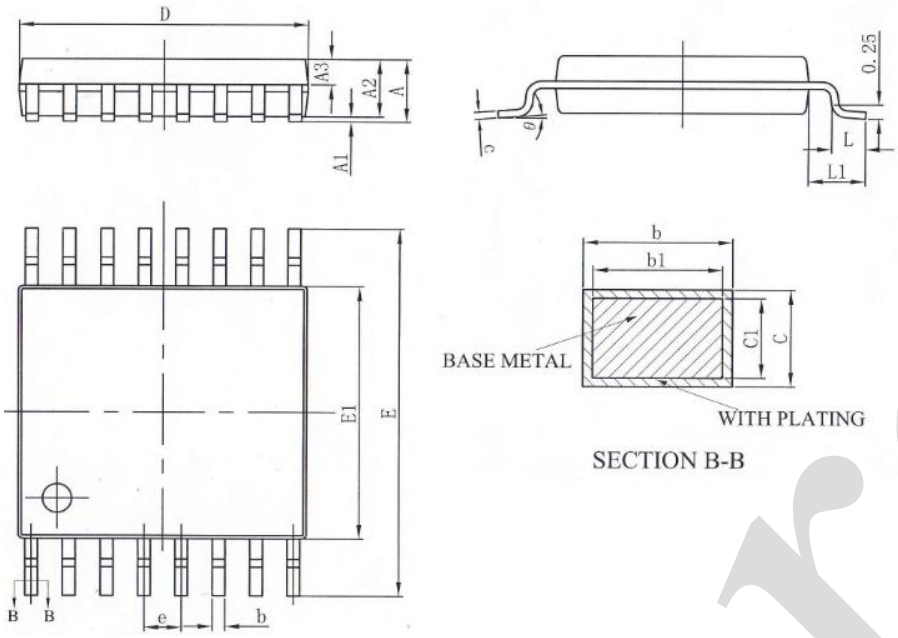
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.3、TSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

i-core

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.