1 Features

Very low power consumption:

– 1-mW typical at V_{DD} = 5 V

Capable of operation in astable mode

CMOS output capable of swinging rail to rail

High output current capability

– Sink: 100-mA typical

– Source: 10-mA typical

2 Applications

Precision timing

Pulse generation

Sequential timing

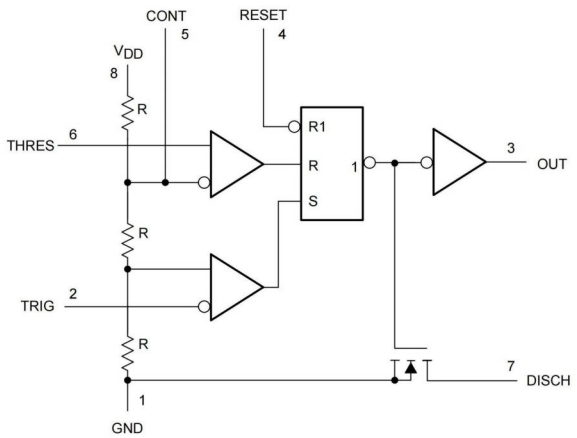
Time delay generation

Pulse width modulation

Pulse position modulation

Linear ramp generator

Simplified Schematic

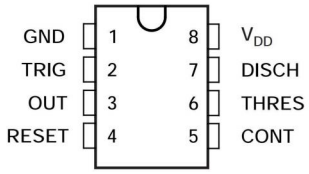


3 Description

This is a monolithic timing circuit fabricated.The timer is fully
compatible with CMOS, and MOS logic and operates at frequencies up to 2 MHz. Because of its high input impedance, this device supports smaller timing capacitors than those supported by other. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage. It has a trigg er level equal
to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, theflip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flipflop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal (DISCH) and GND. All unused inputs must be tied to an appropriate logic level to prevent false triggering.

4 Pin Configuration and Functions

pin diagram



Pin function diagram

PIN		I/O	DESCRIPTION
NAME	SOIC, PDIP, SOP, CDIP		
CONT	5	I	Controls comparator thresholds. Outputs 3 V_{DD} and allows bypass capacitor connection.
DISCH	7	O	Open collector output to discharge timing capacitor.
GND	1	—	Ground.
NC	—	—	No internal connection.
OUT	3	O	High current timer output signal.
RESET	4	I	Active low reset input forces output and discharge low.
THRES	6	I	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V_{DD}	8	—	Power-supply voltage.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)*Continuous total power dissipation* and *lead temperature* parameters from *Absolute Maximum Ratings*

			MIN	MAX	UNIT
Voltage	Supply, V_{DD} (2)		–0.3	18	V
	Input, any input		–0.3	V_{DD}	
	Discharge		–0.3	18	
Current	Sink, discharge or output			150	mA
	Source, output, I_O			15	
Temperature	Operating, T_A	XD/XL555	–40	85	°C
	Case, for 60 seconds	FK package	–65	150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}	XD/XL555	3	15	V
Operating free-air temperature, T_A	XD/XL555	–40	85	°C

5.4 Electrical Characteristics: V_{DD} = 3 V for XD/XL555 over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	XD/XL555	1.6		2.4	V
		Full range	XD/XL555	1.5		2.5	
I_{IT}	Threshold current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
$V_{I(TRIG)}$	Trigger voltage	25°C	XD/XL555	0.71	1	1.29	V
		Full range	XD/XL555	0.61		1.39	
$I_{I(TRIG)}$	Trigger current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
$V_{I(RESET)}$	Reset voltage	25°C	XD/XL555	0.4	1.1	1.5	V
		Full range	XD/XL555	0.3		1.8	
	Control voltage (open-circuit) as a percentage of supply voltage	Max	XD/XL555		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1 mA, 25°C	XD/XL555		0.03	0.2	V
		I_{OL} = 1 mA, Full range	XD/XL555			0.375	
	Discharge switch off-stage current	25°C	XD/XL555		0.1		nA
		Max	XD/XL555		120		
V_{OH}	High-level output voltage	I_{OH} = –300 µA, 25°C	XD/XL555	2.5	2.85		V
		I_{OH} = –300 µA, Full range	XD/XL555	2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, 25°C	XD/XL555		0.07	0.3	V
		I_{OL} = 1 mA, Full range	XD/XL555			0.4	
I_{DD}	Supply current[2]	25°C	XD/XL555			250	µA
		Full range	XD/XL555			500	
C_{PD}	Power dissipation capacitance[3][4]	25°C	XD/XL555		90		pF

(1) Full range is –40°C to 85°C for the XD/XL555. For conditions shown as ***Max***, use the appropriate value specified in the *Recommended Operating Conditions* table.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

5.5 Electrical Characteristics: V_{DD} = 5 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	XD/XL555	2.8	3.3	3.8	V
		Full range	XD/XL555	2.7		3.9	
I_{IT}	Threshold current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
$V_{I(TRIG)}$	Trigger voltage	25°C	XD/XL555	1.36	1.66	1.96	V
		Full range	XD/XL555	1.26		2.06	
$I_{I(TRIG)}$	Trigger current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
C_I	Trigger, threshold capacitance (each pin)	25°C	XD/XL555		2.1		pF
$V_{I(RESET)}$	Reset voltage	25°C	XD/XL555	0.4	1.1	1.5	V
		Full range	XD/XL555	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
	Control voltage (open circuit) as a percentage of supply voltage	Max	XD/XL555		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 10 mA, 25°C	XD/XL555		0.14	0.5	V
		I_{OL} = 10 mA, Full range	XD/XL555			0.6	
	Discharge switch off-stage current	25°C	XD/XL555		0.1		nA
		Max	XD/XL555		120		
V_{OH}	High-level output voltage	I_{OH} = –1 mA, 25°C	XD/XL555	4.1	4.8		V
		I_{OH} = –1 mA, Full range	XD/XL555	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA, 25°C	XD/XL555		0.21	0.4	V
		I_{OL} = 8 mA, Full range	XD/XL555			0.5	

(1) Full range is –40°C to 85°C for the XD/XL555, For conditions shown as ***Max*** use the appropriate value specified in the *Recommended Operating Conditions* table.

Electrical Characteristics: V_{DD} = 5 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 5 mA, 25°C	XD/XL555		0.13	0.3	V
		I_{OL} = 5 mA, Full range	XD/XL555			0.4	
		I_{OL} = 3.2 mA, 25°C	XD/XL555		0.08	0.3	
		I_{OL} = 3.2 mA, Full range	XD/XL555			0.35	
I_{DD}	Supply current(2)	25°C	XD/XL555		170	350	µA
		Full range	XD/XL555			600	
C_{PD}	Power dissipation capacitance(3)(4)	25°C	XD/XL555		115		pF

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

5.6 Electrical Characteristics: V_{DD} = 15 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C	XD/XL555	9.45	10	10.55	V
		Full range	XD/XL555	9.35		10.65	
I_{IT}	Threshold current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
$V_{I(TRIG)}$	Trigger voltage	25°C	XD/XL555	4.65	5	5.35	V
		Full range	XD/XL555	4.55		5.45	
$I_{I(TRIG)}$	Trigger current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		
C_I	Trigger, threshold capacitance (each pin)	25°C	XD/XL555		1.8		pF
$V_{I(RESET)}$	Reset voltage	25°C	XD/XL555	0.4	1.1	1.5	V
		Full range	XD/XL555	0.3		1.8	
$I_{I(RESET)}$	Reset current	25°C	XD/XL555		10		pA
		Max	XD/XL555		150		

(1) Full range is –40°C to 85°C for XD/XL555, For conditions shown as ***Max***, use the appropriate value specified in the *Recommended Operating Conditions* table.

Electrical Characteristics: V_{DD} = 15 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
	Control voltage (open circuit) as a percentage of supply voltage	Max	XD/XL555		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100 mA, 25°C	XD/XL555		0.77	1.7	V
		I_{OL} = 100 mA, Full range	XD/XL555			1.8	
	Discharge switch off-stage current	25°C	XD/XL555		0.1		nA
		Max	XD/XL555		120		
V_{OH}	High-level output voltage	I_{OH} = –10 mA, 25°C	XD/XL555	12.5	14.2		V
		I_{OH} = –10 mA, Full range	XD/XL555	12.5			
		I_{OH} = –5 mA, 25°C	XD/XL555	13.5	14.6		
		I_{OH} = –5 mA, Full range	XD/XL555	13.5			
		I_{OH} = –1 mA, 25°C	XD/XL555	14.2	14.9		
		I_{OH} = –1 mA, Full range	XD/XL555	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA, 25°C	XD/XL555		1.28	3.2	V
		I_{OL} = 100 mA, Full range	XD/XL555			3.7	
		I_{OL} = 50 mA, 25°C	XD/XL555		0.63	1	
		I_{OL} = 50 mA, Full range	XD/XL555			1.4	
		I_{OL} = 10 mA, 25°C	XD/XL555		0.12	0.3	
		I_{OL} = 10 mA, Full range	XD/XL555			0.4	
I_{DD}	Supply current(2)	25°C	XD/XL555		360	600	µA
		Full range	XD/XL555			900	
C_{PD}	Power dissipation capacitance(3)(4)	25°C	XD/XL555		140		pF

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.
(3) C_{PD} is used to determine the dynamic power consumption.
(4) $P_D = V_{DD}^2 f_o (C_{PD} + C_L)$ where f_o = output frequency, C_L = output load capacitance, V_{DD} = supply voltage

5.7 Operating Characteristics

V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Initial error of timing interval(1)	V_{DD} = 5 V to 15 V, C_T = 0.1 F R_A = R_B = 1 k to 100 k (2)		1%	3%	
	Supply voltage sensitivity of timing interval	V_{DD} = 5 V to 15 V, C_T = 0.1 F R_A = R_B = 1 k to 100 k (2)		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 M , C_L = 10 pF		20	75	ns
t_f	Output pulse fall time	R_L = 10 M , C_L = 10 pF		15	60	ns
f_{max}	Maximum frequency in a-stable mode	R_A = 470 , C_T = 200 pF R_B = 200 (2)	1.2	2.1		MHz

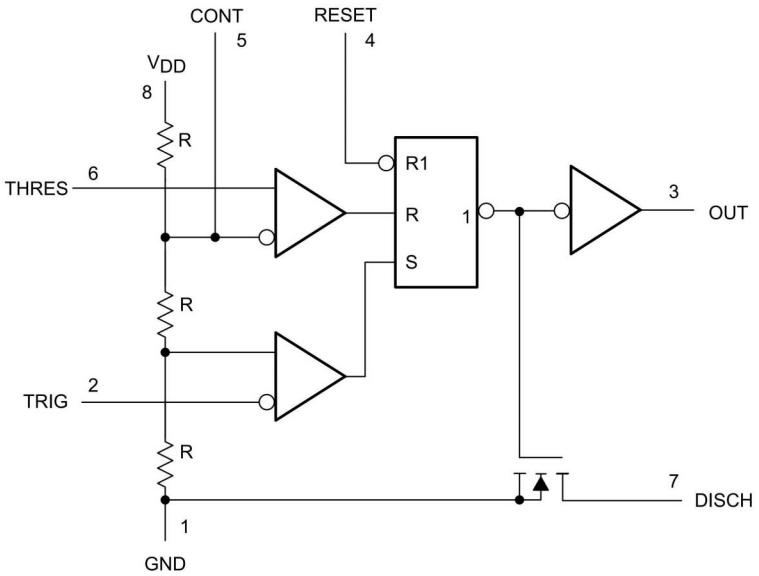
(1) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(2) R_A, R_B, and C_T are as defined in Figure 12.

6 Detailed Description

6.1 Overview

The XD/XL555 is a precision timing device used for general-purpose timing applications up to 2.1 MHz. All inputs are level sensitive not edge triggered inputs.

6.2 Functional Block Diagram



RESET can override TRIG, which can override THRES (when CONT pin is 2/3 V_{DD}).

The resistance of “R" resistors vary with V_{DD} and temperature. The resistors match each other very well across V_{DD} and temperature for a temperature stable control voltage ratio.

6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the internal latch; the output goes high, and discharge pin (DISCH) becomes open drain. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the internal latch, the output goes low, the discharge pin goes low which quickly discharges capacitor C.

Feature Description (continued)

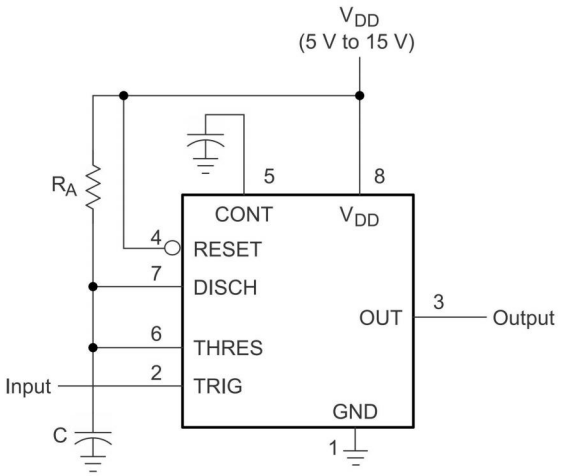


Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 1 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 1 µs, which limits the minimum monostable pulse width to 1 µs. The output pulse duration is approximately $t_w = 1.1 \times R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{DD}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges capacitor C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used it must be connected to V_{DD}.

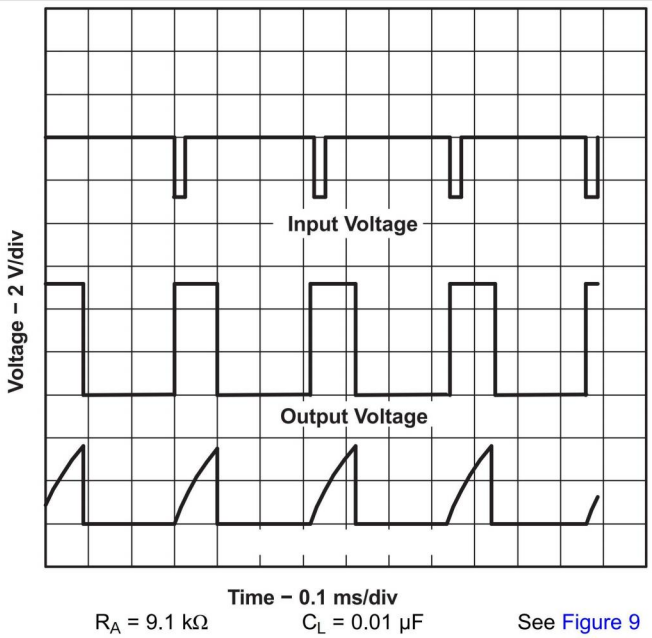


Figure 10. Typical Monostable Waveforms

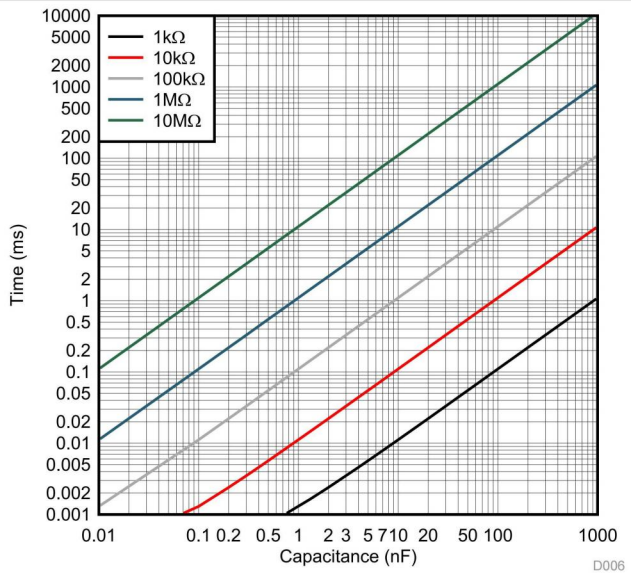


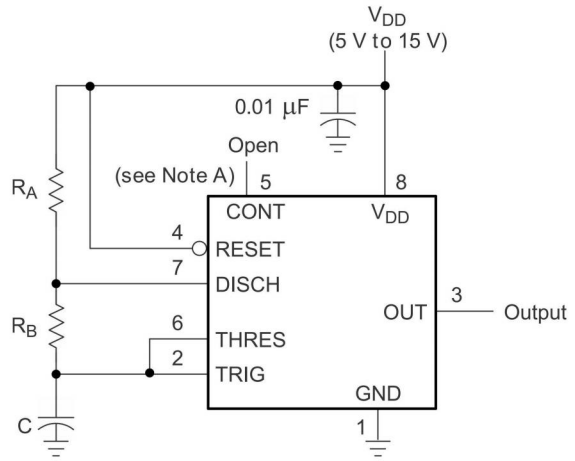
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

6.3.2 Astable Operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

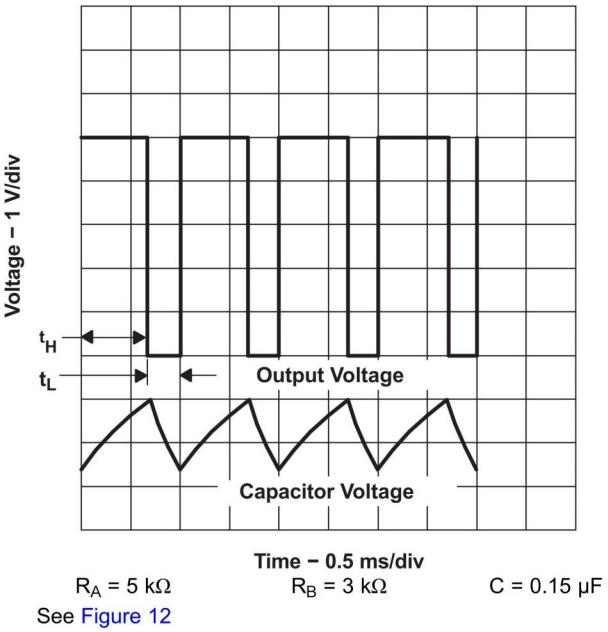


Figure 13. Typical Astable Waveforms

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L for frequencies below 100 kHz can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

period t_H t_L 0.693 R_A $2R_B$ C (3)

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

Output driver duty cycle $\frac{t_L}{t_H}$ $\frac{R_B}{R_A}$ $\frac{}{2R_B}$ (5)

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

Low-to-high ratio $\frac{t_L}{t_H}$ $\frac{R_B}{R_A}$ R_B (7)

Feature Description (continued)

The formulas (1-7) do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor which creates differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low. The equations below provide better agreement with measured values. The formulas Equation 8 represent the actual low and high times when used at higher frequencies because propagation delay and discharge on resistance is added to the formulas. Because the formulas are complex, a calculation tool, XD/XL555 Design Calculator can be used to calculate the component values.

$$t_{c(H)} = C_T\,(R_A + R_B)\,\ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T(R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_{c(L)} = C_T\,(R_B + r_{on})\,\ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T(R_A + R_B)}\right)\right] + t_{PLH} \quad (8)$$

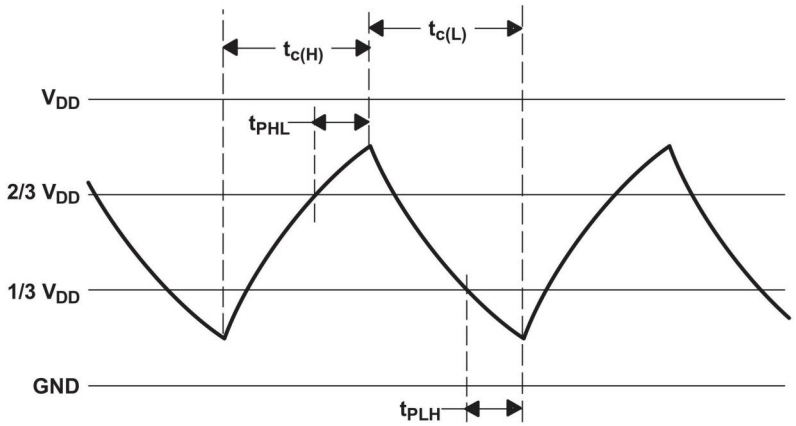


Figure 14. Trigger and Threshold Voltage Waveform

Feature Description (continued)

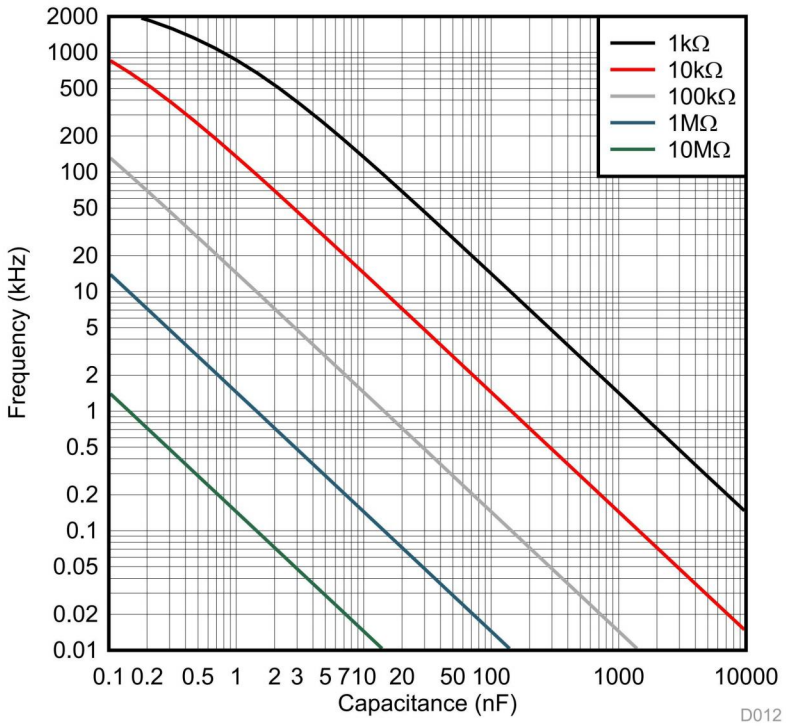
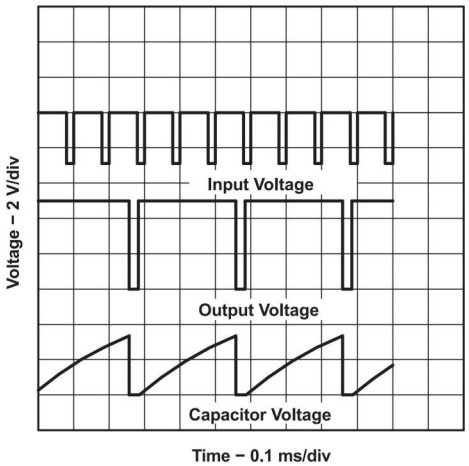


Figure 15. Free-Running Frequency vs Timing Capacitance
Resistance = R_A + 2 × R_B

6.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 16 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.



V_{CC} = 5 V
See Figure 9

R_A = 1250 Ω

C = 0.02 µF

Figure 16. Divide-by-Three Circuit Waveforms

6.4 Device Functional Modes

Table 1 shows the device truth table.

Table 1. Function Table

RESET VOLTAGE(1)	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	L	On
>MAX	<MIN	Irrelevant(2)	H	Off
>MAX	>MAX	>MAX	L	On
>MAX	>MAX	<MIN	As previously established	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Electrical Characteristics: V_{DD} = 5 V*.
(2) CONT pin open or 2/3 V_{DD}.

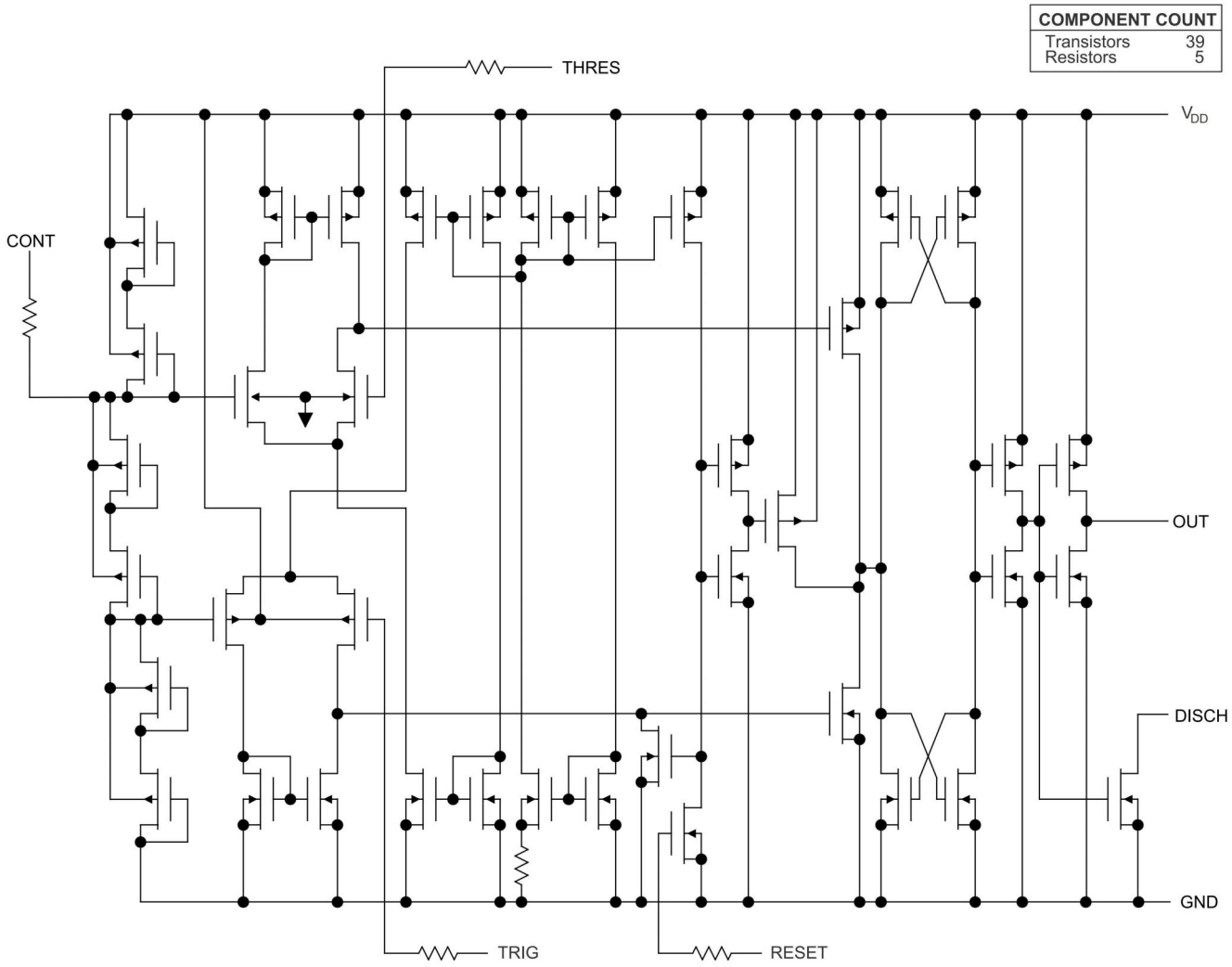


Figure 17. Equivalent Schematic

7 Application and Implementation

7.1 Application Information

The XD/XL555 timer device uses resistor and capacitor charging delay to provide a programmable time delay oroperating frequency. The *Typical Applications* section presents a simplified discussion of the design process. Reset mode forces output and discharge low and provides a small reduction in supply current.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in Figure 18 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 19.

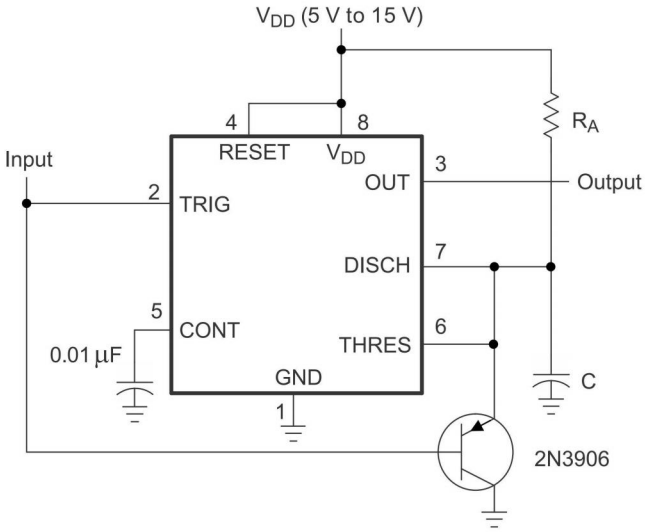


Figure 18. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

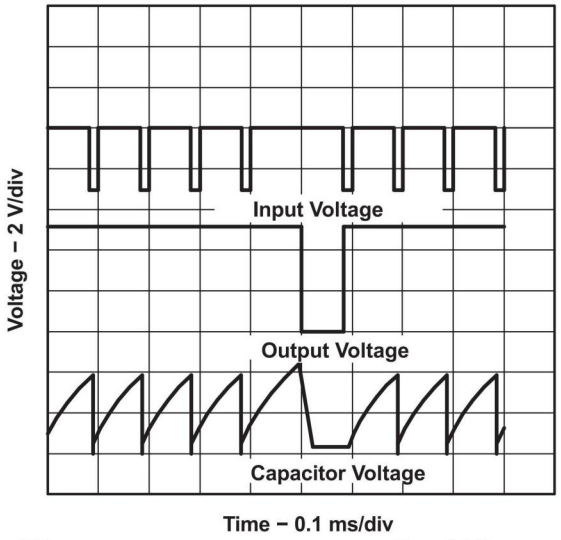
Input fault (missing pulses) must be input high. An input stuck low cannot be detected because the timing capacitor (C) remains discharged.

7.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C >$ [maximum normal input high time].

Typical Applications (continued)

7.2.1.3 Application Curve



V_{DD} = 5 V
See Figure 18

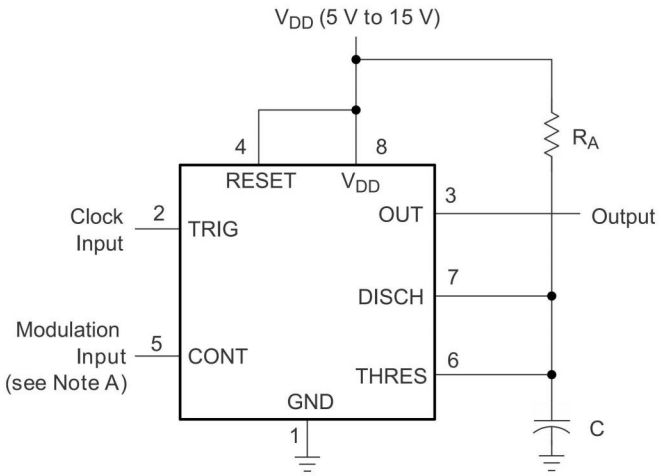
R_A = 1 kΩ

C = 0.1 µF

Figure 19. Timing Waveforms for Missing-Pulse Detector

7.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 20 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 21 shows the resulting duty cycle versus control voltage transfer function. Attempting to run under 10% duty cycle could result in inconsistent output pulses. Attempting to run close to 100% duty cycle will result in frequency division by 2, then 3, then 4.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 20. Circuit for Pulse-Width Modulation

Typical Applications (continued)

7.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD}, respectively. Clock input V_{OL} time must be less than minimum output high time, therefore a high (positive) duty cycle clock is recommended. Minimum recommended modulation voltage is 1 V. Lower CONT voltage can greatly increase threshold comparator's propagation delay and storage time. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC based with an negative exponential curve.

7.2.2.2 Detailed Design Procedure

Choose R_A and C so that R_A × C is same or less than clock input period. Figure 21 shows the non linear relationship between control voltage and output duty cycle. Duty cycle is function of control voltage and clock period relative to RC time constant.

7.2.2.3 Application Curve

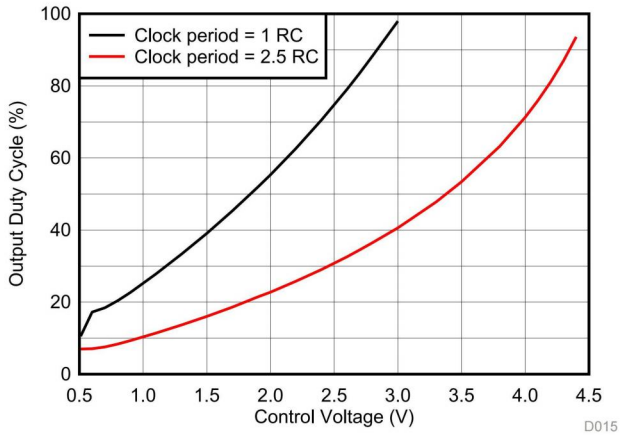
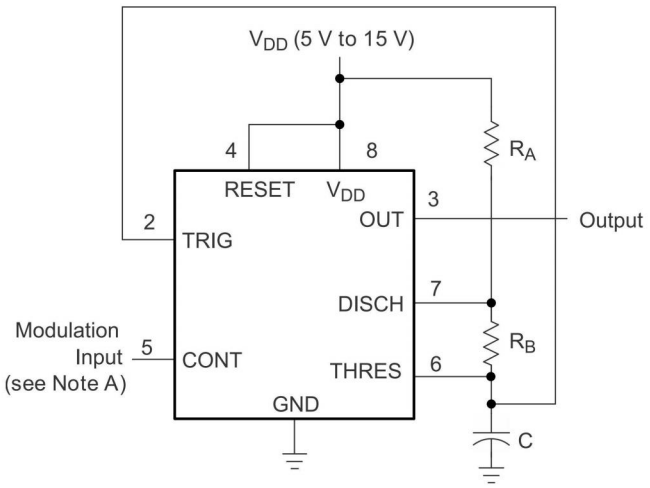


Figure 21. Pulse-Width-Modulation vs Control Voltage
Clock Duty Cycle 98%, V_{DD} = 5 V

7.2.3 Pulse-Position Modulation

As shown in Figure 22, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. Figure 23 and Figure 24 shows the output frequency and duty cycle versus control voltage.

Typical Applications (continued)



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

R_A = 3 kΩ R_B = 309 kΩ C = 1 nF

Figure 22. Circuit for Pulse-Position Modulation

7.2.3.1 Design Requirements

Both DC- and AC-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage. Control voltage below 1 V could result in output glitches instead of a steady output pulse stream

7.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle for control voltage set to 2/3 of V_{DD} can be determined using formulas in *Astable Operation* section.

7.2.3.3 Application Curves

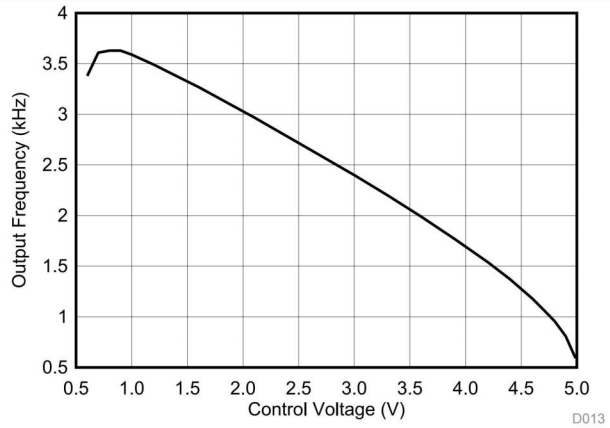


Figure 23. Pulse-Position-Modulation Frequency vs Control Voltage, V_{DD} = 5 V

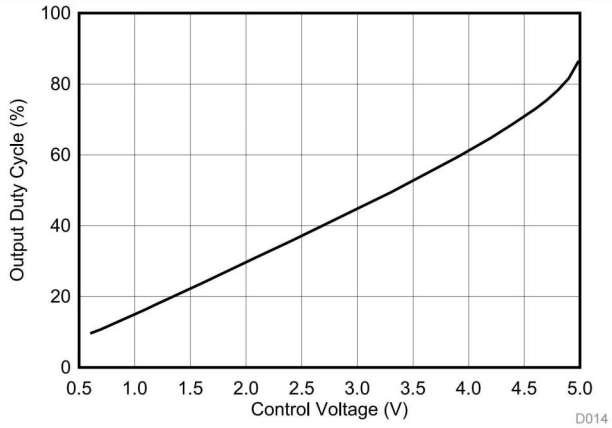
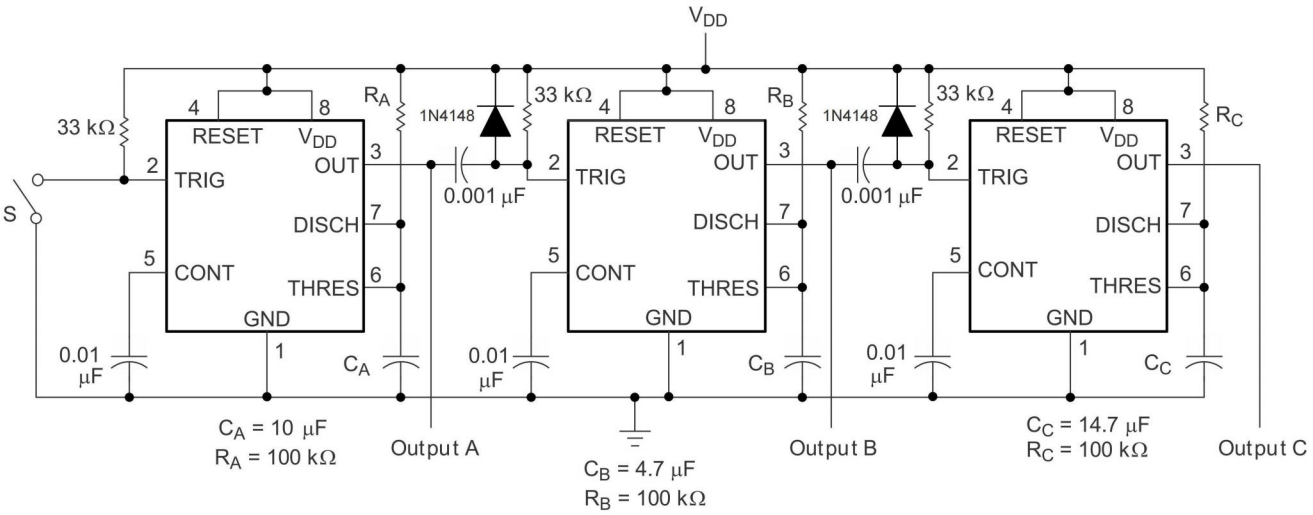


Figure 24. Pulse-Position-Modulation Duty Cycle vs Control Voltage, V_{DD} = 5 V

Typical Applications (continued)

7.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 25 shows a sequencer circuit with possible applications in many systems, and Figure 26 shows the output waveforms.



NOTE: S closes momentarily at t = 0.

Figure 25. Sequential Timer Circuit

7.2.4.1 Design Requirements

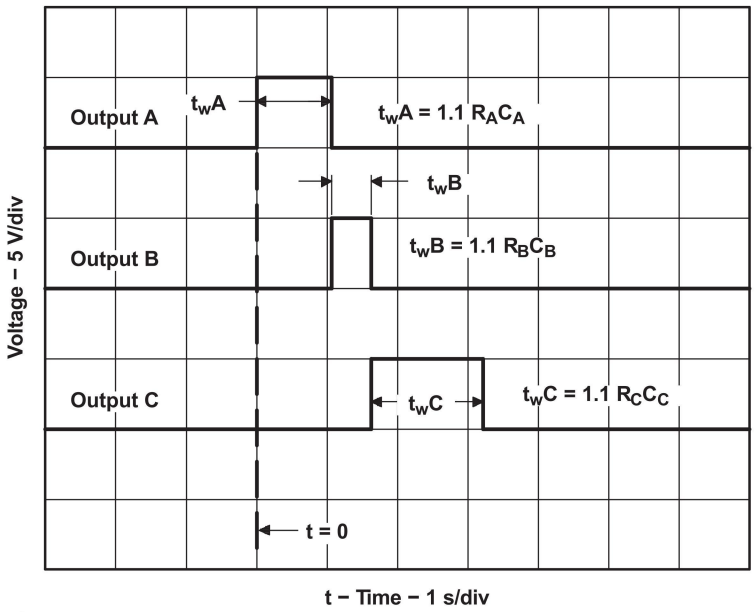
The sequential timer application chains together multiple monostable timers. The joining components are the 33-kΩ resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next monostable. A diode is needed to prevent over voltage on the trigger input when on the previous output's low to high edge.

7.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula: $t_w = 1.1 \times R \times C$.

Typical Applications (continued)

7.2.4.3 Application Curve



See Figure 25

Figure 26. Sequential Timer Waveforms

7.2.5 Designing for Improved ESD Performance

The XD/XL555 internal HBM and CDM protection allows for safe assembly in ESD controlled environments. In applications that may expose pins of the XD/XL555 to ESD, additional protection is highly recommended. The test board schematic below has bypass capacitors, current-limiting resistors, and voltage clamping TVS diodes to provide additional protection for commonly exposed pins [Reset, Trig, and Output] against ESD.

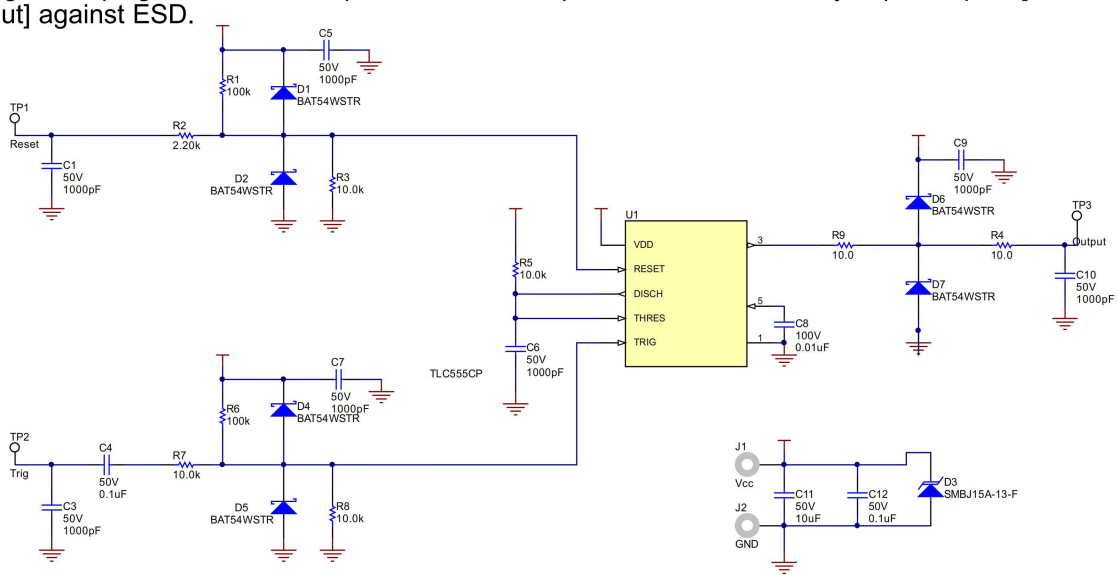


Figure 27. ESD Test Schematic

Typical Applications (continued)

The table below gives the ESD protection levels recorded for different supply voltages and external components populated. Using only passive components to protect the XD/XL555 with a single 15-V supply is not recommended because the higher voltage allows for an unacceptable amount of current to flow through the device.

Table 2. ESD test result table

Supply Voltage	Just passive components populated. D1..D7 not populated(1)	All components populated (1)
5 V	8 kV	12 kV
15 V	Not recommended	12 kV

(1) Sample results. Results may vary with populated components, board layout, and samples used.

8 Power Supply Recommendations

The XD/XL555 requires a voltage supply greater than or equal to 2 V, 3 V, or 5 V based the coldest ambient temperature supported and a supply voltage less than or equal to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry and provide stable output pulses. Minimum recommended is 0.1-μF ceramic in parallel with 1-μF electrolytic. Place the bypass capacitors as close as possible to the XD/XL555 and minimize the trace length.

9 Layout

9.1 Layout Guidelines

Standard PCB rules apply to routing the XD\XL555. The 0.1-μF ceramic capacitor in parallel with a 1-μF electrolytic capacitor must be as close as possible to the XD\XL555.
The capacitor used for the time delay must also be placed as close to the discharge pin.
A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.
Figure 28 is the basic layout for various applications.

- C1—based on time delay calculations
- C2—0.01-μF bypass capacitor for control voltage pin
- C3—0.1-μF bypass ceramic capacitor
- C4—1-μF electrolytic bypass capacitor
- R1—based on time-delay calculations

9.2 Layout Example

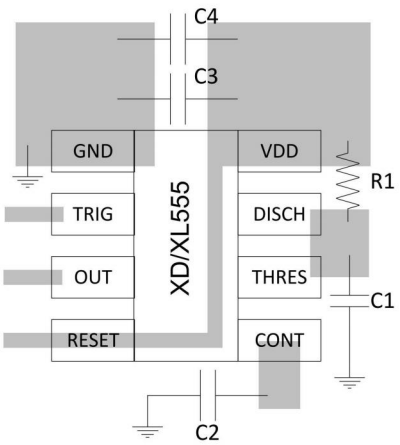
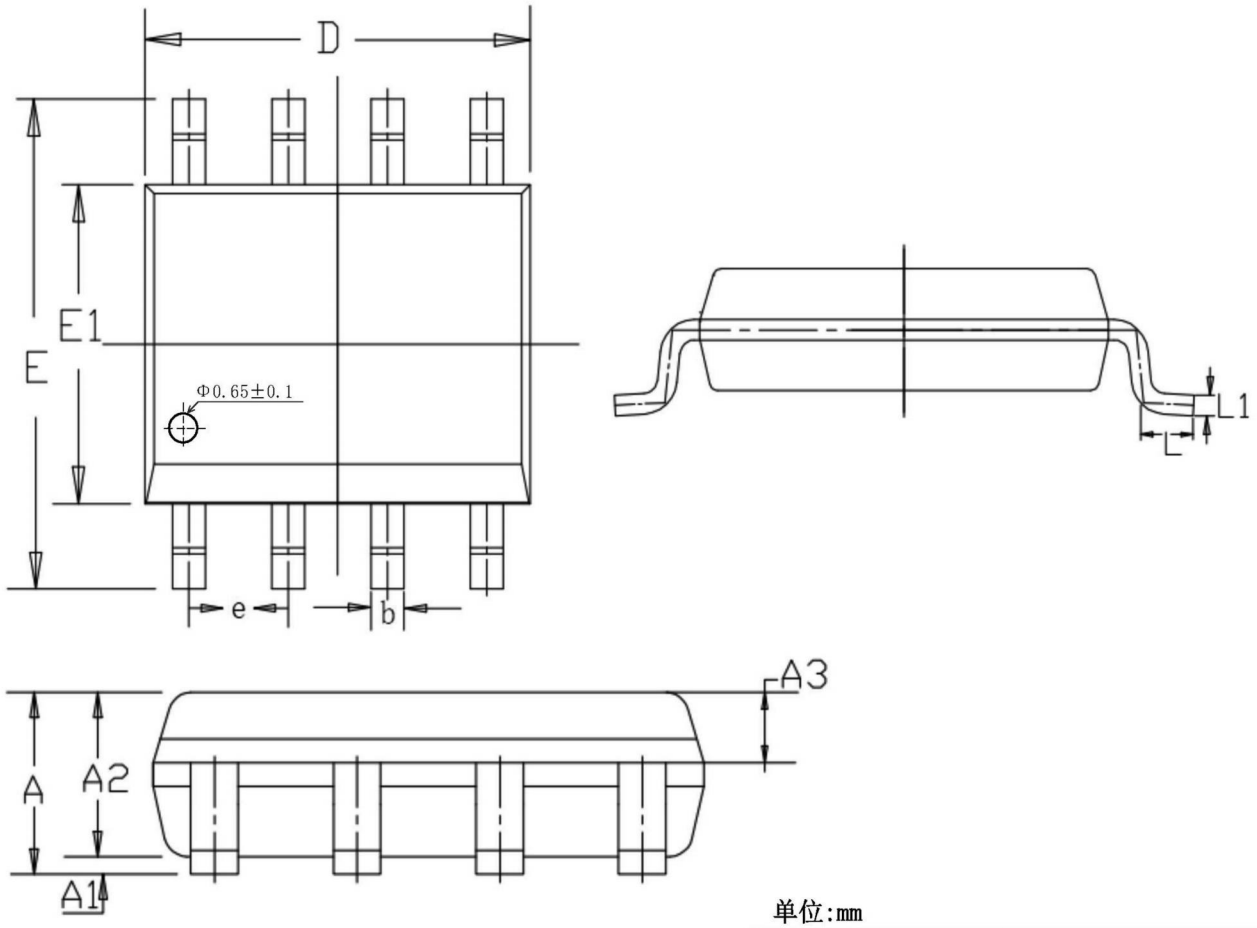


Figure 28. Layout Example

Ordering Information							
part Number	Device Marking	Package type	Body size (mm)	Temperature(℃)	MSL	Transport	Package Quantit
XL555	XL555	SOP8	4.9*3.9	-40 to +85	MSL3	T&R	2500
XD555	XD555	DIP8	9.25*6.38	-40 to +85	MSL3	Tube 50	2000

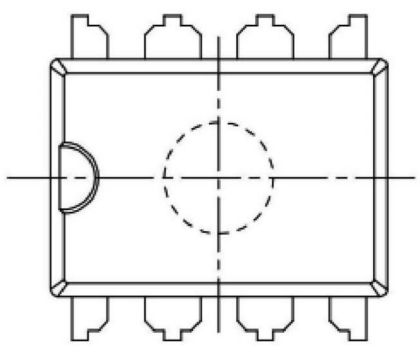
SOP8封装尺寸图

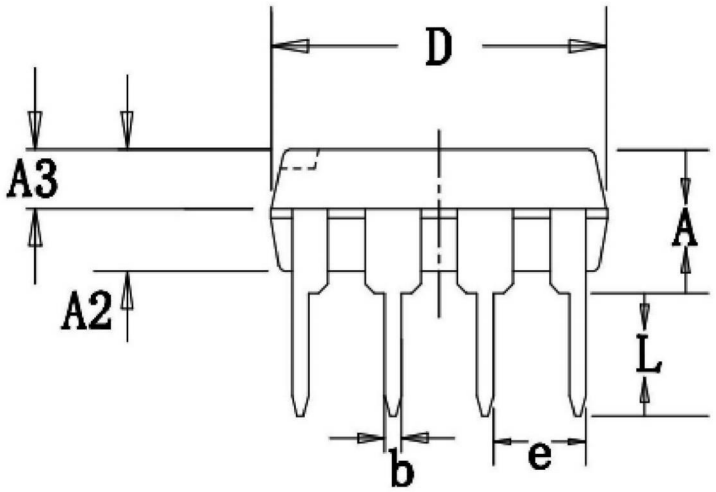


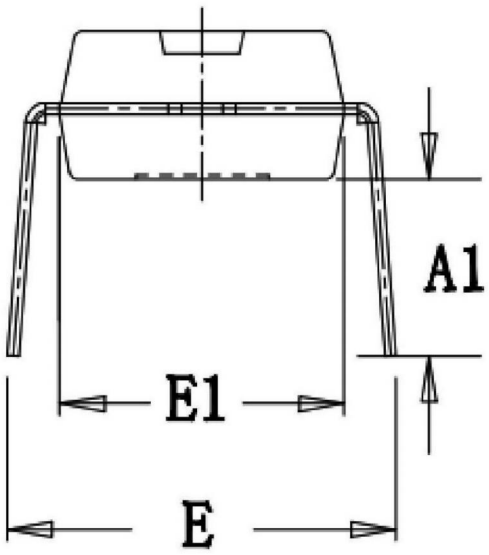
单位:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1(站高)	0.100	0.150	0.200
A2(厚度)	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	-	0.510
e(脚间距)	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
E(跨度)	5.800	6.000	6.200
E1(宽度)	3.800	3.900	4.000
L(脚长)	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8封装尺寸图







单位:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1(站高)	3.786	3.886	3.986
A2(厚度)	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	—	0.490
e(脚间距)	2.510	2.540	2.570
D(长度)	9.150	9.250	9.350
E(跨度)	7.800	8.500	9.200
E1(宽度)	6.280	6.380	6.480
L(脚长)	3.000	—	—