NBM™ Bus Converter
NBM2317S60E1560T0R

Non-Isolated, Fixed Ratio DC-DC Converter

Features & Benefits

- Maximum continuous output power: 800W
  - Up to 1kW, 2ms peak power capability
- Rated output current (step-down operation):
  - 60A continuous
  - 100A transient, up to 2ms
- Rated output current (step-up operation):
  - 15A continuous
  - 25A transient, up to 2ms
- Up to 4.5kW/in^3 power density
- 97.9% peak efficiency
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- NBM2317 SM-ChiP™ package
  - 0.899 x 0.683 x 0.292in [22.83 x 17.34 x 7.42mm]
- Thermally-adept SM-ChiP
- Bidirectional start up and steady-state operation
- Simple implementation, no external components required
- Built-in hot-swap capabilities and inrush current limiting

Typical Applications

- DC Power Distribution
- High-Performance Computing Systems (HPC)
- Mild Hybrid and Autonomous Vehicles
- Automated Test Equipment (ATE)
- Industrial Systems
- High-Density Power Supplies
- Communications Systems
- Transportation
- Bidirectional DC Energy Storage

Product Ratings (Step-Down Operation)	
V_{HI} = 54V (40 – 60V)	I_{LO} = up to 60A
V_{LO} = 13.5V (10 – 15V) (NO LOAD)	K = 1/4

Product Description

The NBM2317S60E1560T0R is a high-efficiency Non-Isolated Bus Converter operating from a 40 to 60V_{DC} high-side voltage bus to deliver a ratiometric low-side voltage from 10 to 15V_{DC}.

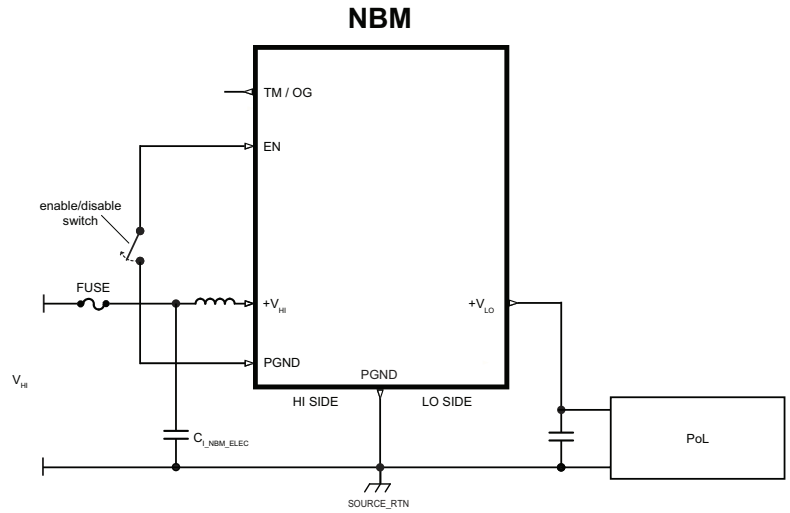
The NBM2317S60E1560T0R offers low noise, fast transient response, and industry-leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a PoL regulator to be located at the high side of the NBM. With a high-side to low-side K factor of 1/4, that capacitance value can be reduced by a factor of 16x, resulting in savings of board area, material and total system cost.

Leveraging the thermal and density benefits of Vicor SM-ChiP packaging technology, the NBM offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally-adept SM-ChiP-based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

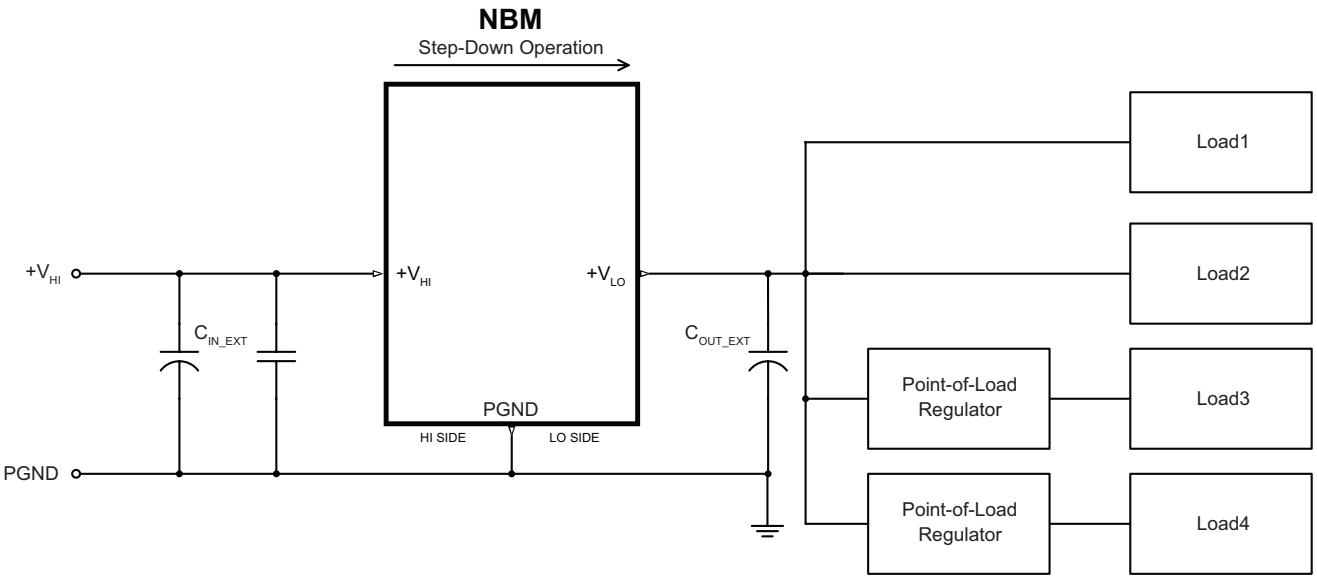
The NBM non-isolated topology allows bidirectional start up and steady-state operation and provides bidirectional protections.

Note: Product images may not highlight current product markings.

Typical Applications

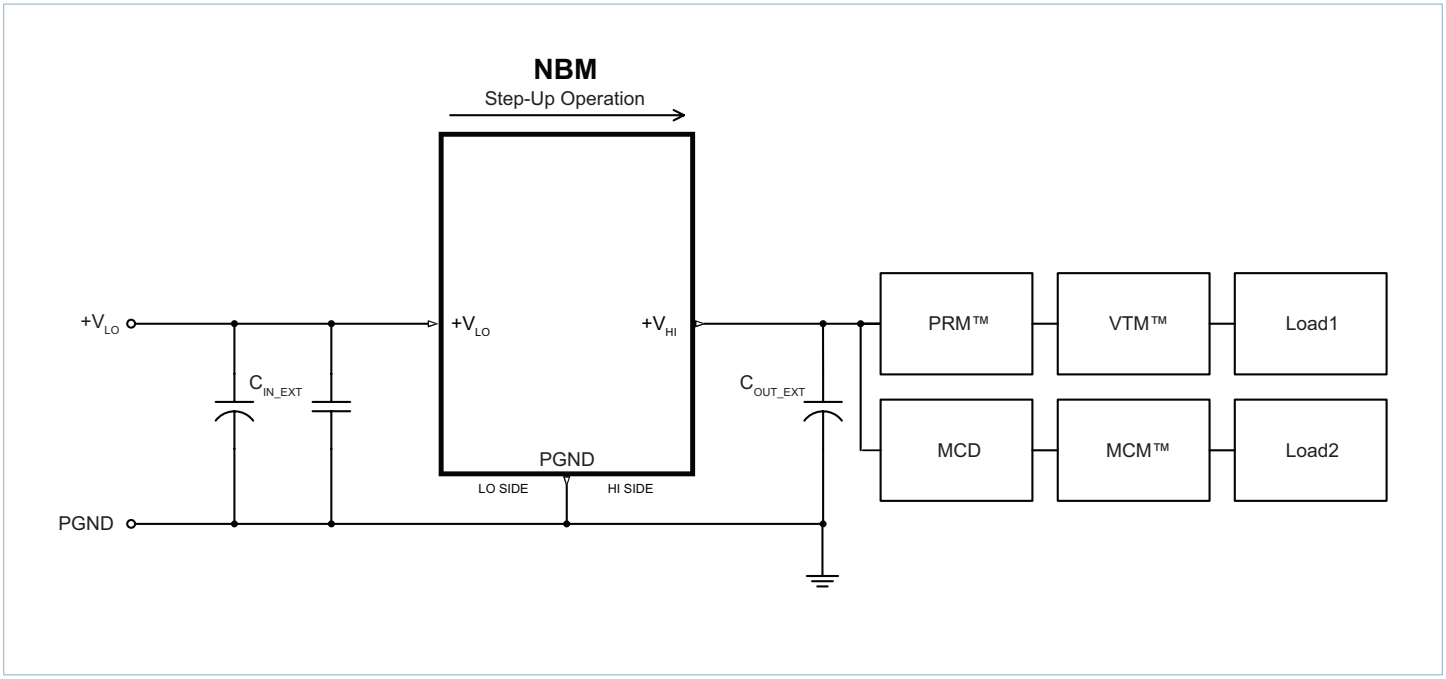


NBM2317S60E1560T0R + point-of-load



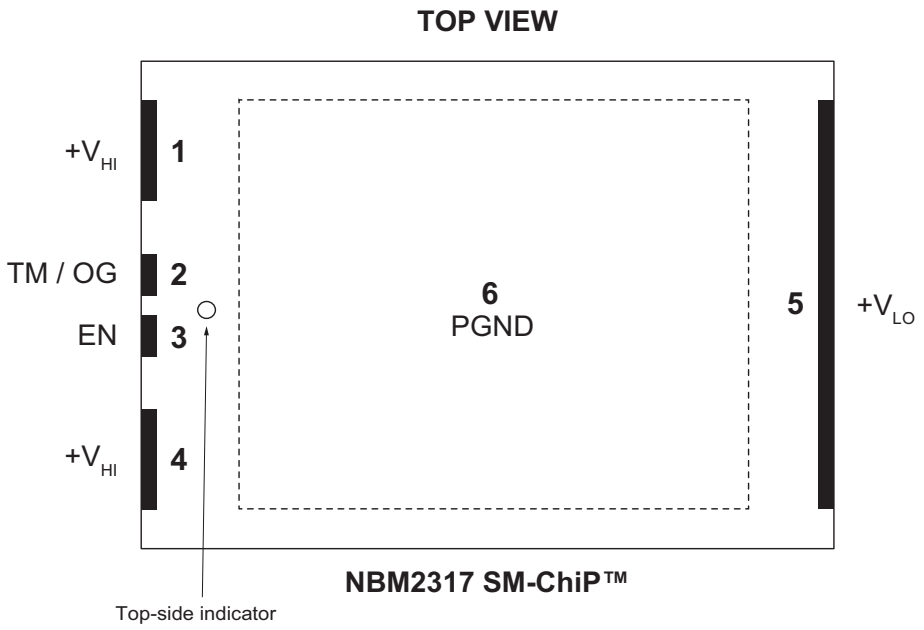
NBM2317S60E1560T0R in step-down operation powering point-of-load regulators and direct loads

Typical Applications (Cont.)



NBM2317S60E1560T0R in step-up operation powering PRM + VTMs and MCD + MCM

Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
1, 4	$+V_{HI}$	HIGH SIDE POWER	High-side power positive terminals
2	TM / OG	OUTPUT	Temperature Monitor and Output Good
3	EN	INPUT	Enables / disables NBM. When held low, the unit will be disabled
5	$+V_{LO}$	LOW SIDE POWER	Low-side power positive terminal
6	PGND	POWER RETURN	Common negative high-side and low-side power return terminal

Part Ordering Information

Part Number	Temperature Grade	Option		Tray Size
NBM2317S60E1560**T0R**	**T** = –40 to 125°C	**0R** = Reversible Analog Control		55 parts per tray

All products shipped in JEDEC standard high-profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
$+V_{HI\_DC}$ to PGND		–1	80	V
V_{HI_DC} or V_{LO_DC} Slew Rate (Operational)			1	V/µs
$+V_{LO\_DC}$ to PGND		–1	16.9	V
TM to PGND		–0.3	7	V
EN to PGND			15	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Step-Down Operation (High-Voltage Side to Low-Voltage Side)						
High-Side Input Voltage Range (Continuous)	V_{HI_DC}		**40**		**60**	V
High-Side Input Quiescent Current	I_{HI_Q}	Disabled, EN low, V_{HI_DC} = 54V		1.5		mA
		$T_{INTERNAL}$ ≤ 100°C			3.0	
No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 54V, $T_{INTERNAL}$ = 25°C		3.6	7	W
		V_{HI_DC} = 54V	**2**		**11**	
		V_{HI_DC} = 40 – 60V, $T_{INTERNAL}$ = 25°C			8	
		V_{HI_DC} = 40 – 60V			**14.5**	
High-Side Input Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 54V, C_{LO_EXT} = 1000µF, no load		7.5		A
		$T_{INTERNAL}$ ≤ 100°C			**12**	
DC High-Side Input Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 60A, $T_{INTERNAL}$ ≤ 100°C			16.3	A
Transformation Ratio	K	High voltage side to low voltage side, K = V_{LO_DC} / V_{HI_DC}, at no load		1/4		V/V
Low-Side Output Current (Continuous)	$I_{LO\_OUT\_DC}$	40V ≤ V_{HI_DC} ≤ 60V			60	A
Low-Side Output Current (Pulsed)	$I_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			100	A
Low-Side Output Power (Continuous)	$P_{LO\_OUT\_DC}$	54V < V_{HI_DC} ≤ 60V			800	W
Low-Side Output Power (Pulsed)	$P_{LO\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $P_{LO\_OUT\_AVG}$ ≤ 50% rated $P_{LO\_OUT\_DC}$			1000	W
Efficiency (Ambient)	η_{AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A	97.0	97.4		%
		V_{HI_DC} = 40 – 60V, $I_{LO\_OUT\_DC}$ = 60A	96.2			
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 30A	97.3	97.8		
Efficiency (Hot)	η_{HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A	96.7	97.4		%
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 30A	97.3	97.9		
Efficiency (Over Load Range)	$\eta_{20\%}$	12A < $I_{LO\_OUT\_DC}$ < 60A	**92.0**			%
Low-Side Output Resistance	R_{LO_COLD}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A, $T_{INTERNAL}$ = –40°C	2.6	3.3	4	mΩ
	R_{LO_AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A	3.5	4.4	5.3	
	R_{LO_HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A, $T_{INTERNAL}$ = 100°C	4.4	5.5	5.7	
Switching Frequency	F_{SW}	Low-side voltage ripple frequency = 2x F_{SW}	**1.57**	1.62	**1.67**	MHz
Low-Side Output Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 60A, V_{HI_DC} = 54V, 20MHz BW		120		mV
		$T_{INTERNAL}$ ≤ 100°C			180	
Effective High-Side Input Capacitance (Internal)	C_{HI_INT}	Effective value at 54V_{HI_DC}		11.2		µF
Effective Low-Side Output Capacitance (Internal)	C_{LO_INT}	Effective value at 13.5V_{LO_DC}		55		µF
Rated Low-Side Output Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into short circuit protection			**1000**	µF
Rated Low-Side Output Capacitance (External), Parallel Array Operation	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N • 0.5 • $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel			500	µF

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protection Specification – Step-Down Operation (High-Voltage Side to Low-Voltage Side), Cont.						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{HI\_DC} > V_{HI\_UVLO+}$	**350**	500	600	ms
High-Side Input Overvoltage Lockout Threshold	V_{HI_OVLO+}			64.6	**66**	V
High-Side Input Overvoltage Recovery Threshold	$V_{HI\_OVLO–}$		**60**	64		V
High-Side Input Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			0.4		V
High-Side Input Overvoltage Lockout Response Time	t_{HI_OVLO}			1		µs
High-Side Input Undervoltage Lockout Threshold	$V_{HI\_UVLO–}$		**31.6**	33.2		V
High-Side Input Undervoltage Recovery Threshold	V_{HI_UVLO+}			35	**40**	V
High-Side Input Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			2		V
High-Side Input Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
Input-to-Output Undervoltage Start-Up Delay	$t_{HI\_TO\_LO\_DELAY}$	From $V_{HI\_DC} = V_{HI\_UVLO+}$ to powertrain active, EN floating (i.e., one-time start-up delay from application of V_{HI_DC} to V_{LO_DC})			600	ms
Low-Side Output Soft-Start Ramp Time	$t_{LO\_SOFT\_START}$	From powertrain active; fast current limit protection disabled during soft start		0.5		ms
Low-Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**61**	75	**110**	A
Low-Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter	2	5		ms
Low-Side Output Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**100**			A
Low-Side Output Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC			–45	°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain Specification – Step-Up Operation (Low-Voltage Side to High-Voltage Side)						
Low-Side Input Voltage Range (Start Up)	V_{LO_DC}		**10.8**		**15**	V
Low-Side Input Voltage Range (Continuous)			**10**		**15**	
Low-Side Input Quiescent Current	I_{LO_Q}	Disabled, EN low, V_{LO_DC} = 13.5V		0.6		mA
		$T_{INTERNAL}$ ≤ 100°C			1.2	
No Load Power Dissipation	P_{LO_NL}	V_{LO_DC} = 13.5V, $T_{INTERNAL}$ = 25°C		4.3	7	W
		V_{LO_DC} = 13.5V	**3**		**11**	
		V_{LO_DC} = 10 – 15V, $T_{INTERNAL}$ = 25 °C			8	
		V_{LO_DC} = 10 – 15V			**14**	
Low-Side Input Inrush Current Peak	$I_{LO\_INR\_PK}$	V_{LO_DC} = 15V, C_{HI_EXT} = 68µF, no load		45		A
		$T_{INTERNAL}$ ≤ 100°C			**60**	
DC Low-Side Input Current	$I_{LO\_IN\_DC}$	At $I_{HI\_OUT\_DC}$ = 15A, $T_{INTERNAL}$ ≤ 100°C			62	A
Transformation Ratio	K	Low-voltage side to high-voltage side, K = V_{HI_DC} / V_{LO_DC}, at no load		4		V/V
High-Side Output Current (Continuous)	$I_{HI\_OUT\_DC}$	10V ≤ V_{LO_DC} ≤ 13.5V			15	A
High-Side Output Current (Pulsed)	$I_{HI\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $I_{HI\_OUT\_AVG}$ ≤ 50% rated $I_{HI\_OUT\_DC}$			25	A
High-Side Output Power (Continuous)	$P_{HI\_OUT\_DC}$	13.5V < V_{LO_DC} ≤ 15V			800	W
High-Side Output Power (Pulsed)	$P_{HI\_OUT\_PULSE}$	2ms pulse, 25% duty cycle, $P_{HI\_OUT\_AVG}$ ≤ 50% rated $P_{HI\_OUT\_DC}$			1000	W
Efficiency (Ambient)	η_{AMB}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 15A	96.9	97.3		%
		V_{LO_DC} = 10 – 15V, $I_{HI\_OUT\_DC}$ = 15A	96.2			
		V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 7.5A	97.3	97.9		
Efficiency (Hot)	η_{HOT}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 15A	96.7	97.0		%
		V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 7.5A	97.3	97.8		
Efficiency (Over Load Range)	$\eta_{20\%}$	3A < $I_{HI\_OUT\_DC}$ < 15A	**92.0**			%
High-Side Output Resistance	R_{HI_COLD}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 15A, $T_{INTERNAL}$ = –40°C	50	65	80	mΩ
	R_{HI_AMB}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 15A	62	80	98	
	R_{HI_HOT}	V_{LO_DC} = 13.5V, $I_{HI\_OUT\_DC}$ = 15A, $T_{INTERNAL}$ = 100°C	75	97	118	
Switching Frequency	F_{SW}	High-side output voltage ripple frequency = 2x F_{SW}	**1.57**	1.62	**1.67**	MHz
High-Side Output Voltage Ripple	$V_{HI\_OUT\_PP}$	C_{HI_EXT} = 0µF, $I_{HI\_OUT\_DC}$ = 15A, V_{LO_DC} = 13.5V, 20MHz BW		138		mV
		$T_{INTERNAL}$ ≤ 100°C			**200**	
Effective Low-Side Input Capacitance (Internal)	C_{LO_INT}	Effective value at 13.5V_{LO_DC}		55		µF
Effective High-Side Output Capacitance (Internal)	C_{HI_INT}	Effective value at 54V_{HI_DC}		11.2		µF
Rated High-Side Output Capacitance (External)	$C_{HI\_OUT\_EXT}$	At start up with no load; excessive capacitance may prevent module start up			**68**	µF
Rated High-Side Output Capacitance (External), Parallel Array Operation	$C_{HI\_OUT\_AEXT}$	$C_{HI\_OUT\_AEXT}$ Max = N • 0.5 • $C_{HI\_OUT\_EXT\ MAX}$, where N = the number of units in parallel			34	µF

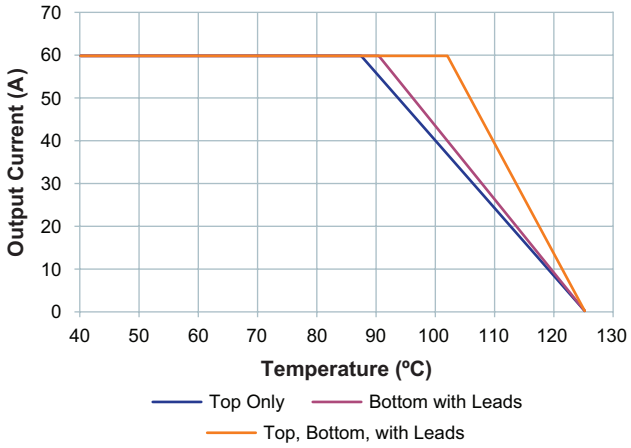
Electrical Specifications (Cont.)

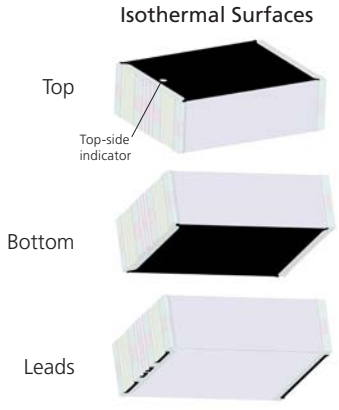
Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protection Specification – Step-Up Operation (Low-Voltage Side to High-Voltage Side), Cont.						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{LO\_DC} > V_{LO\_UVLO+}$	**350**	500	**600**	ms
Low-Side Input Overvoltage Lockout Threshold	V_{LO_OVLO+}			16.7	**17.2**	V
Low-Side Input Overvoltage Recovery Threshold	$V_{LO\_OVLO–}$		**15.4**	15.8		V
Low-Side Input Overvoltage Lockout Hysteresis	$V_{LO\_OVLO\_HYST}$			0.1		V
Low-Side Input Overvoltage Lockout Response Time	t_{LO_OVLO}			1		µs
Low-Side Input Undervoltage Lockout Threshold	$V_{LO\_UVLO–}$		**8.0**	8.6		V
Low-Side Input Undervoltage Recovery Threshold	V_{LO_UVLO+}			10.5	**10.8**	V
Low-Side Input Undervoltage Lockout Hysteresis	$V_{LO\_UVLO\_HYST}$			0.1		V
Low-Side Input Undervoltage Lockout Response Time	t_{LO_UVLO}			8		µs
Input-to-Output Start-Up Delay	$t_{LO\_TO\_HI\_DELAY}$	From $V_{LO\_DC} = V_{LO\_UVLO+}$ to powertrain active, EN floating (i.e., one-time start-up delay from application of V_{LO_DC} to V_{HI_DC})			600	ms
High-Side Output Soft-Start Ramp Time	$t_{HI\_SOFT\_START}$	From powertrain active.		500		µs
High-Side Output Overcurrent Trip Threshold	$I_{HI\_OUT\_OCP}$	Protection will stop powertrain; conduction path from low side to high side still exists through body diodes of powertrain MOSFETs [a]	**15.25**	18.75	**27.5**	A
High-Side Output Overcurrent Response Time Constant	$t_{HI\_OUT\_OCP}$	Effective internal RC filter	2	5		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC	**125**			°C
Overtemperature Recovery Threshold	$t_{OTP–}$		105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC			–45	°C

[a] Sustained current through body diodes can cause powertrain damage. See "start up and bidirectional operation" on page 21.

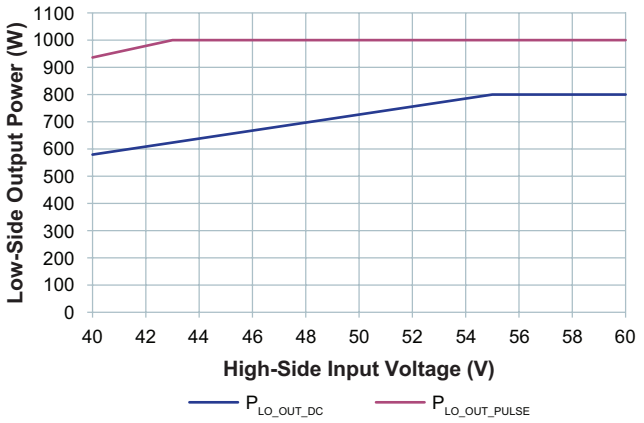
Operating Area





Note: Generic SM-ChiP™ package shown. Representation may not match specific footprint of the product in this data sheet.

Figure 1 — *Specified thermal operating area*



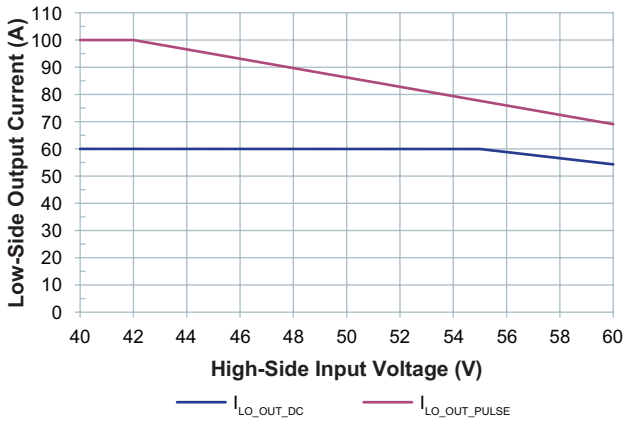
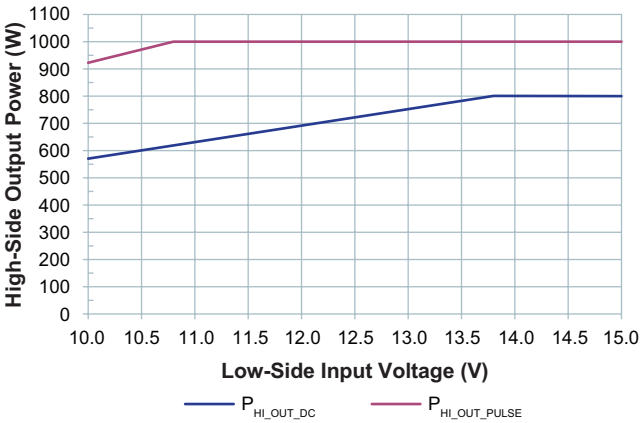


Figure 2 — *Specified electrical operating area, step-down operation*



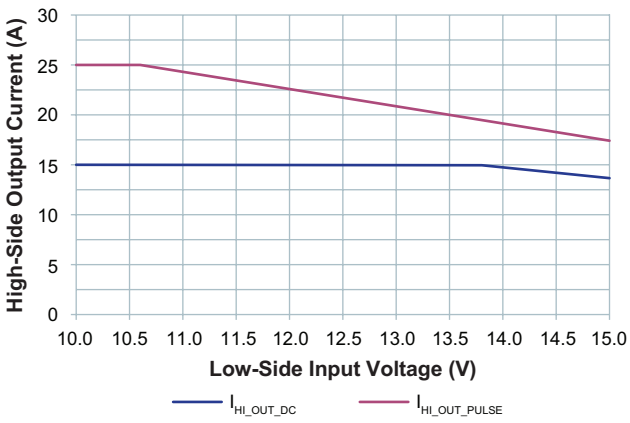


Figure 3 — *Specified electrical operating area, step-up operation*

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Temperature Monitor / Output Good (TM / OG)

- The TM/OG pin provides temperature monitoring and power good functionalities.
- The TM/OG is internally held low (0V) until the start up has completed.
- This signal can be used to drive logic circuit downstream for delayed enable of the load.
- After start up, this pin provides a voltage proportional to the absolute temperature of the converter control IC.
- For more information, see signal pin description section, page 21.

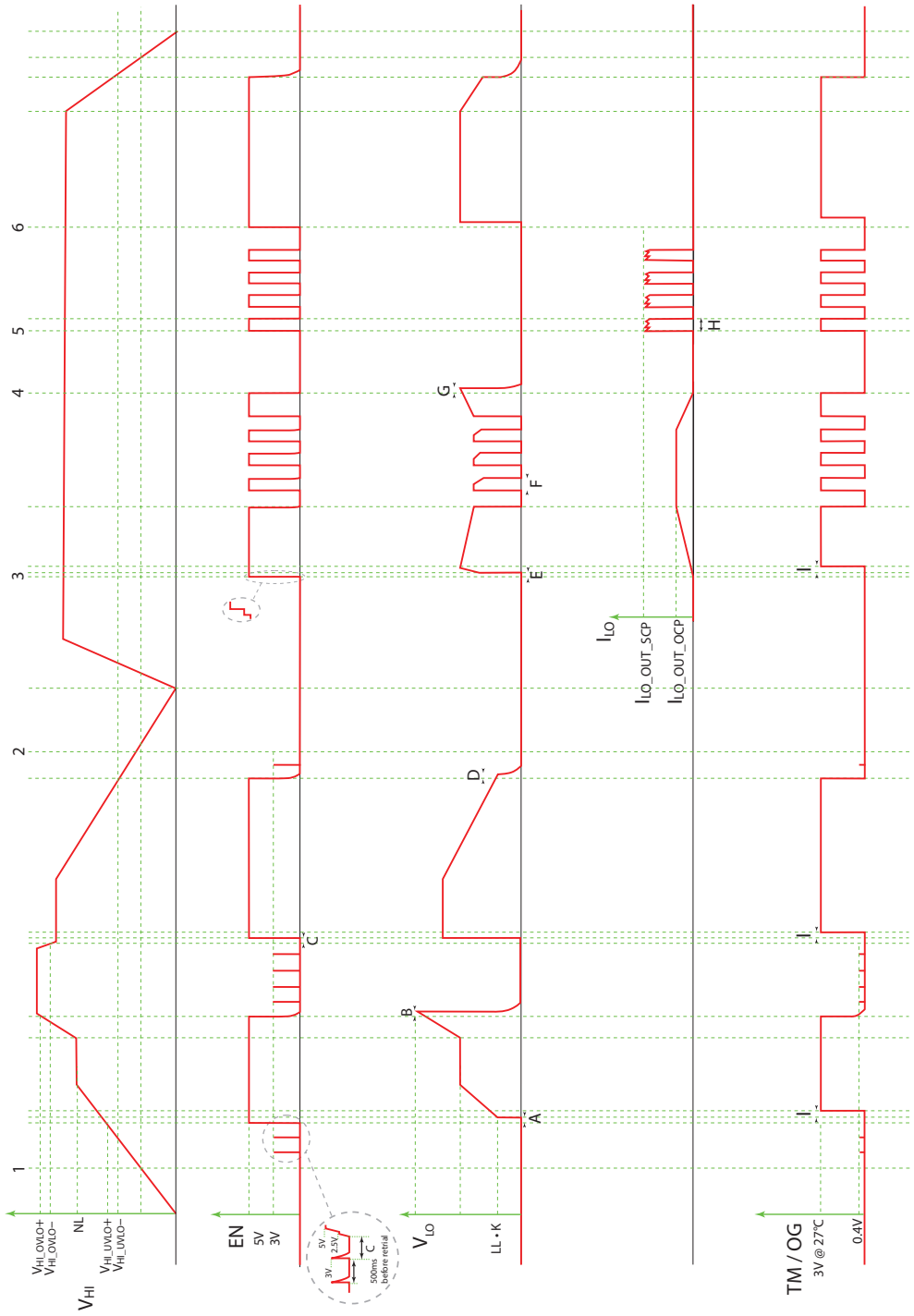
Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Start Up	Powertrain active to TM / OG time	$t_{TM/OG}$	Powertrain active to TM / OG high		1800		µs
	Regular Operation	TM / OG Voltage Range	$V_{TM/OG}$		**2.12**		**4.04**	V
		TM / OG Voltage Reference	V_{TM/OG_AMB}	T_J controller = 27°C	2.95	3.00	3.05	V
		TM / OG Source Current	$I_{TM/OG}$	TM accuracy = ±5°C			**10**	µA
		TM / OG Short Circuit Current	$I_{SC\_TM/OG}$	Maximum source current when pulled to ground externally			**5**	mA
		TM / OG Gain	$A_{TM/OG}$			10		mV / °C
		TM / OG Voltage Ripple	V_{TM/OG_PP}	$C_{TM/OG}$ = 0pF, V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 60A		120	**200**	mV
Digital Input / Output	Transition	TM / OG Capacitance (External)	C_{TM/OG_EXT}				**50**	pF
		TM / OG Fault Response Time	$T_{FR\_TM/OG}$	From fault to TM / OG low		10		µs
	Standby	TM / OG Voltage	V_{TM/OG_DIS}	TM/OG held low by internal FET		0		V
		TM / OG Sinking Current	$I_{SINK\_TM/OG}$	Maximum current TM/OG can sink when pulled low by internal FET			**180**	mA

Enable / Disable Control (EN)

- The EN pin enables and disables the NBM. When held low, the NBM is disabled.
- In an array of NBM modules, EN pins should be interconnected to synchronize start up.
- Unit must not be disabled if a load is present on $+V_{HI}$ while operating in step-up mode.
- EN pin outputs 5V during normal operation.
- For more information, see signal pin description, see signal pin description section, page 21.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Regular Operation	EN Voltage	V_{EN}		**4.7**	5.0	**5.3**	V
		EN Available Current	I_{EN_OP}		**2.0**	3.5	5.0	mA
	Standby	EN Source (Current)	I_{EN_EN}		**50**	100		µA
		EN Resistance (Internal)	R_{EN_INT}	Internal pull-down resistor	**50**	150	**400**	kΩ
	Transition	EN Capacitance (Internal)	C_{EN_INT}				**1000**	pF
	Start Up	EN Load Resistance	R_{EN_S}	To permit regular operation	**60**			kΩ
Digital Input / Output	Regular Operation	EN Enable Threshold	$V_{EN\_EN\_TH}$		**2.0**	2.5	**3.0**	V
		EN Disable Threshold	$V_{EN\_DIS\_TH}$				**1.95**	V
	Standby	EN Disable Duration	$t_{EN\_DIS\_t}$	Minimum time before attempting re-enable	**1**			s
	Transition	EN Threshold Hysteresis	V_{EN_HYSTER}			50		mV
		EN Enable to Powertrain Active Time	t_{EN_START}	V_{HI_DC} > V_{HI_UVLO+}, EN held low. Both conditions satisfied for time > $t_{HI\_TO\_LO\_DELAY}$	5	10	30	µs
		EN Disable to V_{OUT} Time	t_{EN_DIS}			4	**10**	µs
		EN Fault Response Time	t_{FR_EN}	From fault to EN low		100		µs

NBM Step-Down Operation Timing Diagram



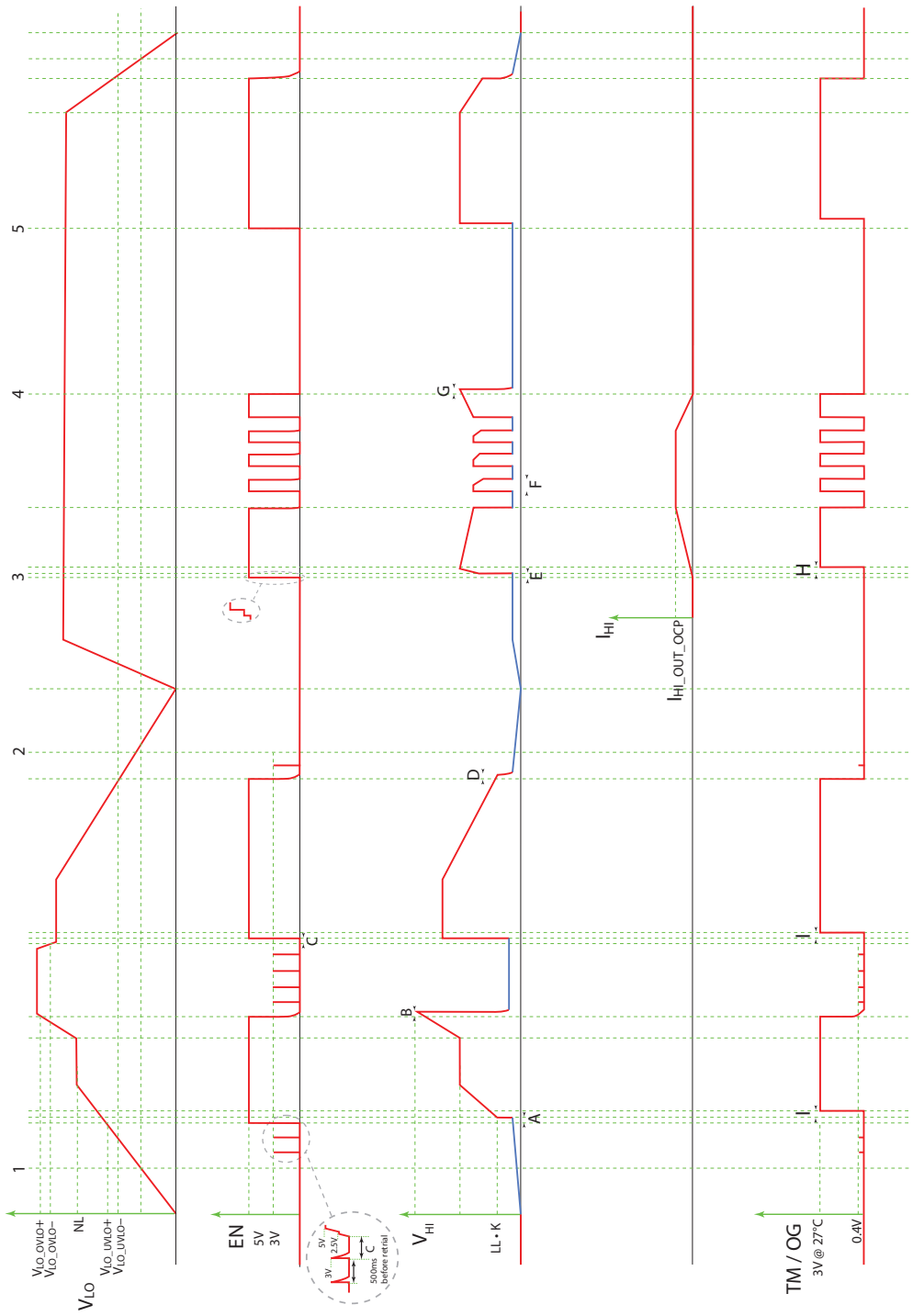
Notes:
– Timing and signal amplitudes are not to scale
– Error pulse width is load dependent

1: Controller start
2: Controller turn off
3: EN release
4: EN pulled low
5: EN released on low-side SC
6: Low-side SC removed

A: $t_{HI\_UVLO+\_DELAY}$
B: t_{HI_OVLO*}
C: $t_{AUTO\_RESTART}$
D: t_{UVLO}
E: t_{EN_START}
F: $t_{LO\_OUT\_OCP}$
G: t_{EN_DIS}
H: $t_{LO\_OUT\_SCP**}$
I: $t_{TM/OG}$

* Min value switching off
** From detection to powertrain shut down

NBM Step-Up Operation Timing Diagram



A: $t_{LO\_UVLO+\_DELAY}$
B: t_{LO_OVLO*}
C: $t_{AUTO\_RESTART}$
D: t_{UVLO}
E: t_{EN_START}
F: $t_{HI\_OUT\_OCP}$
G: t_{EN_DIS}
H: $t_{TM/OG}$

1: Controller start
2: Controller turn off
3: EN release
4: EN pulled low
5: Thermal fault removed

* Min value switching off

Notes:
– Timing and signal amplitudes are not to scale
– Error pulse width is load dependent
– Blue line: A conduction path from low side to high side exists through body diodes of powertrain MOSFET. When the powertrain is disabled and V_{LO} present, a voltage equal to V_{LO} minus the body diode drops will appear on the HI side.

Application Characteristics, Step-Down Operation

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-down mode, processing power from high-voltage side to low-voltage side. See associated figures for general trend data.

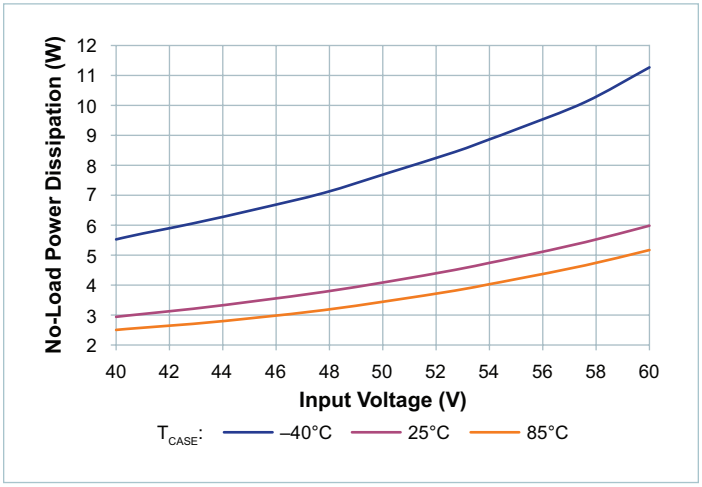


Figure 4 — *No-load power dissipation vs. V_{HI_DC}*

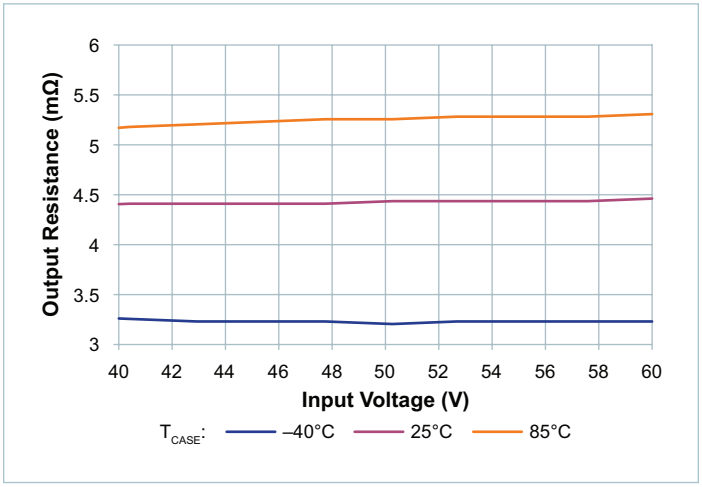


Figure 5 — *R_{LO} vs. R_{HI_IN}, I_{LO_DC} = 60A*

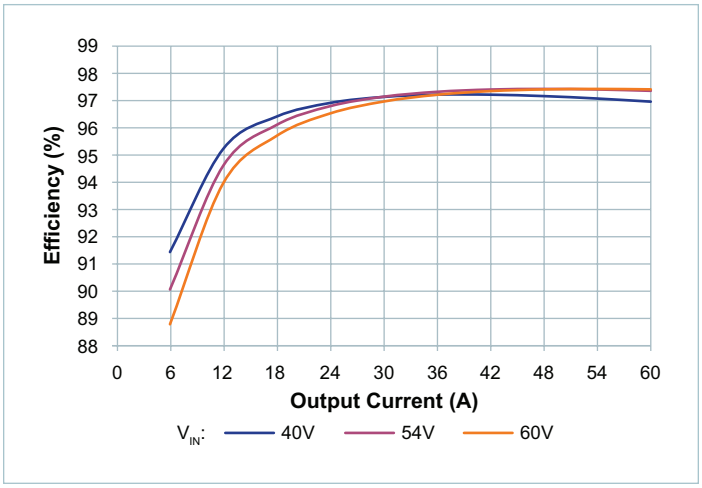


Figure 6 — *Efficiency at T_{CASE} = –40°C*

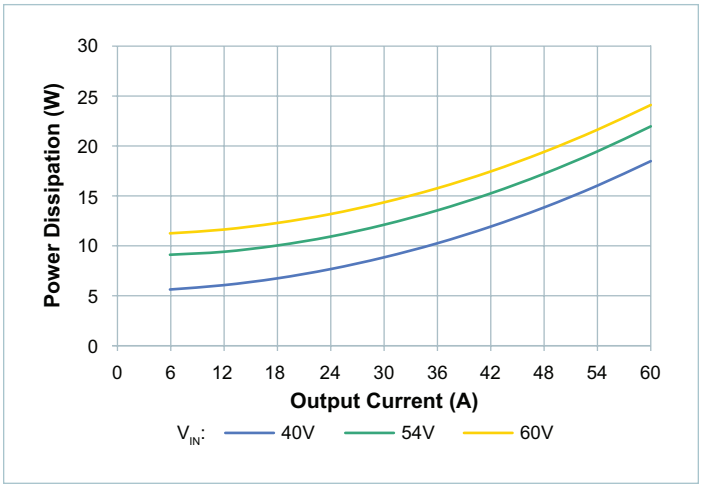


Figure 7 — *Power dissipation at T_{CASE} = –40°C*

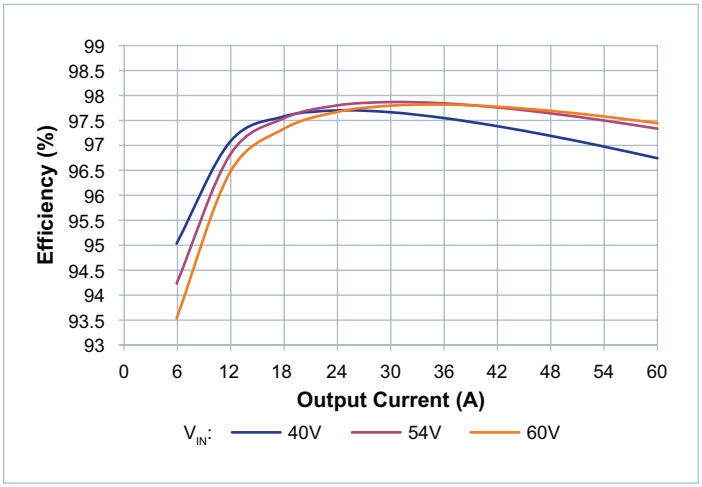


Figure 8 — *Efficiency at T_{CASE} = 25°C*

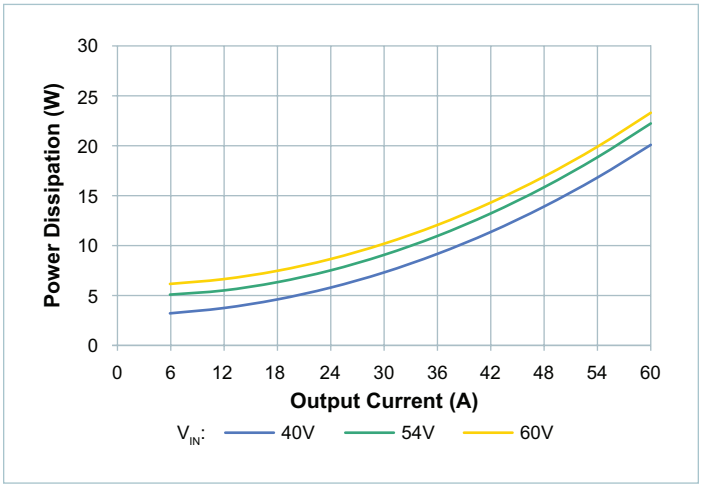


Figure 9 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics, Step-Down Operation (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-down mode, processing power from high-voltage side to low-voltage side. See associated figures for general trend data.

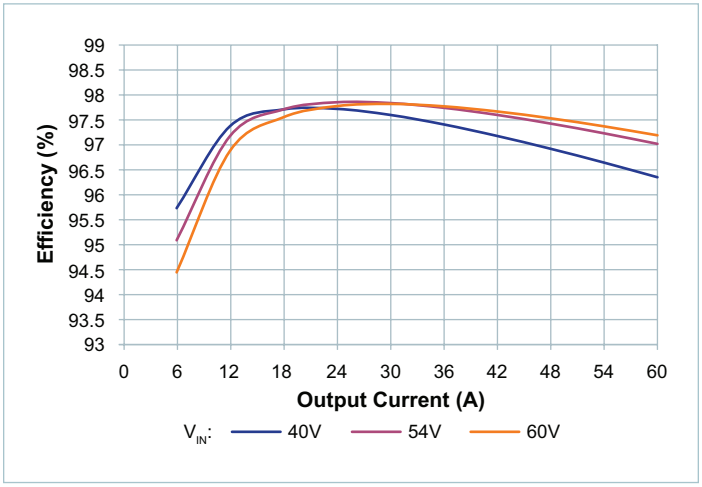


Figure 10 *— Efficiency at T_{CASE} = 85°C*

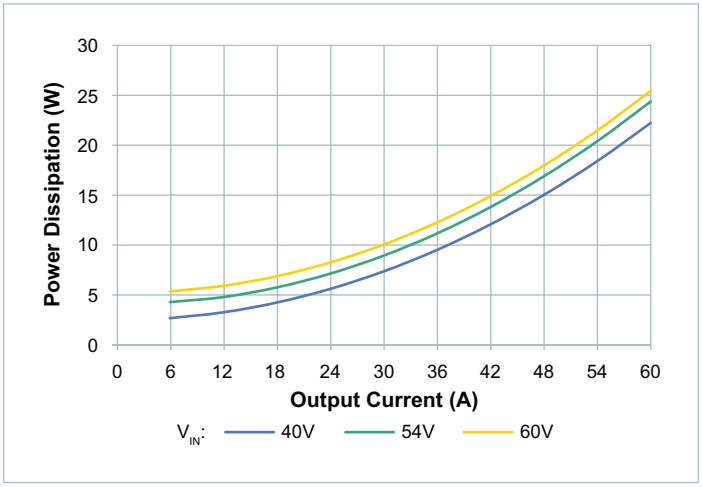


Figure 11 *— Power dissipation at T_{CASE} = 85°C*

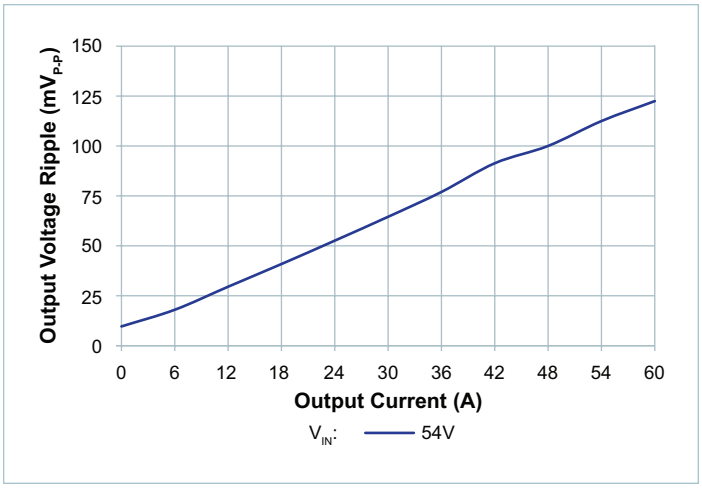


Figure 12 *— $V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; no external $C_{LO\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

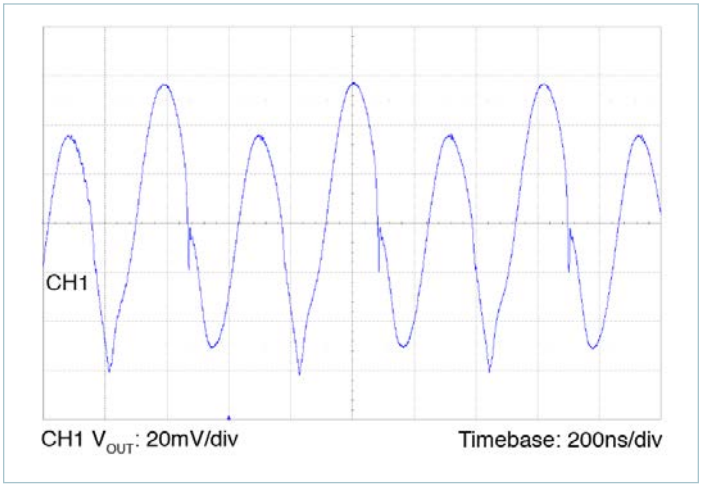


Figure 13 *— Full-load low-side voltage ripple, 68µF $C_{HI\_IN\_EXT}$, no external $C_{LO\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

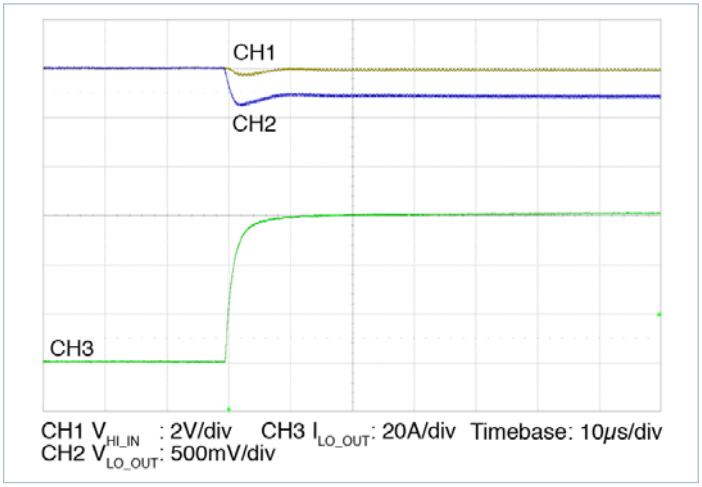


Figure 14 *— 0 – 60A transient response: $C_{HI\_IN\_EXT}$ = 68µF, no external $C_{LO\_OUT\_EXT}$*

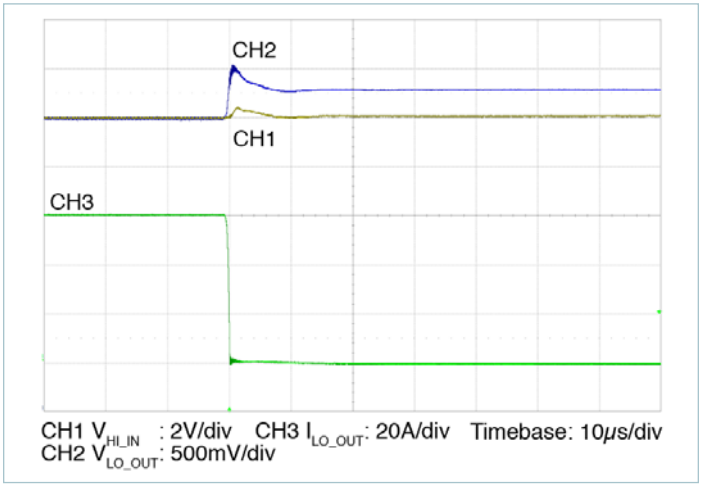


Figure 15 *— 60 – 0A transient response: $C_{HI\_IN\_EXT}$ = 68µF, no external $C_{LO\_OUT\_EXT}$*

Application Characteristics, Step-Down Operation (Cont.)

Temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-down mode, processing power from high-voltage side to low-voltage side. See associated figures for general trend data.

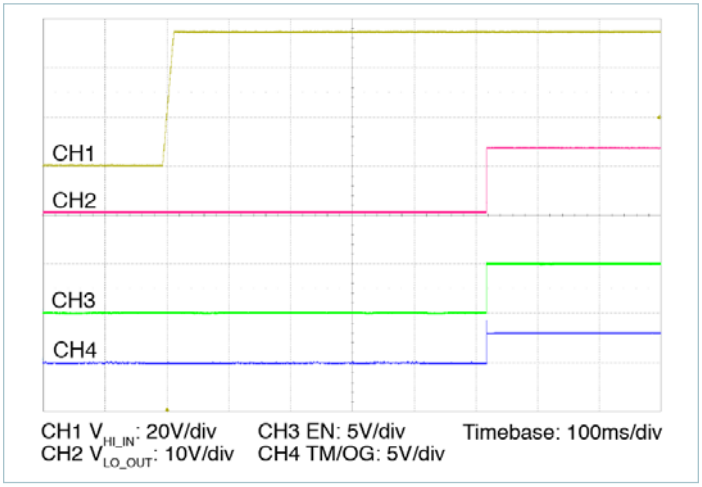


Figure 16 — *Start up from application of V_{HI_DC} = 54V, $C_{LO\_OUT\_EXT}$ = 1000µF, no load*

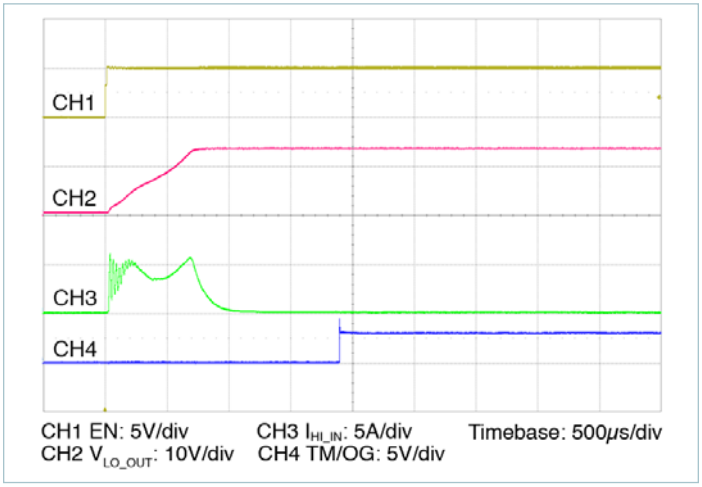


Figure 17 — *Start up from application of EN with pre-applied V_{HI_DC} = 54V, $C_{LO\_OUT\_EXT}$ = 1000µF, no load*

Application Characteristics, Step-Up Operation

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-up mode, processing power from low-volage side to high-voltage side. See associated figures for general trend data.

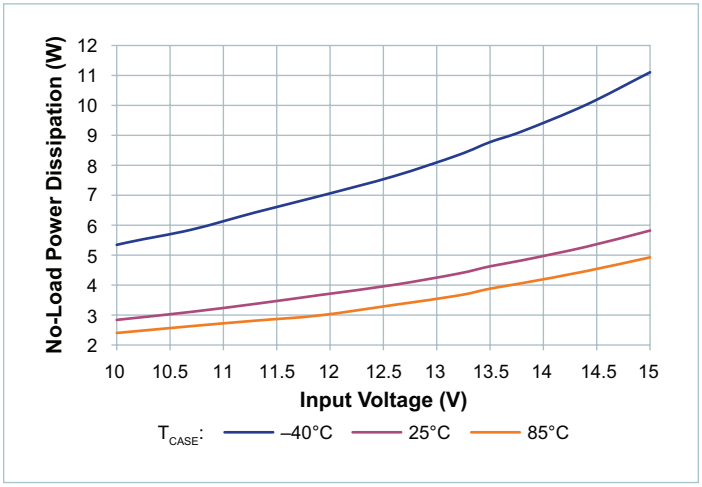


Figure 18 — *No-load power dissipation vs. V_{LO_DC}*

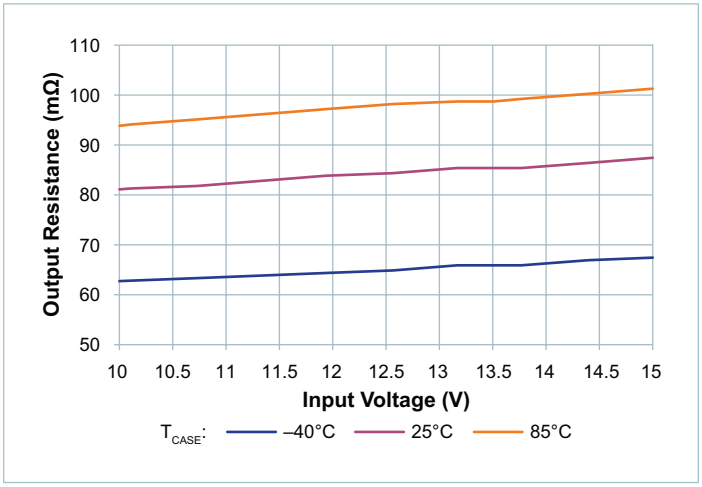


Figure 19 — *R_{HI} vs. R_{LO_IN}, I_{HI_DC} = 15A*

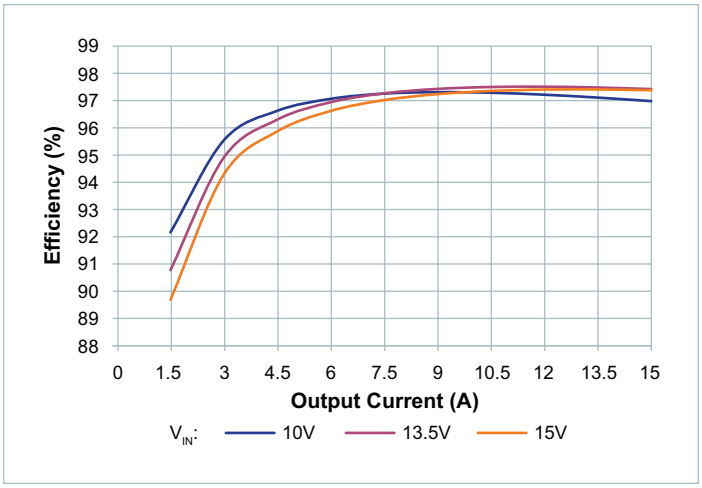


Figure 20 — *Efficiency at T_{CASE} = –40°C*

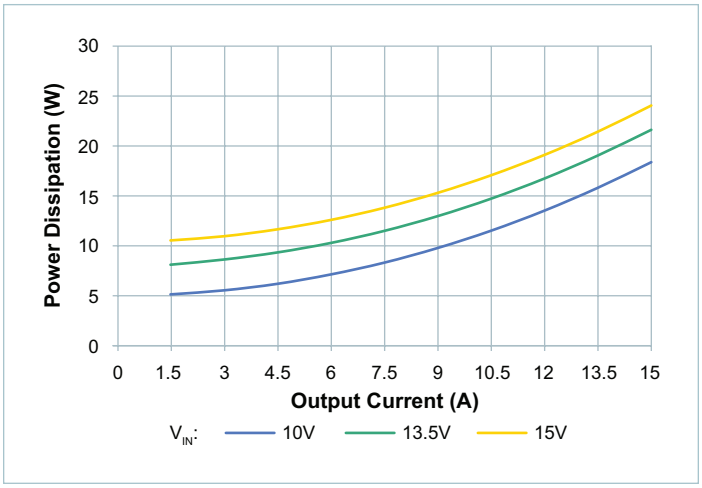


Figure 21 — *Power dissipation at T_{CASE} = –40°C*

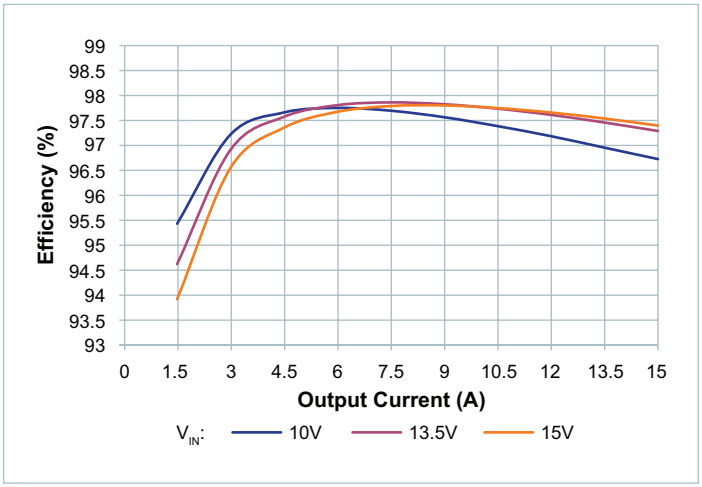


Figure 22 — *Efficiency at T_{CASE} = 25°C*

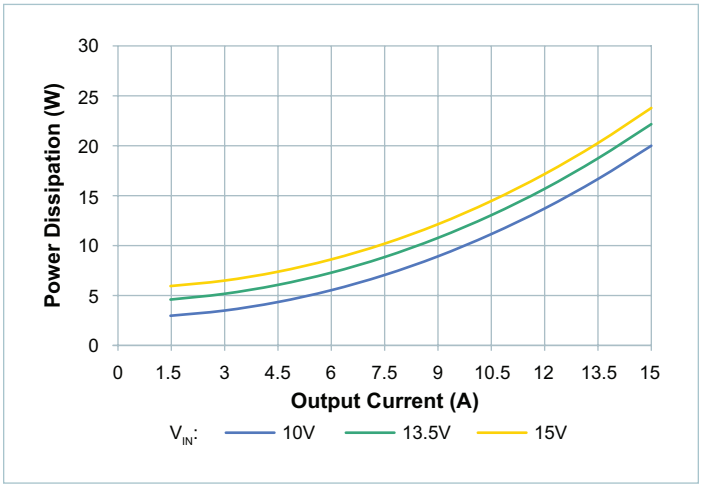


Figure 23 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics, Step-Up Operation (Cont.)

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-up mode, processing power from low-volage side to high-voltage side. See associated figures for general trend data.

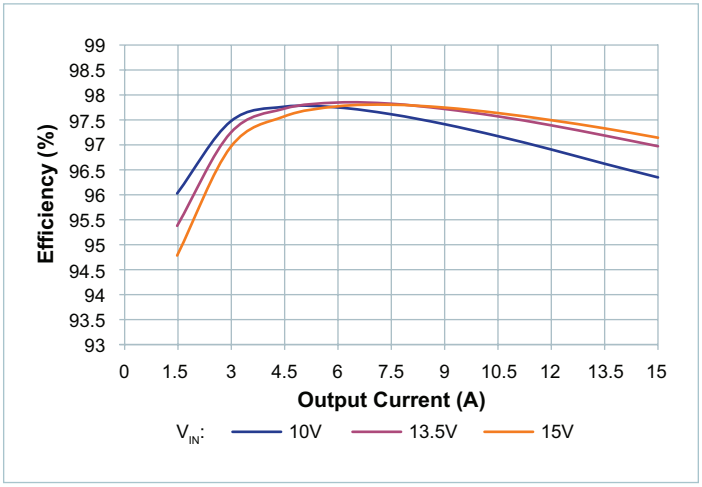


Figure 24 *— Efficiency at T_{CASE} = 85°C*

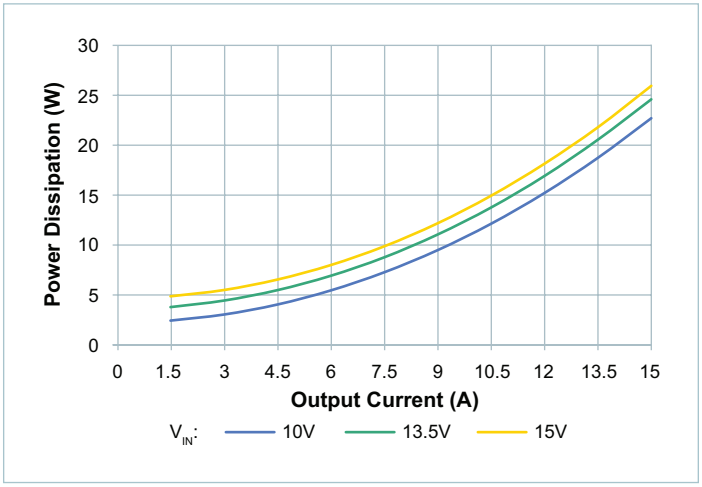


Figure 25 *— Power dissipation at T_{CASE} = 85°C*

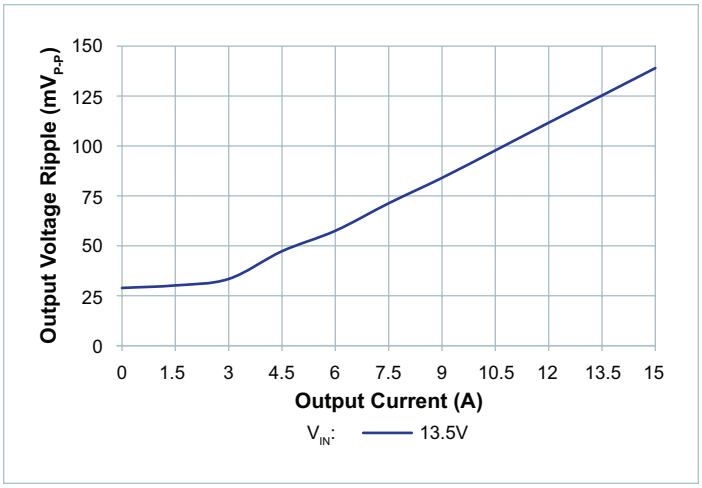


Figure 26 *— $V_{HI\_OUT\_PP}$ vs. I_{HI_DC} ; no external $C_{HI\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

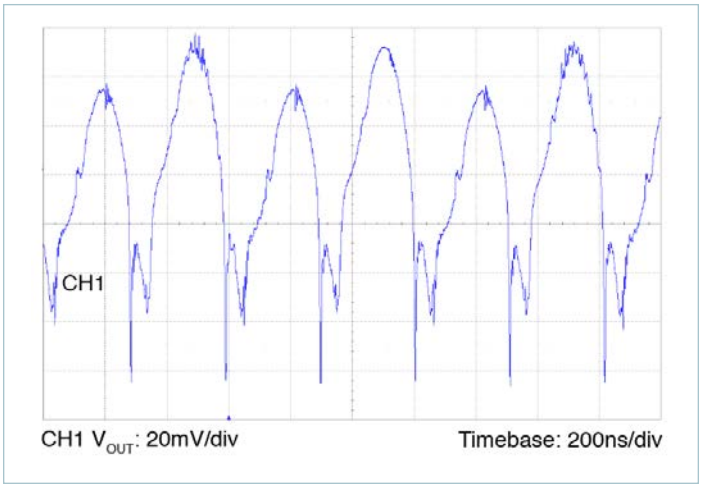


Figure 27 *— Full-load high-side output voltage ripple, 1000µF $C_{LO\_IN\_EXT}$; no external $C_{HI\_OUT\_EXT}$. Board-mounted module, scope setting: 20MHz analog BW*

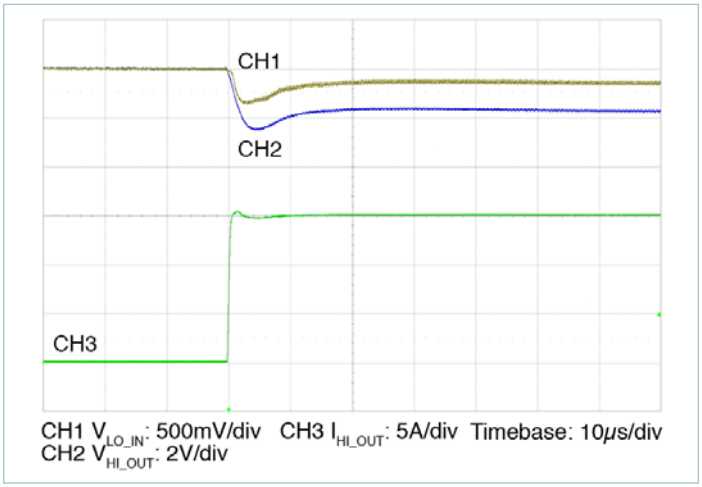


Figure 28 *— 0 – 15A transient response: $C_{LO\_IN\_EXT}$ = 1000µF, no external $C_{HI\_OUT\_EXT}$*

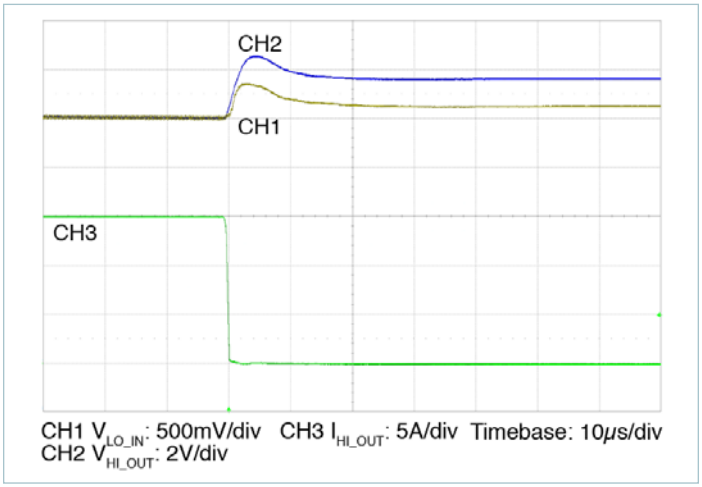


Figure 29 *— 15 – 0A transient response: $C_{LO\_IN\_EXT}$ = 1000µF, no external $C_{HI\_OUT\_EXT}$*

Application Characteristics, Step-Up Operation (Cont.)

Temperature controlled via top-side cold plate, unless otherwise noted. All data presented in this section are collected from units operating in step-up mode, processing power from low-volage side to high-voltage side. See associated figures for general trend data.

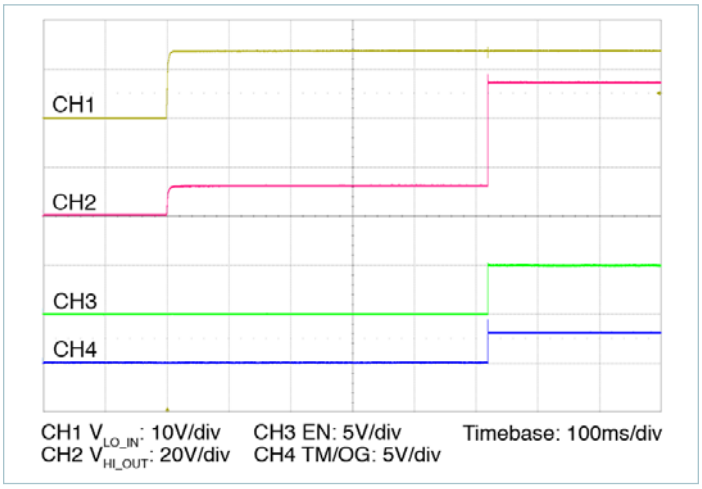


Figure 30 — *Start up from application of V_{LO_DC} = 13.5V, $C_{HI\_OUT\_EXT}$ = 68µF, no load*

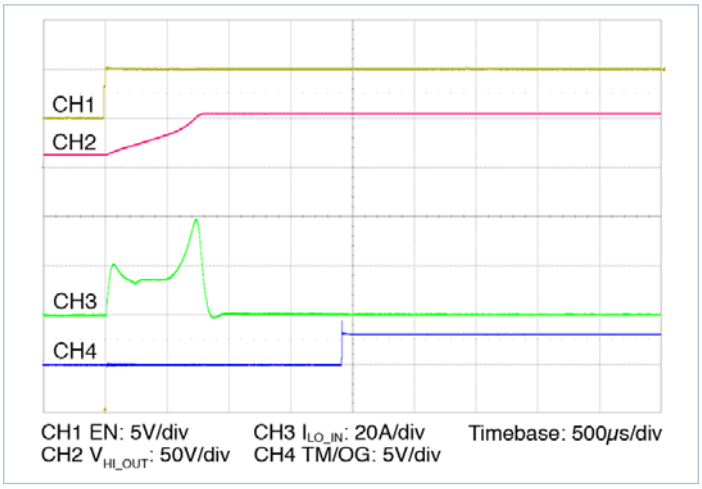


Figure 31 — *Start up from application of EN with pre-applied V_{LO_DC} = 13.5V, $C_{HI\_OUT\_EXT}$ = 68µF, no load*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); all other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		22.70 [0.894]	22.83 [0.899]	22.96 [0.904]	mm [in]
Width	W		17.21 [0.678]	17.34 [0.683]	17.47 [0.688]	mm [in]
Height	H		7.292 [0.287]	7.417 [0.292]	7.542 [0.297]	mm [in]
Volume	Vol	Without heatsink		2.94 [0.179]		cm^3 [in^3]
Weight	W			12 [0.423]		g [oz]
Exterior Package Plating		Nickel	100		300	µin
		Gold	2		5	
Thermal						
Operating Temperature	$T_{INTERNAL}$	NBM2317S60E1560T0R (T-Grade)	–40		125	°C
Assembly						
Storage Temperature		NBM2317S60E1560T0R (T-Grade)	–40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2kV)				
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)				
Soldering						
Peak Temperature During Reflow		MSL 4			245	°C
Safety						
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		6.46		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		15.0		MHrs
Agency Approvals / Standards		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Signal Pin Descriptions

Enable Control (EN)

The EN pin enables and disables the NBM. When held low, the NBM is disabled. When allowed to float with an impedance to PGND greater than 60kΩ, the module will start. In an array of NBM modules, EN pins should be interconnected to synchronize start up. The NBM modules will start simultaneously when enabled.

The EN pin is capable of being either driven high by an external open collector or open drain logic signal or internal pull up to 5V (operating). EN pin outputs 5V during normal operation. Note that EN pin does not have current sink capability. Therefore, in an array configuration of multiple NBMs, the EN pin of one unit is not capable of disabling other modules in the event of a fault condition. The EN pin must not be driven high by directly applying an external voltage.

Temperature Monitor and Output Good (TM / OG)

The TM / OG pin provides temperature monitoring and power good functionalities. It can be used to accomplish the following two functions.

- *Monitor the control IC temperature*

  This pin provides a voltage proportional to the absolute temperature of the converter control IC. It monitors the internal junction temperature of the controller IC within an accuracy of ±5°C. It has a room temperature set point of ~3.0V and an approximate gain of 10mV/°C. The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e., 3.0V = 300K = 27°C).

  The following equation can be used to calculate the equivalent TM voltage in Volts for a given junction temperature (T_J) in °C.

$$TM(V) = \frac{1}{100}\left(T_J\right) + 2.73$$

  The following equation can be used to calculate the junction temperature (T_J) in °C for a given TM voltage in Volts.

$$TM(^{o}C) = (TM - 2.73) \bullet 100$$

- *Output Good flag*

  This pin will be internally held low (0V) by an internal pull-down FET until the start up has completed. When the output voltage is in a steady state condition after the completion of the soft start, it will internally be released and can be used as a "Ready to process full load current" flag.

  This signal can be used to drive logic circuitry downstream for delayed enable or connection of the load. It can also be used as "Fault flag", as the pin is pulled low internally when a fault is detected.

Start Up and Bidirectional Operation

The NBM2317S60E1560T0R is capable of start up in both directions of operation (step-up and step-down) once the applied voltage is greater than the undervoltage lockout threshold.

The non-isolated bus converter module is fully bidirectional. Once the unit is enabled, the NBM2317S60E1560T0R will operate in step-up mode, transferring energy from low side to the high side, whenever the low-side voltage exceeds $V_{HI} \bullet K$. The NBM2317S60E1560T0R module will operate in step-down mode, transferring energy from high side to the low side, whenever the high-side voltage exceeds V_{LO} / K.

Loading must be delayed until completion of start up. The output good (OG) signal can be used to determine when the start-up has completed and the load can be safely enabled. A load must not be present on the $+V_{HI}$ pin if the powertrain is not actively switching and $+V_{LO}$ is present: remove any HI-side load prior to disabling the module.

Conduction from LO to HI side through powertrain MOSFET body diodes will occur if the unit stops switching while a load is present on the HI side and $+V_{LO}$ is present. In other words, if the powertrain is disabled through EN pin or by any protection and V_{LO} is present, then a voltage equal to V_{LO} minus the body diode drops will appear on the HI side. Note that in this condition the NBM does not have a current-limiting mechanism from +LO to +HI. The built-in short-circuit protection will stop the powertrain switching in case of a fault on the HI side; however external circuitry will be needed to limit the fault current and remove faults.

SM-ChiP™ NBM

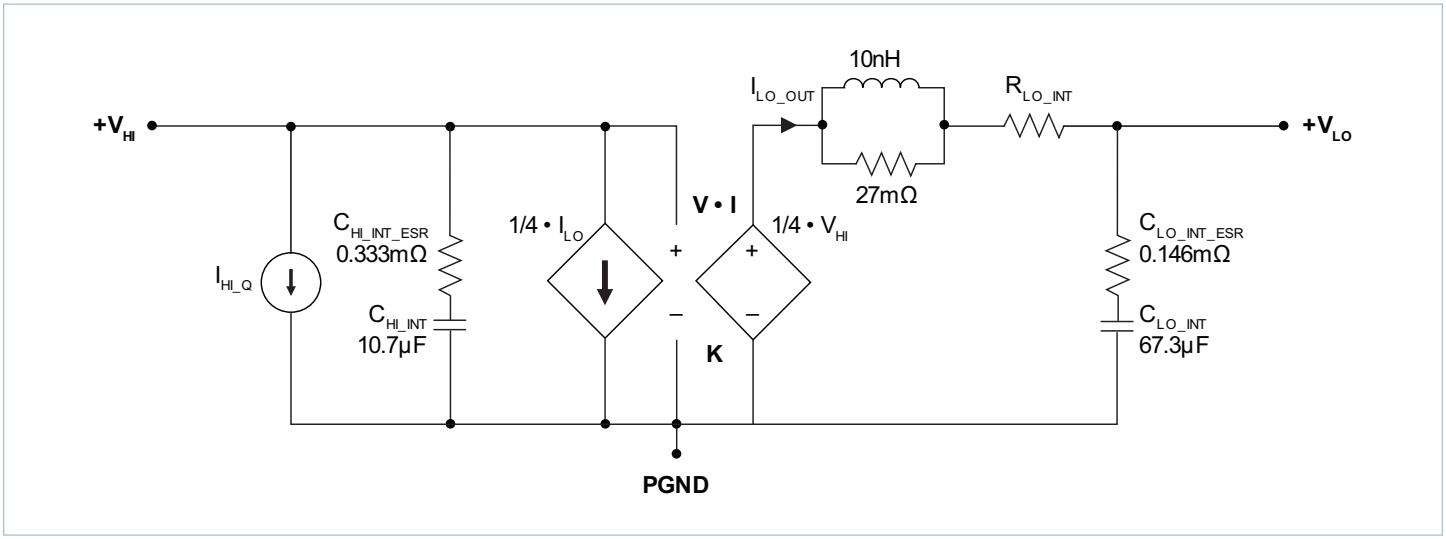


Figure 34 — *NBM AC model*

The NBM uses a high-frequency resonant tank to move energy from high-voltage side to low-voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the high-side voltage and the low-side current. A small amount of capacitance embedded in the high-voltage side and low-voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The NBM2317S60E1560T0R can be simplified into the model shown in Figure 34.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the NBM.
Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the NBM, and is a function of the R_{DS_ON} of the high-side and low-side MOSFETs and the winding resistance of the power transformer. I_{HI_Q} represents the quiescent current of the NBM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI}.

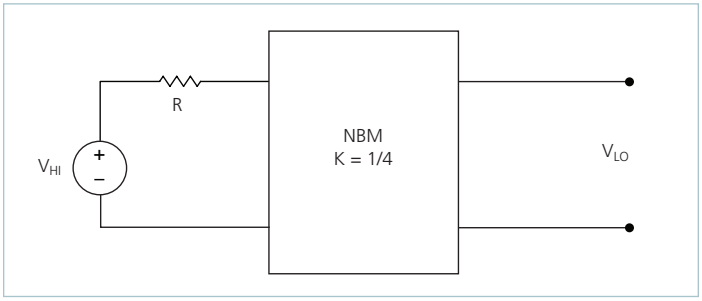


Figure 35 — *K = 1/4 NBM with series high-side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the NBM. However, in this case a real resistor, R, on the high side of the NBM is effectively scaled by K^2 with respect to the low side.

Assuming that R = 1Ω, the effective R as seen from the low side is 62.5mΩ, with K = 1/4.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the high-voltage side of the NBM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 36.

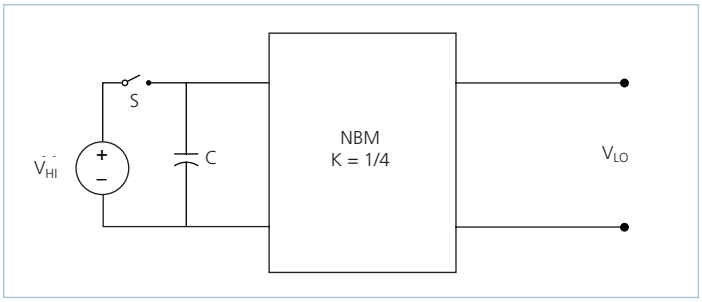


Figure 36 — *NBM with high-side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized NBM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the low side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low side when expressed in terms of the high side. With K = 1/4 as shown in Figure 36, C = 1µF would appear as C = 16µF when viewed from the low side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a NBM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the NBM is too high. The impedance of the NBM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the NBM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the NBM are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the NBM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Input and Output Filter Design

A major advantage of NBM systems versus conventional PWM converters is that the auto-transformer based NBM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of high-side voltage and low-side current and efficiently transfers charge through the auto-transformer. A small amount of capacitance embedded in the high-side and low-side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the NBM's dynamic response, the impedance presented to its high-side terminals must be low from DC to approximately 5MHz. The connection of the non-isolated bus converter module to its power source should be implemented with minimal distribution inductance. In step-down operation, the interconnect inductance on the high side should not exceed 300nH; in step-up operation, the interconnect inductance on the low side should not exceed 20nH. If the interconnect inductance exceed these limits, the input side of the NBM should be bypassed with a RC damper or electrolytic capacitor to retain low source impedance and stable operation.

- *Further reduce high-side and/or low-side voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the high-side source will appear at the low side of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module high-side/low-side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating range.

Total load capacitance of the NBM module shall not exceed the specified maximum. Owing to the wide bandwidth and low low-side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the high side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the high side appears as effective capacitance on the low side per the relationship defined in Equation 13.

$$C_{LO\_EXT} = \frac{C_{HI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Current Sharing

The performance of the NBM topology is based on efficient transfer of energy through a auto-transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal auto-transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple NBMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that NBM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each NBM in an array is recommended to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays

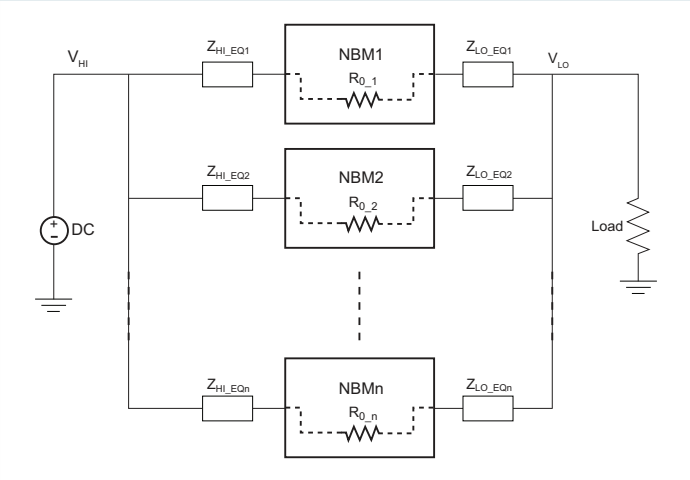


Figure 39 — *NBM parallel array*

Fuse Selection

In order to provide flexibility in configuring power systems, SM-ChiP modules are not internally fused. Input line fusing of SM-ChiP products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of NBM)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: see agency approval

Thermal Considerations

The SM-ChiP™ module provides a high degree of flexibility in that it presents several pathways to remove heat from the internal power dissipating components. Heat may be removed from the top surface, the bottom surface, the power pins and the signal pins. The extent to which these surfaces are cooled is a key component in determining the maximum current that is available from an SM-ChiP, as can be seen from Figures 2 and 3.

Since the SM-ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are many pathways to remove heat from the SM-ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors.

Figure 40(a) shows the "thermal circuit" for a NBM2317 SM-ChiP in two-sided cooling application, where the product is cooled through the PCB at the bottom and a heat sink at the top. In this case, the NBM power dissipation is $P_{DISSIPATION}$ and the top and bottom (heat sink and PCB) surface temperatures are represented as $T_{TOP\_HEAT\_SINK}$ and T_{PCB}. This thermal system can now be very easily analyzed as an electrical network with simple resistors, voltage sources, and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

Figure 40(b) shows the thermal model for an application with single-side cooling, where the heat is dissipated through the PCB only. In this case, the heat flow path to the top heat sink is removed; the top of the package now contributes to the cooling into the PCB via the package metalization (i.e., the θ_{PGND_TOP} and $\theta_{PGND\_TOP\_BOTTOM}$ resistances are in series between the maximum internal temperature point and the PCB temperature).

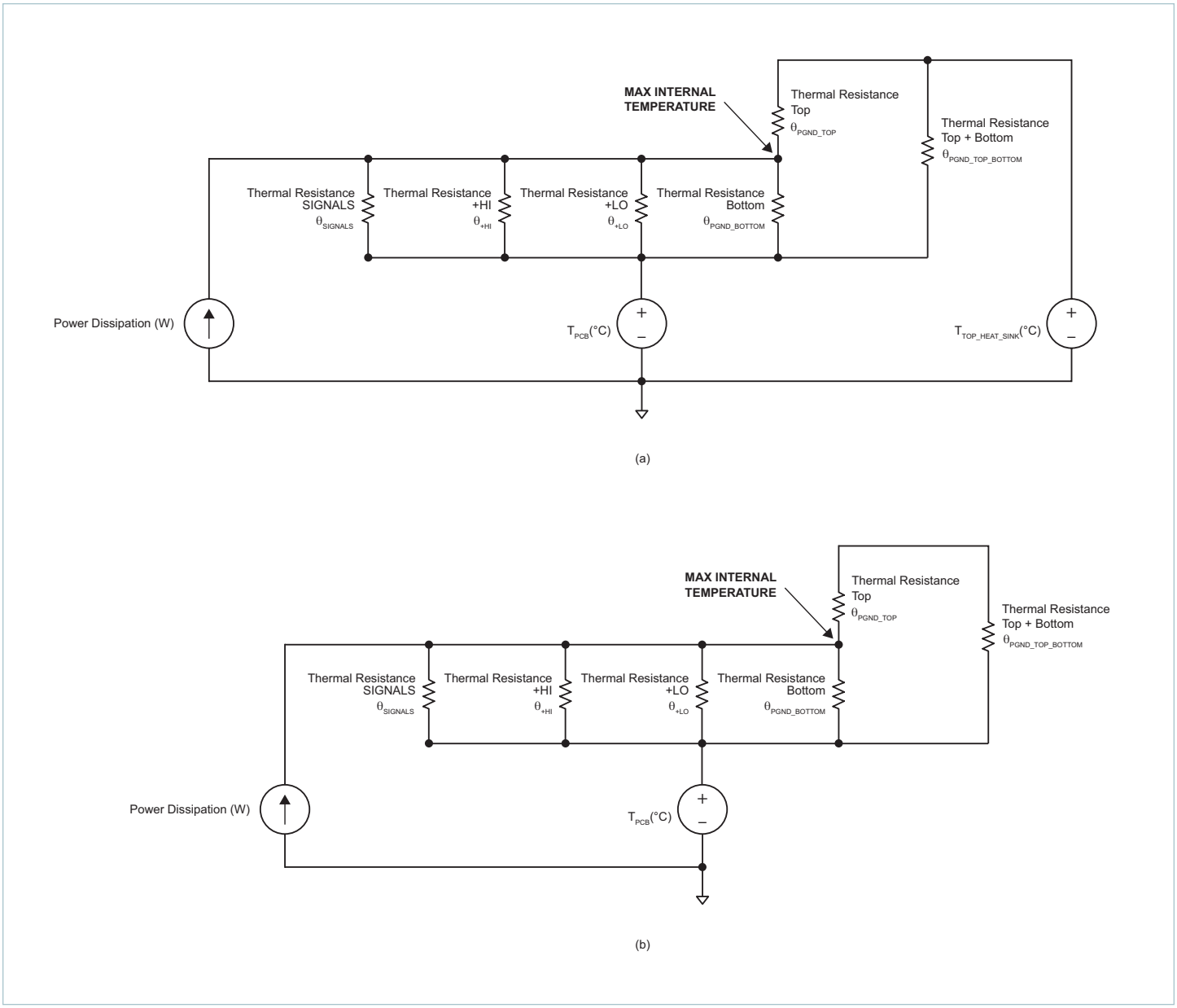


Figure 40 — *NBM2317S60E1560T0R two-sided cooling thermal model (a) and bottom-side cooling only (through PCB) thermal model (b).*

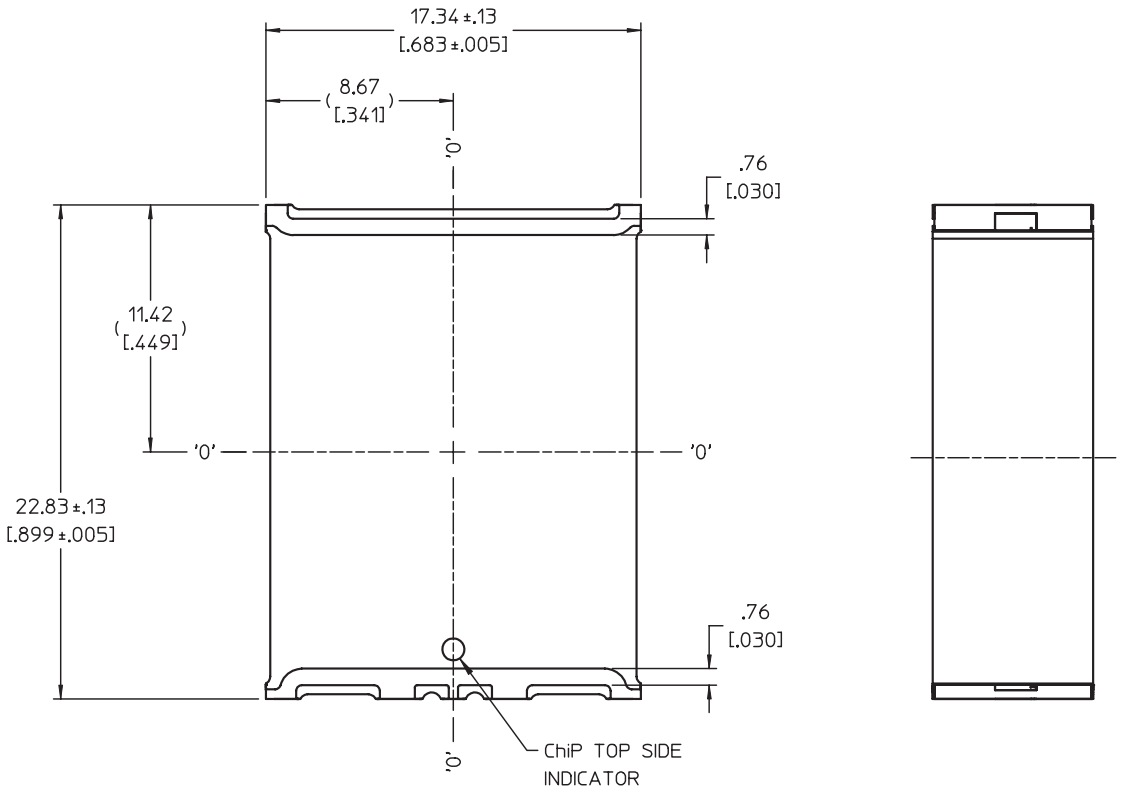
Where the symbol in Figure 40 is defined as the following:

$\theta_{SIGNALS}$	Estimated thermal resistance from TM/OG and EN signal pins to maximum temperature internal component.
θ_{+HI}	Estimated thermal resistance from +HI pins to maximum temperature internal component.
θ_{+LO}	Estimated thermal resistance from +LO pin to maximum temperature internal component.
θ_{PGND_BOTTOM}	Estimated thermal resistance from bottom of PGND to maximum temperature internal component.
θ_{PGND_TOP}	Estimated thermal resistance from top of PGND to maximum temperature internal component.
$\theta_{PGND\_TOP\_BOTTOM}$	Estimated thermal resistance between top and bottom of PGND.

Thermal Impedance					
$\theta_{SIGNALS}$ (°C / W)	θ_{+HI} (°C / W)	θ_{+LO} (°C / W)	θ_{PGND_BOTTOM} (°C / W)	θ_{PGND_TOP} (°C / W)	$\theta_{PGND\_TOP\_BOTTOM}$ (°C / W)
210	82	15	2.7	2.5	5.4

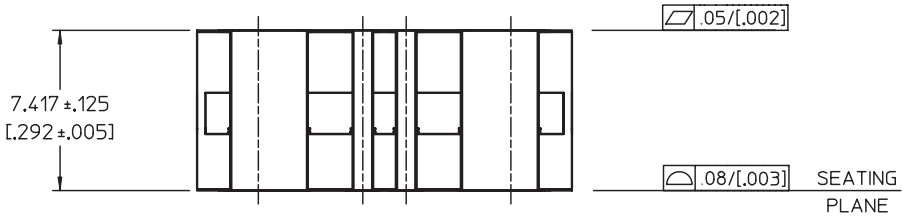
Table 1 — *Thermal impedances; assumes top and bottom cooling used*

NBM Package Drawing Top & Side View



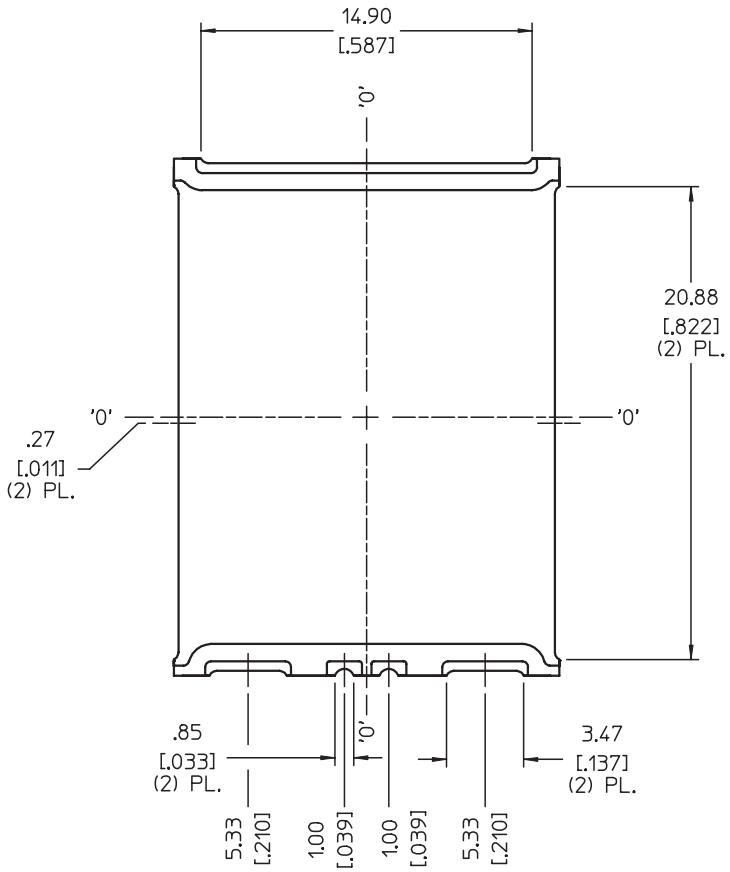
TOP VIEW (COMPONENT SIDE)

2317 NBM



NOTES:
1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]

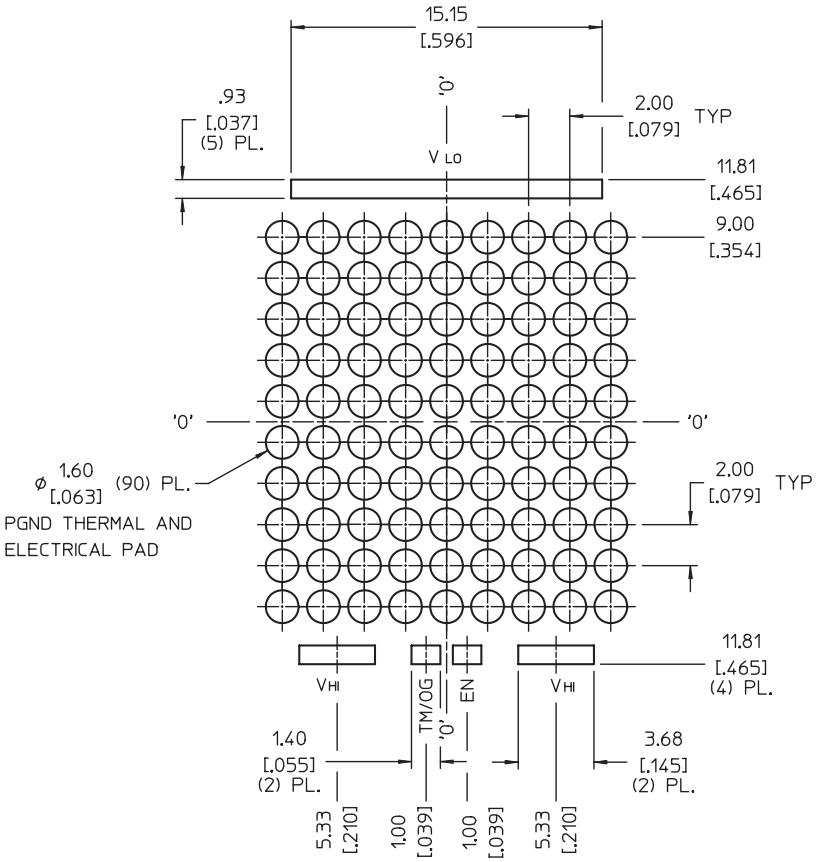
NBM Package Drawing Bottom View



BOTTOM VIEW

2317 NBM

NBM Recommended Land Pattern (Component Side)



RECOMMENDED LAND PATTERN,
2317 NBM

Revision History

Revision	Date	Description	Page Number(s)
1.0	08/27/18	Initial release	n/a
1.1	12/18/18	Updated features & benefits Updated specifications and performance characteristics	1 5 – 19
1.2	01/29/19	Updated specified electrical operating area Updated TM/OG characteristics Updated output good flag description	10 11 21
1.3	06/26/19	Updated electrical specifications Updated TM/OG signal characteristics Corrected height specifications to match mechanical drawing	6, 8 11 20
1.4	11/06/19	Typo correction to ESR values in AC model	22
1.5	09/02/20	Changed product voltage ratings to V_{HI} = 40 – 60V and V_{LO} = 10 – 15V Added exterior package plating specification	1, 6, 7, 8, 10, 14, 15, 17, 18 20

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Information furnished by Vicor is believed to be accurate and reliable. However, no responsibility is assumed by Vicor for its use. Vicor makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication. Vicor reserves the right to make changes to any products, specifications, and product descriptions at any time without notice. Information published by Vicor has been checked and is believed to be accurate at the time it was printed; however, Vicor assumes no responsibility for inaccuracies. Testing and other quality controls are used to the extent Vicor deems necessary to support Vicor's product warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Specifications are subject to change without notice.

Visit http://www.vicorpower.com/NBM-Non-isolated-Bus-Converter-Module for the latest product information.

Vicor's Standard Terms and Conditions and Product Warranty

All sales are subject to Vicor's Standard Terms and Conditions of Sale, and Product Warranty which are available on Vicor's webpage (http://www.vicorpower.com/termsconditionswarranty) or upon request.

Life Support Policy

VICOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF VICOR CORPORATION. As used herein, life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness. Per Vicor Terms and Conditions of Sale, the user of Vicor products and components in life support applications assumes all risks of such use and indemnifies Vicor against all liability and damages.

Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and Foreign Patents and pending patent applications) relating to the products described in this data sheet. No license, whether express, implied, or arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Numbers:
6,911,848; 6,930,893; 6,934,166; 7,145,786; 7,782,639; 8,427,269; 10,199,950; and for use under 6,975,098 and 6,984,965.

Contact Us: http://www.vicorpower.com/contact-us

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Vicor:

NBM2317S60E1560T0R NBM2317D60E1560T0R