TET1500 Series

AC-DC Front End Power Supplies

The TET1500 Series is a 1500 W AC to DC power-factor-corrected (PFC) power supply that converts standard AC or HVDC power into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

Key Features & Benefits

- High Efficiency, typ. 96% efficiency at half load
- Universal input voltage range: 90-305 VAC
- High voltage DC input: 180-400 VDC
- AC input with power factor correction
- Always-On standby output:
  - Programmable 3.3 V / 5 V (16.5 W)
- Hot-plug capable
- Parallel operation with active analog current sharing
- Digital controls for improved performance
- High density design: 35 W/in^3
- Small form factor (W x H x L): 54.5 x 40.0 x 321.5 mm
  2.14 x 1.57 x 12.66 in
- I2C communication interface for control, programming and monitoring with Power Management Bus protocol
- Over temperature, output over voltage and over current protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: OK and FAIL with fault signalling

Applications

- High Performance Servers
- Routers
- Switches

1. ORDERING INFORMATION

MODELS WITH PROGRAMMABLE 3.3 V / 5 V STANDBY OUTPUT

TET	1500	-	12	-	054	x	Ax
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
TET Front-Ends	1500 W		12 V		54 mm	N: Normal [1] R: Reverse [2]	A: C14 Socket AC: C16 Socket AH: HVDC Socket

[1] "N" Normal Airflow from Output connector to Input AC socket
[2] "R" Reverse Airflow from Input AC socket to Output connector

2. OVERVIEW

The TET1500 Series AC/DC power supply is combination of analog and DSP control, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal derating of output power with input voltage and temperature, the TET1500 power supply maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths. The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output, provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability. Status information is provided with front-panel LEDs.

In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

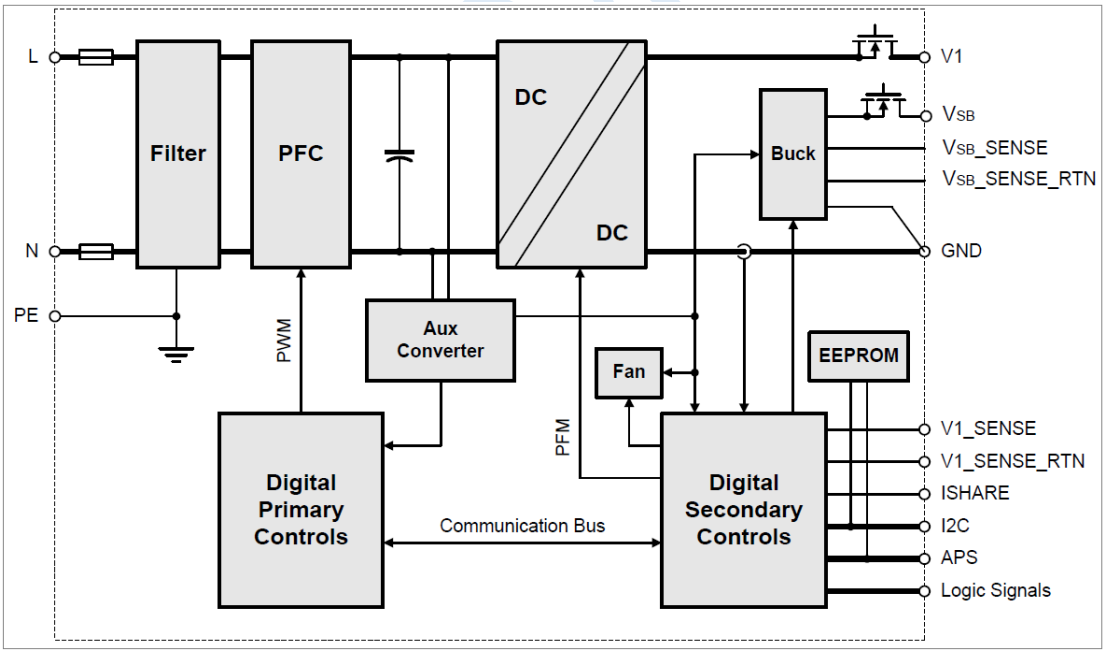


Figure 1. TET1500 Series Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi maxc	Maximum Input	Continuous			305 400	VAC VDC

4. INPUT SPECIFICATIONS

General Condition: T_A = 0… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal Input Voltage		100 200	230	277 350	VAC VDC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90 180		305 400	VAC VDC
Ii max	Max Input Current	Vin = 100 VAC, 836 W Vin = 200 VAC, 1500 W			*10* *9*	*Arms* *Arms*
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{PTC} = 25°C *(Figure 4)*			20	A_p
F_i	Input Frequency		40	50/60	70	Hz
PF	Power Factor	Vi = 230 VAC/277 VAC, 50 Hz and 60 Hz 10%, Load 20%, Load 50%, Load 100%, Load	 0.9 0.98 0.98 0.98		 	 W/VA W/VA W/VA W/VA
iTHD	Input iTHD	Vi = 230 VAC/277 VAC, 50 Hz and 60 Hz 10%, Load 20%, Load 50%, Load 100%, Load	 		 10 10 5 5	 % % % %
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	85 172		90 177	VAC VDC
$V_{i\,off}$	Turn-off Input Voltage	Ramping down	79 167		84 172	VAC VDC
η	Efficiency without Fan at AC input	V_{IN} = 230 VAC/277VAC, 10% load, T_A = 25°C V_{IN} = 230 VAC/277VAC, 20% load, T_A = 25°C V_{IN} = 230 VAC/277VAC, 50% load, T_A = 25°C V_{IN} = 230 VAC/277VAC, 100% load, T_A = 25°C	90 95 96 93			%
T_{Vout_hold}	12V1 Hold-up Time	After last AC zero point to $V_1 \geq$ 11.4 V, V_{SB} within regulation, V_i = 230 VAC, $P_{x\,nom}$	10			ms
T_{Vsb_hold}	Vsb Hold-up Time	V_{SB}, full load	100			ms

Table 1. Input Specification

[1] The Front-End is provided with a minimum hysteresis of 5V during turn-on and turn-off within the ranges

4.1 INPUT FUSE

The PSU has dual pole fusing for the AC input. Time-lag 16A input fuse (5 x 20 mm) in series with the L line and N line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 2.1 µF, resulting in a low and short peak current when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.
NOTE: Do not repeat plug-in/out operations within a short time, or else the internal in-rush current limiting device (PTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage.

4.5 EFFICIENCY

High efficiency (see *Figure 2)* is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

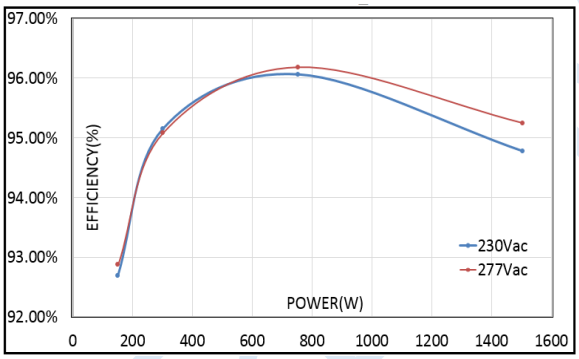


Figure 2. Efficiency vs. Load current (ratio metric loading)

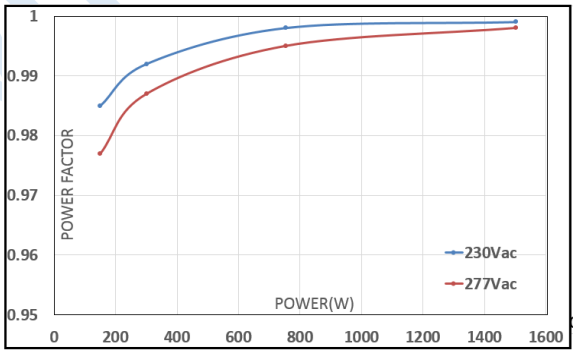


Figure 3. Power factor vs. Load current

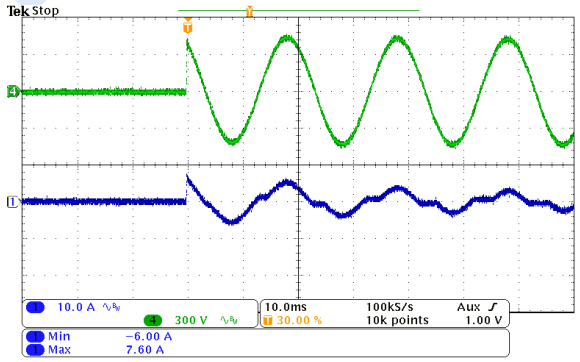


Figure 4. Inrush current, Vin = 305 VAC, 90°, CH1: Iin (10A/div), CH4: Vin (300V/div)

4.6 AC LINE TRANSIENT SPECIFICATION

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage, the power supply shall meet the requirements under the following AC line sag and surge conditions. The peak current shall not exceed 3 times inrush current during ride through time. There shall be 3.5s of normal AC input power between each dropout.

AC Line Sag (3.5 sec interval between each sagging)

Duration	Sag	Operating AC Voltage	Load condition	Performance Criteria*
10s	20%	100 VAC/200 VAC	1* $P_{1\ nom}$	Class A
500ms	30%	100 VAC/200 VAC	1* $P_{1\ nom}$	Class A
200ms	60%	100 VAC/200 VAC	1* $P_{1\ nom}$	Class B
20ms	100%	100 VAC/200 VAC	0.5*$P_{1\ nom}$	Class A
10ms	100%	100 VAC/200 VAC	1* $P_{1\ nom}$	Class A

Table 2. AC Line Sag Transient Performance

Note: 1. Performance criteria Class A is “Normal performance within the specification limits”.
2. Performance criterial Class B is “Temporary degradation or loss of function or with is self-recoverable”.

5. OUTPUT SPECIFICATIONS

General Condition: Ta = 0… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
Main Output V_1							
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C			12		VDC
$V_{1\ set}$	Output Setpoint Accuracy			-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-2		+2	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	305 VAC > V_{in} ≥ 180 VAC, V_1 = 12 VDC 400 VDC > V_{in} ≥180 VDC, V_1 = 12 VDC 180 VAC > V_{in} ≥ 90 VAC, V_1 = 12 VDC			1500 836		W W
$I_{1\ nom}$	Nominal Output Current	264 VAC > V_{in} ≥180 VAC, V_1 = 12 VDC 400 VDC > V_{in} ≥180 VDC, V_1 = 12 VDC 180 VAC > V_{in} ≥ 90 VAC, V_1 = 12 VDC			125 69.5		ADC ADC
$v_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See Section 5.1)				120	mVpp
$dV_{1\ Load}$	Load Regulation	V_i = $V_{i\ nom}$, 0 - 100 % $I_{1\ nom}$			100		mV
$dV_{1\ Line}$	Line Regulation	V_i = $V_{i\ min}$…$V_{i\ max}$			50		mV
$dI_{1\ share}$	Current Sharing Deviation	Deviation from $I_{1\ tot}$ / N, I_1 > 10%		-3		+3	A
dV_{dyn}	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs		-0.6		+0.6	V
T_{rec}	Recovery Time	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom}$			2		ms
$T_{Vout\_on\_delay}$	Start-up Time from AC					3	sec
T_{Vout_rise}	Rise Time	V_1 = 10…90% $V_{1\ nom}$				10	ms
C_{Load}	Capacitive Loading	T_a = 25°C				30000	µF
3.3/5 V_{SB} Standby Output							
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL = 1 VSB_SEL = 0		3.3 5.0		VDC VDC
$V_{SB\ set}$	Output Setpoint Accuracy	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL = 0/1	-0.5		+0.5	% V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-5		+5	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	V_{SB} = 3.3 VDC, V_{SB} = 5.0 VDC,			16.5 16.5		W
$I_{SB\ nom}$	Nominal Output Current	V_{SB} = 3.3 VDC, V_{SB} = 5.0 VDC,			5 3.3		ADC
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$,20 MHz BW (See Section 5.1)	VSB_SEL = 1 VSB_SEL = 0			50 80	mVpp
$I_{SB\ max}$	Current Limitation	VSB_SEL = 1, VSB_SEL = 0,		5.25 3.45		6.2 4.5	ADC
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.5 A/µs, recovery within 1% of $V_{1\ nom}$		-3		+3	%V_{SBnom}
T_{rec}	Recovery Time					250	us
$T_{Vout\_on\_delay}$	Start-up Time from AC	V_{SB} = 90% $V_{SB\ nom}$				2	sec
T_{Vsb_rise}	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$		10		100	ms
C_{Load}	Capacitive Loading	T_{amb} = 25°C				2000	µF

Table 3. Output Specifications

5.1 OUTPUT VOLTAGE RIPPLE

The test set-up shall be following *Figure 5*

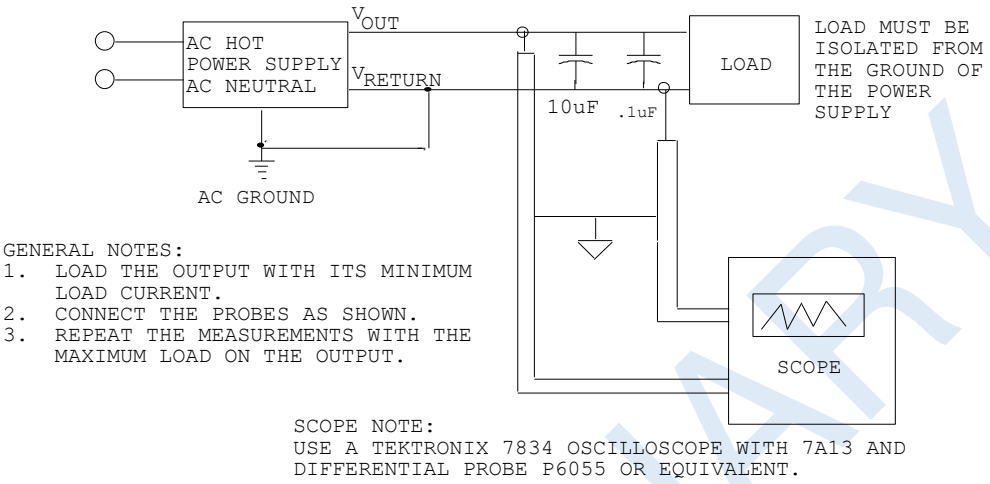


Figure 5. Output ripple test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

The output ripple voltage on standby output (V_{SB}) is influenced by the main output V_1. Evaluating standby output (V_{SB}) output ripple must be done when maximum load is applied to V_1.

6. PROTECTION SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (L)	Not user accessible, Time-lag(F)		16		A
$V_{1\ OV}$	OV Threshold V_1		13.3		14.5	VDC
$V_{SB\ OV}$	OV Threshold V_{SB}		110		120	% V_{SB}
$I_{V1\ lim}$	Over Current Limitation V_1	V_1 > 180 VAC/HVDC, T_a < 50°C V_1 > 90 VAC, T_a < 50°C	128 72		160 90	A
$I_{VSB\ lim}$	Over Current Limitation V_{SB}	T_a < 50°C for 5 V_{SB} T_a < 50°C for 3.3 V_{SB}	3.45 5.25		4.5 6.2	A A
T_{SD}	Over Temperature On Heat Sinks	Automatic shut-down		115	120	°C

Table 4. Protection Specifications

6.1 OVERVOLTAGE PROTECTION

6.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs (V_{SB}) are monitored.

3.3 / 5 V_{SB}

LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage. Output under voltage protection is provided on the standby output (V_{SB}) and main output V_1. When V_{SB} falls below 75% of its nominal voltage, the main output V_1 is inhibited.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn off and latch. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

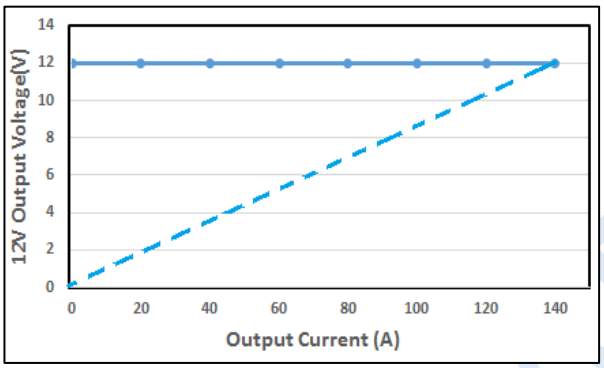


Figure 6. Current Limitation on V_1 (V_i = 230 VAC)

6.3.2 STANDBY OUTPUT

3.3 / 5 V_{SB}

A fault of over current protection on standby output (V_{SB}) will cause the V1 output to turn off and latch. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. The current limitation of the standby output (V_{SB}) is independent of the AC input voltage.

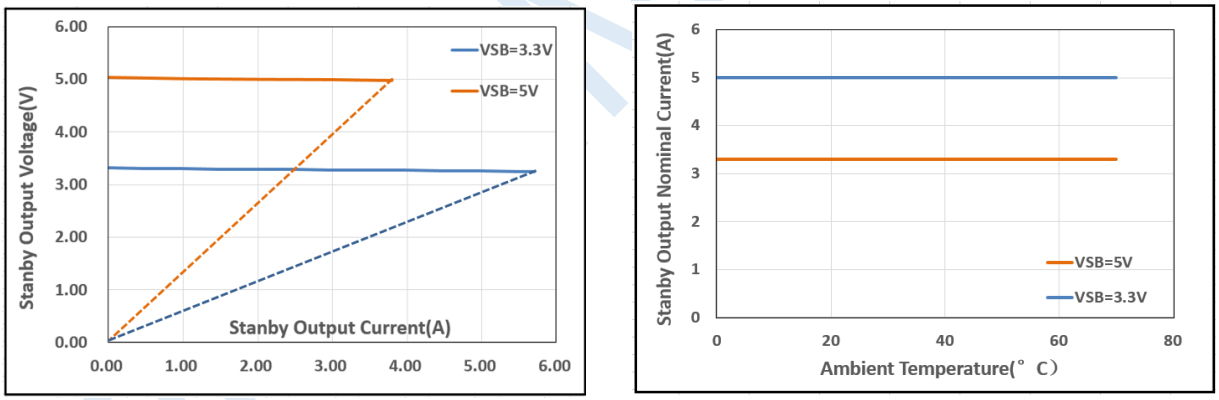


Figure 7. Current Limitation and Temperature Derating on 3.3 / 5 V_{SB}

7. MONITORING

PARAMETER	DESCRIPTION / CONDITION			MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input RMS Voltage	$V_{i\,min} \le V_i \le V_{i\,max}$		-2		+2	%
$I_{i\,mon}$	Input RMS Current	$I_i > 1.5A_{RMS}$		-5		+5	%
$P_{i\,mon}$	True Input Power	$I_i > 1.5A_{RMS}$		-5		+5	%
$V_{1\,mon}$	V_1 Voltage	$I_1 > 20\%\ I_{1\,nom}$		-2		+2	%
$I_{1\,mon}$	V_1 Current	$I_1 > 20\%\ I_{1\,nom}$		-5		+5	%
$P_{o\,nom}$	Total Output Power	$I_1 > 20\%\ I_{1\,nom}$		-5		+5	%
$V_{SB\,mon}$	Standby Voltage		3.3 / 5 V_{SB} Models	-0.2		+0.2	V
$I_{SB\,mon}$	Standby Current	$I_{SB} \le I_{SB\,nom}$	3.3 / 5 V_{SB} Models	-0.5		+0.5	A

Table 5. Monitoring parameters

8. SIGNAL & CONTROL SPECIFICATIONS

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL,\,H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H			10		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
R_{puVSB_SEL}	Internal Pull Up Resistor on VSB_SEL			10		kΩ
$R_{puHOTSTANDBYEN\_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H			10		kΩ
R_{LOW}	Resistance Pin to SGND for Low Level		0		1	kΩ
R_{HIGH}	Resistance Pin to SGND for High Level		50			kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	$I_{sink} < 4$ mA	0		0.4	V
V_{OH}	Output High Level Voltage	$I_{source} < 50$ uA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			10		kΩ
ACOK_H Output						
V_{OL}	Output Low Level Voltage	$I_{sink} < 2$ mA	0		0.4	V
V_{OH}	Output High Level Voltage	$I_{source} < 50$ µA	2.6		3.5	V
R_{puACOK_H}	Internal Pull Up Resistor on ACOK_H			10		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	$I_{source} < 4$ mA	0		0.4	V
I_{OH}	Maximum High Level Leakage Current				10	µA
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ

Table 6. Signal & Control Specifications

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off. If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in (*Figure 8*) except for SMB_ALERT_L, ISHARE and I²C pins. SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

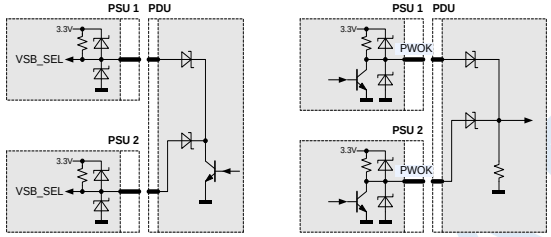


Figure 8. Interconnection of Signal Pins

8.3 FRONT LEDS

There will be 2 separate LED indicators, one blue and one amber to indicate the power supply status. There will be a (slow) blinking blue POWER LED (OK) to indicate that AC is applied to the PSU and the Standby Voltage is available. This same LED shall go steady to indicate that all the Power Outputs are available. This same LED or separate one will blink (slow) or be solid ON amber to indicate that the power supply has failed or reached a warning status and therefore a replacement of the unit is/maybe necessary. The LED are visible on the power supply's exterior face. The LED location meets ESD Requirements.

EVENT	BLUE LED STATUS	AMBER LED STATUS
12V main on and in voltage regulation band (Active mode)	Solid	OFF
12V main off (Standby mode)	1Hz Blinking	OFF
No AC input power to any of the system power supplies	OFF	OFF
No AC input power, but other PSU in the system operating	OFF	1HZ Blinking
Warning event (Output OCW/ OTW/ Fan Fail)	OFF	1HZ Blinking
Fault event (Input OVP/ Output OVP, UVP, OCP/ OTP/ Other internal fault)	OFF	Solid
FW update	OFF	2Hz Blinking

Table 7. LED Definitions

8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

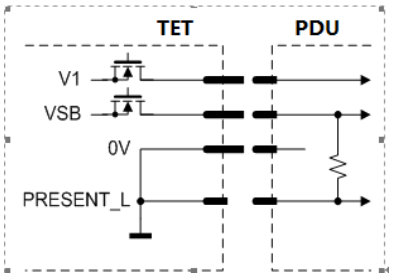


Figure 9. PRESENT_L signal pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 TIMING REQUIREMENTS

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The ACOK_H signal is active-high. The timing diagram is shown in *Figure 10* and referenced in *Table 8.*

OPERATING CONDITION		MIN	MAX	UNIT
TVout_rise	Output voltage rise time for Vout		10	ms
TVsb_rise	Output voltage rise time for Vsb	10	100	ms
TVsb_on_delay	Delay from Vin being applied to Vsb being within regulation		2000	ms
TVout_on_delay	Delay from Vin being applied to Vout being within regulation		3000	ms
Tacok_on	Input voltage to ACOK_H signal delay time		2000	ms
TVout_holdup	Time of Vout output voltage stay within regulation after loss of Vin	10		ms
Tpwok_holdup	Delay from loss of Vin to de-assertion of PWOK	9		ms
Tpson_off_delay	Delay from PSON de-asserted to power supply turning off		5	ms
Tpson_on_delay	Delay from PSON active to output voltages within regulation limits	5	200	ms
Tpson_pwok	Delay from PSON de-active to PWOK being de-asserted		4	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted	100	500	ms
Tpwok_off	Delay from PWOK de-asserted to output voltages dropping out of regulation limits	1		ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using Vin or the PSON signal	100		ms
TVsb_Vout	Delay from Vsb being in regulation to Vout being in regulation at Vin turn on	50	500	ms
TVsb_holdup	Time of Vsb output voltage stays within regulation after loss of Vin	100		ms
Tacok_de-asserted	Delay from Vin drop being 0V to de-aseertion of ACOK		5	ms
Tacok_de-asserted_Vout	ACOK de-asserted to Vout out of regulation	7		ms
Tacok_ de-asserted_Vsb	ACOK de-asserted to Vsb out of regulation	15		ms
Tpskill_off	PSKILL high to Vo1 turn OFF by PSKILL		0.1	ms

Table 8. Timing Requirements

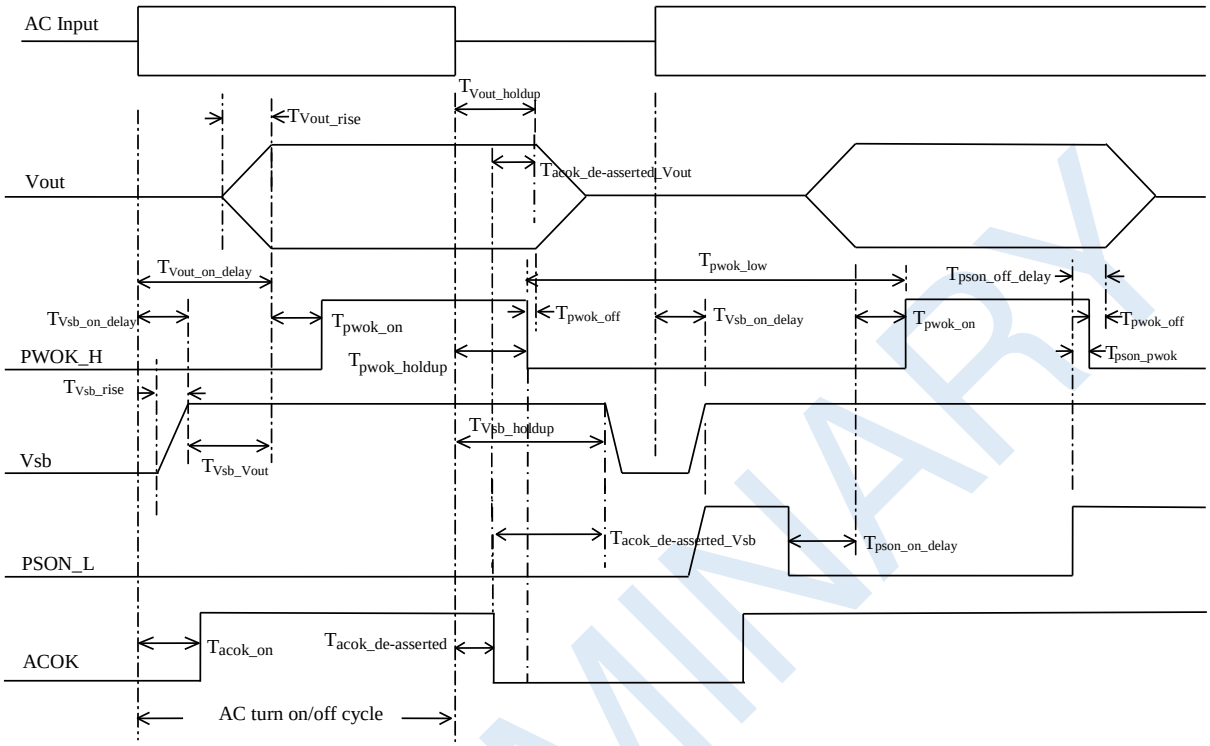


Figure 10. Turn On/Off Timing

8.7 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in *Figure 10* and the parameters in the *Table 8.*

8.8 PWOK_H SIGNAL

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both V_{SB} and V_1 outputs are within regulation. This pin is active-low. The timing diagram is shown in *Figure 10* and referenced in the *Table 8.*

8.9 CURRENT SHARE

The TET front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

8.10 SENSE INPUTS

Both main and standby outputs have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the power GND rail.

With open sense inputs the main output voltage will rise by 230 mV and the standby output by 50 mV. Therefore, if not used, these inputs should be connected to the power output and power GND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its OR-ing device on the output. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN_H pin is high, the load current is low (see *Figure*) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I²C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

Figure 11 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 6 W is achievable.

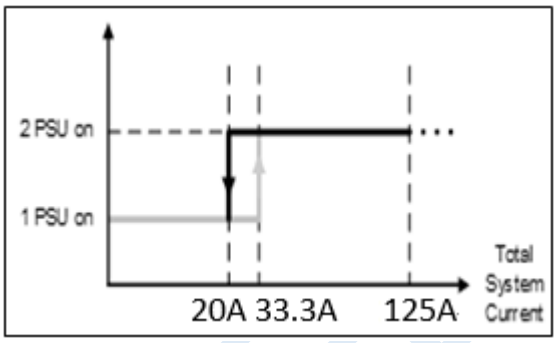


Figure 11. Hot-standby enable/disable current thresholds

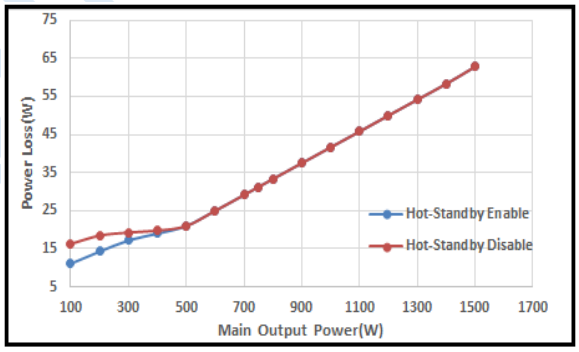


Figure 12. PSU power losses with/without hot-standby mode

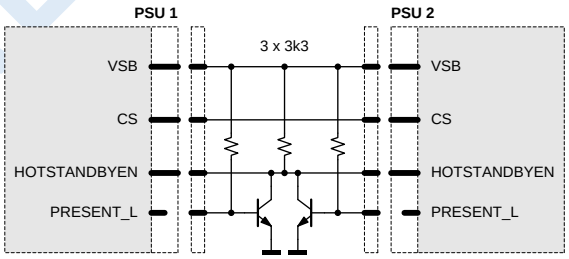


Figure13. Recommended hot-standby configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure13.* If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

8.12 I2C / SMBUS COMMUNICATION

The interface driver in the TET supply is referenced to the V1 Return. The TET supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in *Table 6* and further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

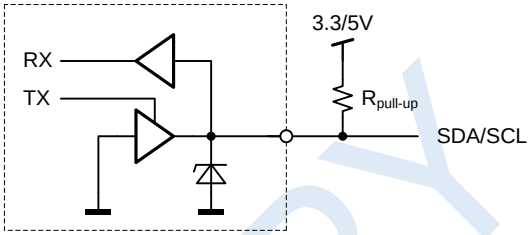


Figure14. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V
t_r	Rise time for SDA and SCL(ViLmax-0.15V to ViHmin+0.15V)	0.65V to 2.25V $f_{SCL} \leq$ 100 kHz	20+0.1Cb[2]		1000	ns
t_{of}	Output fall time (ViHmin+0.15V to ViLmax-0.15V)	2.25V to 0.65V $f_{SCL} \leq$ 100 kHz	20+0.1Cb[3]		300	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10		10	µA
C_i	Internal Capacitance for each SCL/SDA				50	pF
f_{SCL}	SCL clock frequency		0		100	kHz
R_{pu}	External pull-up resistor	$f_{SCL} \leq$ 100 kHz			1000 ns/ Cb	Ω
t_{HDSTA}	Hold time (repeated) START	$f_{SCL} \leq$ 100 kHz	4.0			µs
t_{LOW}	Low period of the SCL clock	$f_{SCL} \leq$ 100 kHz	4.7			µs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \leq$ 100 kHz	4.0			µs
t_{SUSTA}	Setup time for a repeated START	$f_{SCL} \leq$ 100 kHz	4.7			µs
t_{HDDAT}	Data hold time	$f_{SCL} \leq$ 100 kHz	0		3.45	µs
t_{SUDAT}	Data setup time	$f_{SCL} \leq$ 100 kHz	250			ns
t_{SUSTO}	Setup time for STOP condition	$f_{SCL} \leq$ 100 kHz	4.0			µs
t_{BUF}	Bus free time between STOP and START	$f_{SCL} \leq$ 100 kHz	5			ms

Table 9. I2C / SMBus Specification

[2] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

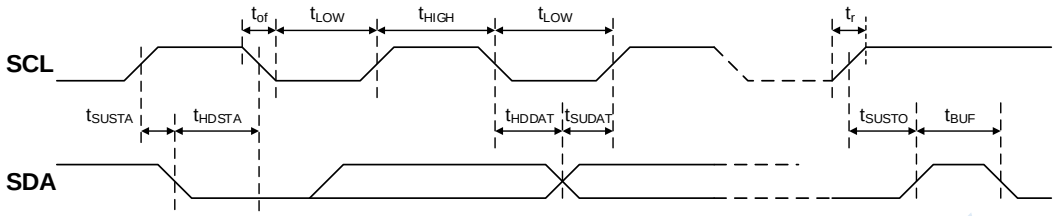


Figure15. I2C / SMBus Timing

8.13 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTE:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

R_{APS} (Ω)[3]	Protocol	I2C Address [4]	
		Controller	EEPROM
820	Power Management Bus	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6

Table 10. I2C / SMBus Specifications

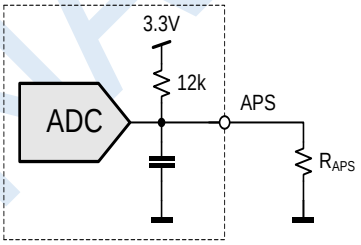


Figure16. I2C address and protocol setting

8.14 CONTROLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure17*). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

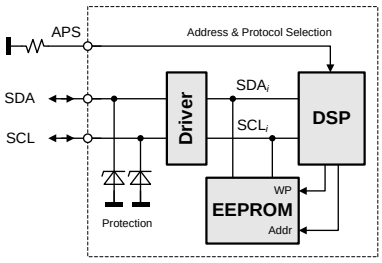


Figure17. I2C Bus to DPS and EEPROM

4 E12 resistor values, use max 5% resistors

5 The LSB of the address byte is the R/W bit

8.15 EEPROM PROTOCOL

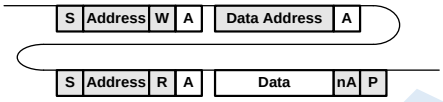
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.16 POWER MANAGEMENT BUS PROTOCOL

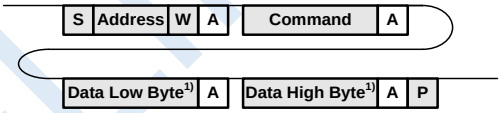
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The TET1500 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

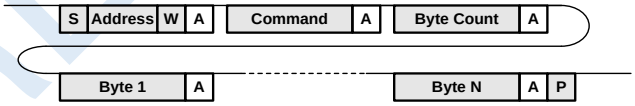
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



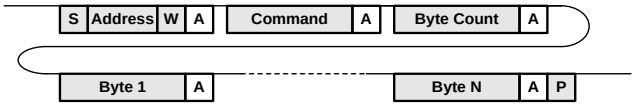
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.

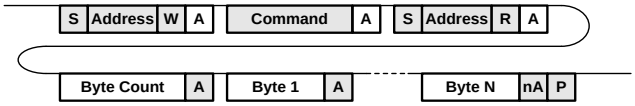


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes.



8.17 POWER SUPPLY DIAGNOSTIC Black box

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus interface with an external source providing power to the
12V main output bus or standby by 5VSB output bus.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.00XXX_TET1500-12-054NA Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

8.18 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus interface while it is in standby mode. This
FW can be updated when in the system and in standby mode and outside the system with power applied to the 12V main output bus or standby by 5VSB output bus.
BPS standard GUI supports the firmware upgrade function.

8.19 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the TET1500-12-054NA Front-End.
The utility can be downloaded on: belfuse.com/power-solutions and supports Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G1Q01.0 Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

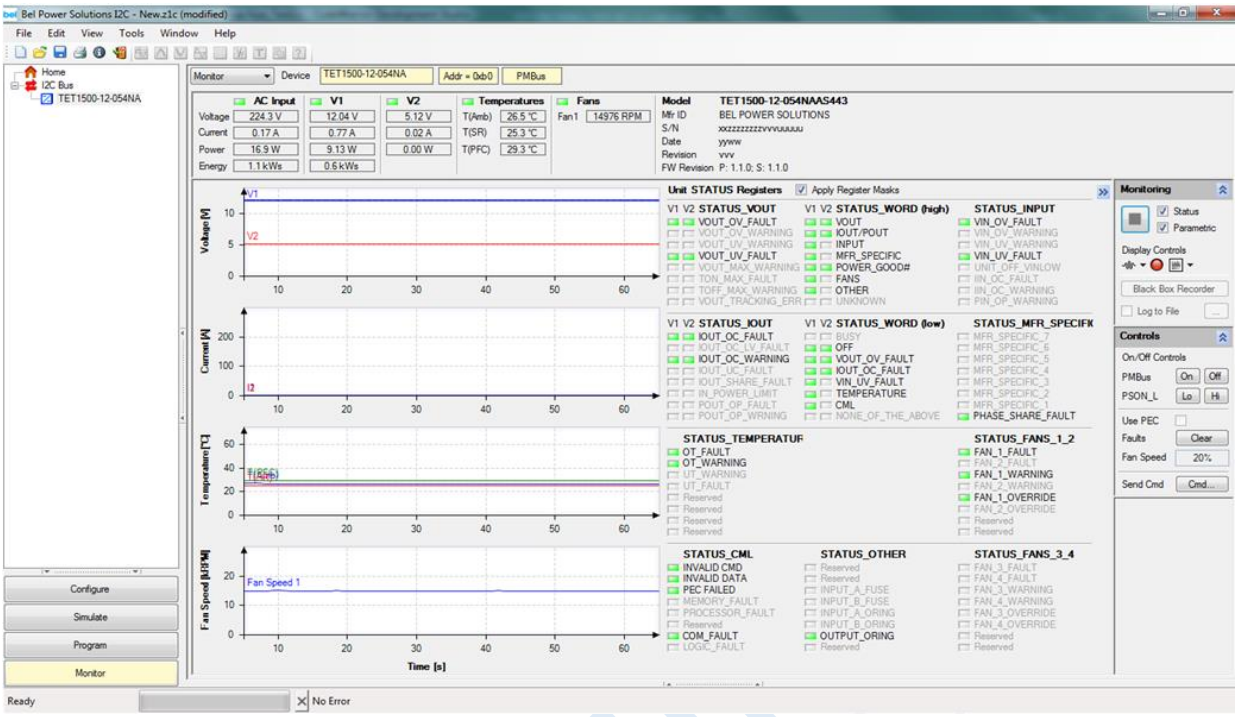


*Figure18. Monitoring dialog of the I2C Utility (for **reference)***

9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The TET1500-12-054NA is provided with normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 120°C. If 70°C mating connector is used then end user must derated the input power to meet a maximum 70°C temperature at the front.

NOTE: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

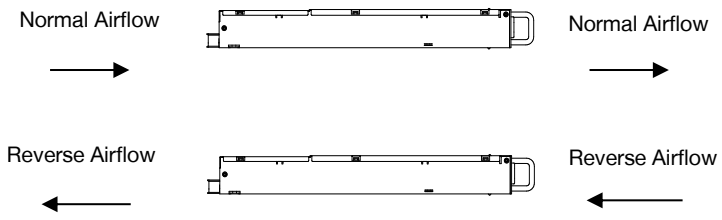


*Figure **19**. Airflow direction*

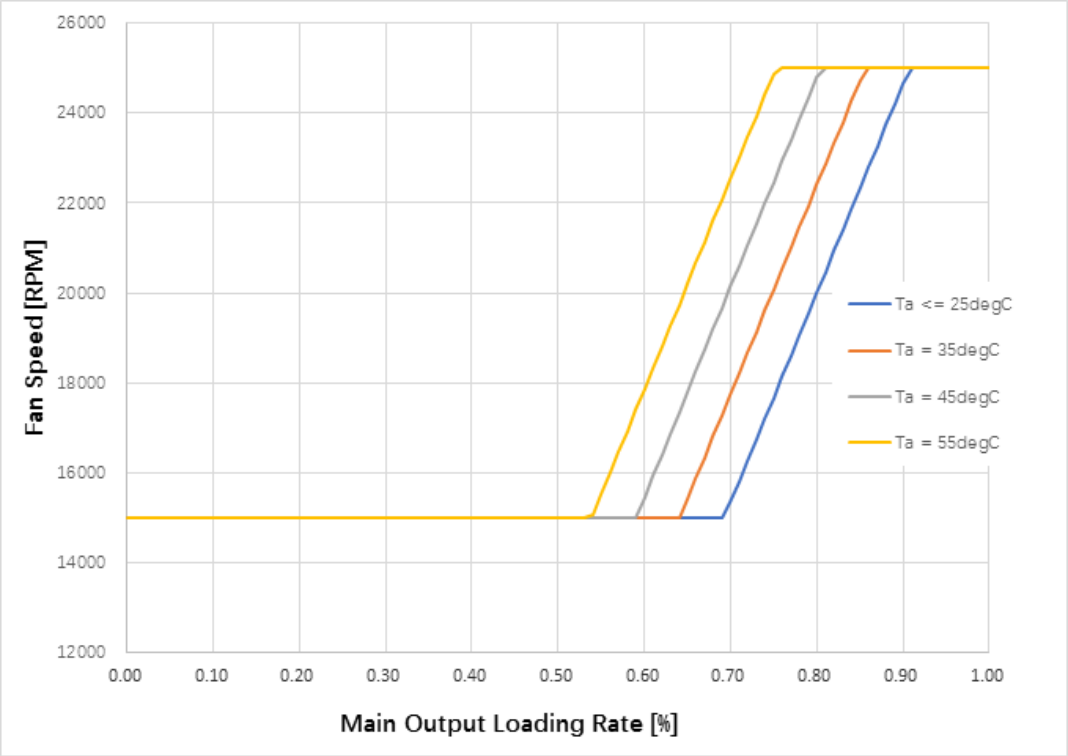


Figure 20. Fan speed VS main output load

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz…2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: ±2 kV,2ohm Line to line: ±2 kV,2ohm	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 10 ms 2: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration 20 ms 3: Vi 230 V, 100% Load, Phase 0 °, Dip 100%, Duration >20 ms	A V_{SB}: A, V_1: B B

Table 11. Immunity

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, single unit	Class A
	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, 2 units in rack system	Class A
Radiated Emission	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, single unit	Class A
	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, 2 units in rack system	Class A
Harmonic Emissions	IEC61000-3-2, Vin = 115 VAC / 60 Hz, & Vin = 230VAC/ 50 Hz, from 10% load to full load	Class A
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 60 Hz, 100% Load	Pass

Table 12. Emission

11. SAFETY APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Agency Approvals	UL60950-1/CSA 60950-1 (USA / Canada) EN60950-1 (Europe) IEC60950-1 (International) CB Certificate & Report, IEC60950-1 (report to include all country national deviations) CE - Low Voltage Directive 2014/35/EC (Europe) GB4943.1- CNCA Certification (China) CNS14336-1 Taiwan BSMI safety regulation		Pending		
	Isolation Strength	Input (L/N) to case (PE) Input (L/N) to output Output to case (PE)		Basic Reinforced Functional		
d_C	Creepage / Clearance	Primary (L/N) to protective earth (PE) Primary to secondary		According to safety standard		mm
	Electrical Strength Test	Input to case Input to output Output and Signals to case		According to safety standard		kVAC

Table 13. Safety Approvals

12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{I\,min}$ to $V_{I\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$ below 3000m Altitude	-5		+50	°C
T_{Aext}	Extended Temp. Range	Derating output power	+51		+61	°C
T_S	Storage Temperature	Non-operational	-40		+85	°C
	Altitude	Operational, above Sea Level, refer derating to Ta	3000			meters
N_a	Audible Noise	$V_{I\,nom}$, 50% $I_{o\,nom}$, T_A = 30°C		55		dBA
Humidity	Operating	*Operating humidity noncondensing*	5		90	%
	Storage	*Storage humidity noncondensing*	5		95	%

Table 14. Environmental Specifications

12.1 COOLING

The power supply shall include fans self-cooling. The fans shall use an acceptable anti-vibration mounting technique. The estimates system back pressure is 0.7 in-H_2O (180 Pa backpressure).

12.2 OPERATIONAL SHOCK/ VIBRATION

Random Vibration – Operating
IPC 9592 Requirements for Power Conversion Devices for the Computer and Telecommunications Industries – Section 5.2.9

Random Vibration – Non-operating
IPC 9592 Requirements for Power Conversion Devices for the Computer and Telecommunications Industries – Section 5.2.10

Shock – Operating
IPC 9592 Requirements for Power Conversion Devices for the Computer and Telecommunications Industries – Section 5.2.11.

13. RELIABILITY

PARAMETER	NOTES	MIN	NOM	MAX	UNIT
Demonstrated MTBF @ 25 °C	1	300			K hours
Demonstrated MTBF @ 41 °C	1	140			K hours
Predicted MTBF (Telcordia)	2	300			K hours
Fan L10 Life@ 40 °C		70			K hours
Electrolytic Capacitor Calculated Life	3	10			Years
Field MTBF		1			M hours

Table 15. Reliability

1. At 25C and 41C ambient and 90% Confidence Level
2. At 40C and 50% part count (method 1 case 1)
3. To calculate electrolytic capacitor life, use capacitor supplier's equation with 40°C ambient and 80% load.
4. Component De-rating follow IPC9592B.

14. MECHANICAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		54.5		mm
		Height		40.0		
		Depth		321.5		
M	Weight			1.13		kg

Table 16. Mechanical Specifications

NOTE: A 3D step file of the power supply casing is available on request.

TET1500-12-054NA/RA: C14 type Input AC connector RongFeng SS-120-1.0B-2.8BV or equivalent

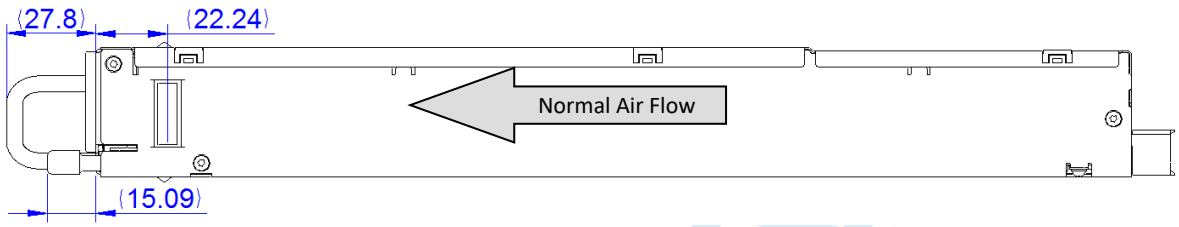


Figure 21. Side View 1

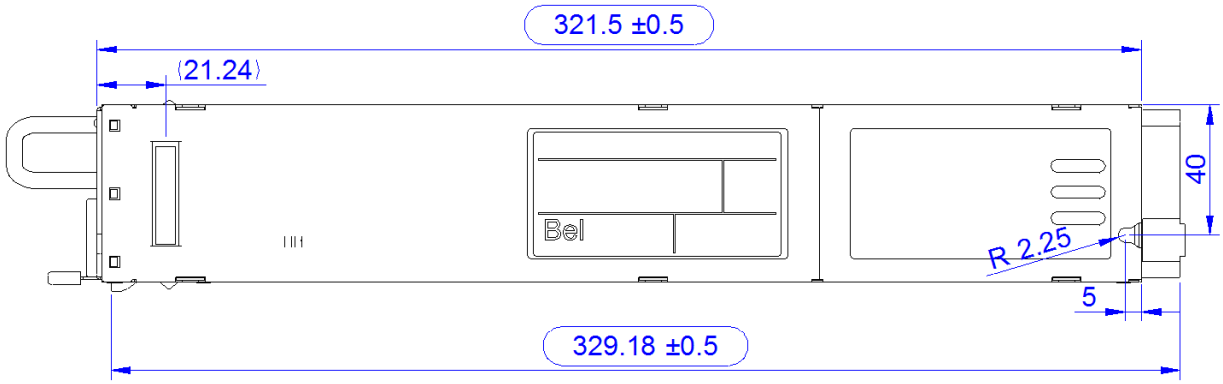


Figure 22. Top View

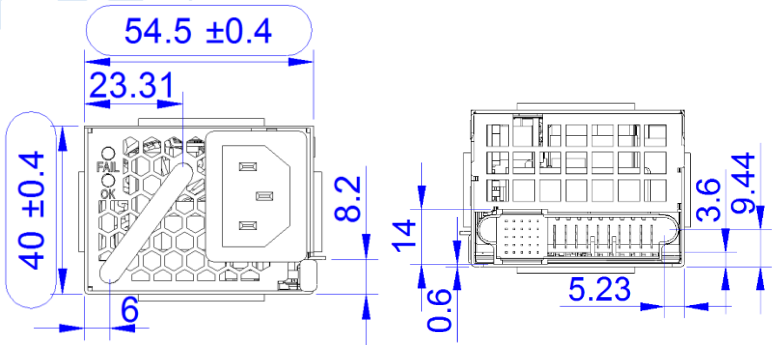


Figure 23. Front and Rear View

TET1500-12-054NAC/RAC: C16 Type Input AC connector, RongFeng SS-120B-1.0-4.0Ad or equivalent

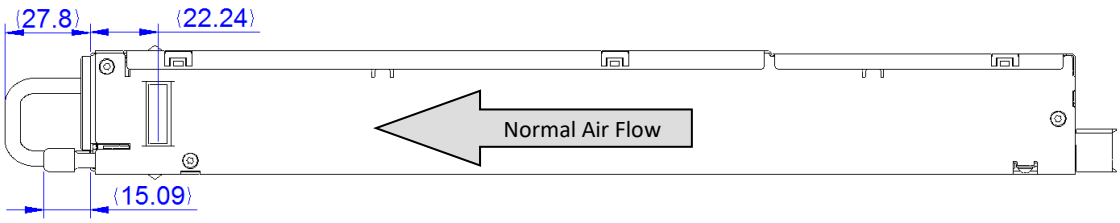


Figure 24. Side View 1

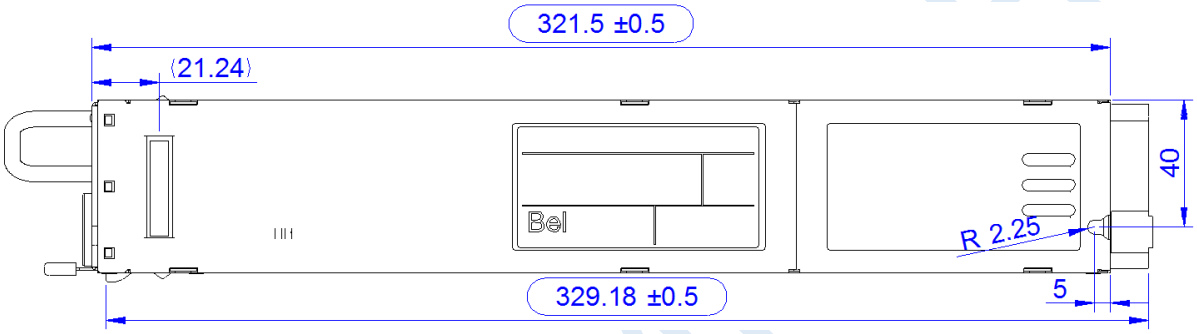


Figure 25. Top View

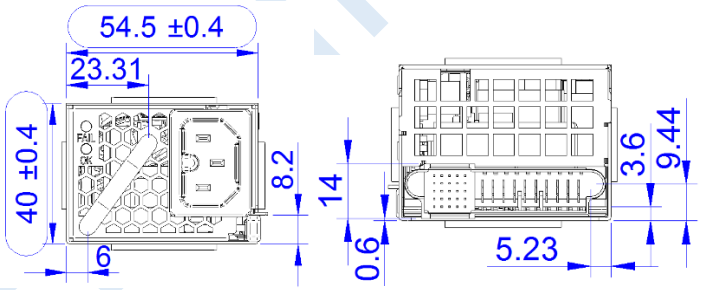


Figure 26. Front and Rear View

TET1500-12-054NAH/RAH: ANDERSON POWER PRODUCTS 2006G1-BK

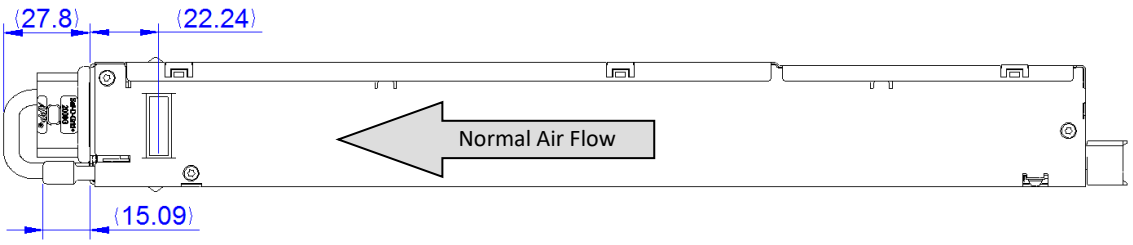


Figure 27. Side View 1

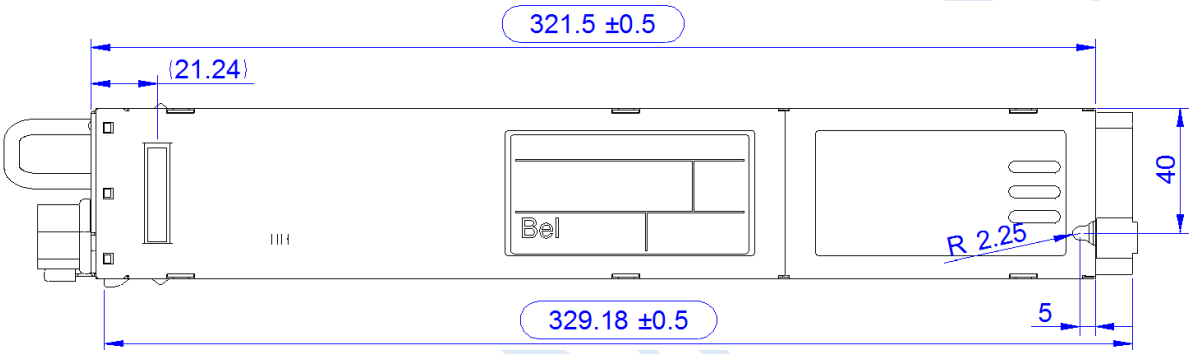


Figure 28. Top View

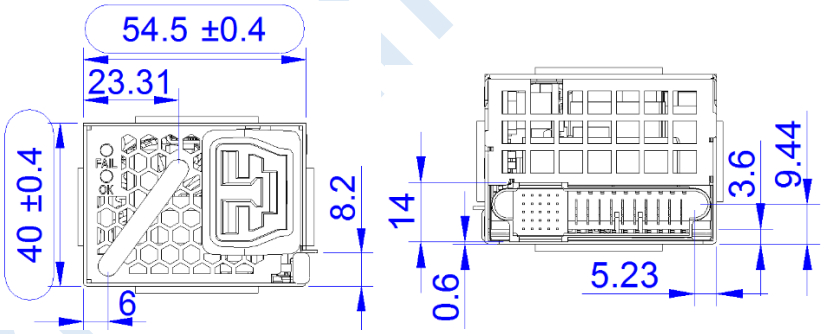


Figure 29. Front and Rear View

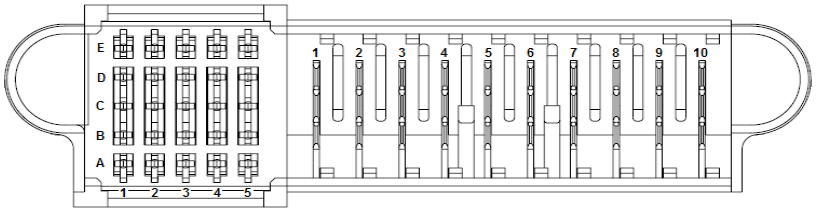
15. CONNECTIONS

AC INPUT CONNECTOR:

TET1500-12-054NAH/RAH: Power supplier connector: ANDERSON POWER PRODUCTS 2006G1-BK
Mating connector: Anderson Saf-D-Grid Power cord 2034KZ2 or equivalent, http://www.andersonpower.com/

TET1500-12-054NA/RA: Power supplier connector: IEC320 C14 type
TET1500-12-054NAC/RAC: Power supplier connector: IEC320 C16 type

DC OUTPUT CONNECTOR:



Power Supply Connector: Tyco Electronics P/N 2-1926736-3 (NOTE: Column 5 is recessed (short pins))
Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

PIN	NAME	DESCRIPTION
Output		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
Control Pins		
A1	VSB	Standby positive output (+3.3/5 V_{SB})
B1	VSB	Standby positive output (+3.3/5 V_{SB})
C1	VSB	Standby positive output (+3.3/5 V_{SB})
D1	VSB	Standby positive output (+3.3/5 V_{SB})
E1	VSB	Standby positive output (+3.3/5 V_{SB})
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I^2C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I^2C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I^2C clock signal line
B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	N/C	Reserved
E4	ACOK_H	AC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin)
E5	PRESENT_L	Power supply present (lagging pin): active-low

Table 17. Connector Pins Configurations

16. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**Bel Power Solutions I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor TET Front-Ends (and other I²C units)	N/A	belfuse.com/power-solutions
	**Dual Connector Board** Connector board to operate 2 TET units in parallel. Includes an on-board USB to I²C converter (use *Bel Power Solutions I²C Utility* as desktop software).	YTM.G1Q01.0	belfuse.com/power-solutions

17. REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2018/11/05	001	/	First release	Jemrry Zhang	BaoJun Zeng
2019/09/17	002	1.0	Description of adding AH in model name	Rick Luo	BaoJun Zeng
2019/09/17	002	5.0	Remove droop voltage spec for Vsb	Rick Luo	BaoJun Zeng
2019/09/17	002	7.0	Change Iin & Pin monitoring condition to I_i>2A from I_1>20%I_{1NOM}	Rick Luo	BaoJun Zeng
2019/09/17	002	8.19	Add TBD on figure 18	Rick Luo	BaoJun Zeng
2020/03/24	003	8.19	Update figure 18	Rick Luo	BaoJun Zeng
2020/03/30	003	14&15	14: Add NA(C) and RA(C); 15: Add models and connectors	Ryan Li	Andrew Li

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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