LTC2325/LTC2324/LTC2320 Quad/Octal 16-Bit/14-Bit/12-Bit, 5Msps/2Msps/1.5Msps, Serial, High Speed SAR ADCs

DESCRIPTION

Demonstration circuit 2395A features the LTC®2325/LTC2324/LTC2320 family. With up to 5Msps, these differential, multiple channel, 16-bit, serial, high speed successive approximation register (SAR) ADCs are available in a 52-lead QFN package. Each ADC has an internal 20ppm/°C maximum drift reference and an SPI-compatible serial interface that supports CMOS and LVDS logic. Note the demo board is configured for CMOS operation by default; see the note under JP8 for LVDS operation. The following text refers to the LTC2325, but applies to all members of the family, the only difference being the number of channels, the sample rate and/or the number of bits. The DC2395A demonstrates the DC and AC performance of the LTC2325 in conjunction with the DC890 PScope™ data collection board. Alternatively, by connecting the DC2395A into a customer application, the performance of the LTC2325 can be evaluated directly in that circuit.

Design files for this circuit board are available at http://www.linear.com/demo/DC2395A

ASSEMBLY OPTIONS

Table 1. DC2395A Assembly Options

VERSION	U1 PART NUMBER	MAX CONVERSION RATE	# OF BITS	MAX CLOCK FREQUENCY
DC2395A-A	LTC2320CUKG-16#PBF	1.5Msps	16	52.5MHz
DC2395A-B	LTC2324CUKG-16#PBF	2Msps	16	110MHz
DC2395A-C	LTC2325CUKG-16#PBF	5Msps	16	110MHz
DC2395A-D	LTC2320CUKG-14#PBF	1.5Msps	14	52.5MHz
DC2395A-E	LTC2324CUKG-14#PBF	2Msps	14	110MHz
DC2395A-F	LTC2325CUKG-14#PBF	5Msps	14	110MHz
DC2395A-G	LTC2320CUKG-12#PBF	1.5Msps	12	52.5MHz
DC2395A-H	LTC2324CUKG-12#PBF	2Msps	12	110MHz
DC2395A-I	LTC2325CUKG-12#PBF	5Msps	12	110MHz

BOARD PHOTO

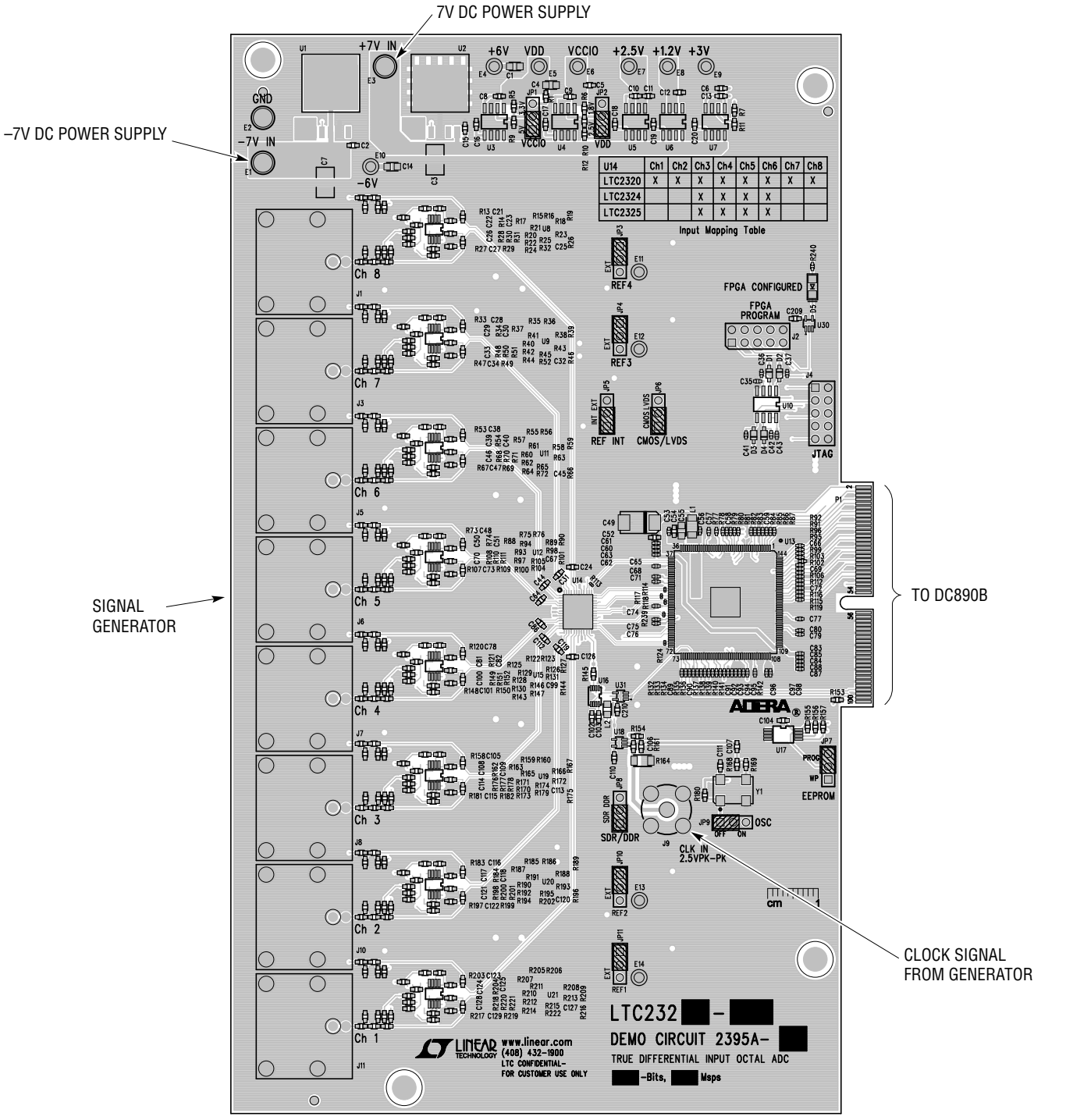

Figure 1. DC2395A Connection Diagram

QUICK START PROCEDURE

Demonstration circuit 2395A is easy to set up and evaluate for performance. Refer to Figure 1 and follow the procedure below.

- Connect the DC2395A to a DC890 USB high speed data collection board using edge connector P1.
- Connect the DC890 to a host PC with a standard USB A/B cable.
- Apply a low jitter signal source to J11 to test channel 1. Note that the DC2395A is capable of accepting a differential input signal as well as a single-ended signal. See the Hardware Setup section for the jumper positions that correspond to these configurations.
- As a clock source, apply a low jitter 10dBm sine wave or square wave to connector J9. See Table 1 for maximum clock frequencies. Note that J9 has a 50Ω termination resistor to ground.
- Run the PScope software (Pscope.exe version K73, or later) supplied with the DC890 or download it from www.linear.com/software. Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically, as new features may be added. The PScope software should recognize the DC2395A and configure itself automatically.
- Click the Collect button (Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be used to stop data acquisition.

DRIVE OPTIONS

There are several ways to drive the LTC2325 on the DC2395A. It can be driven with a true differential source, or a single-ended source in either pseudo-differential bipolar or unipolar mode. For details on how to configure the DC2395A for any of these see Table 2.

An example input circuit for channel 1 is shown in Figure 3.

Table 2. Resistor Values for Different Input Configurations

INPUT CONFIGURATION	R32, 52, 72, 104, 146, 179, 202, 222	R17, 37, 57, 88, 125, 163, 187, 207	R15, 35, 55, 75, 122, 159, 185, 205	R16, 36, 56, 76, 123, 160, 186, 206	R24, 44, 64, 100, 143, 173, 194, 214
Differential	0Ω	DNI	DNI	0Ω	DNI
Single-Ended Differential ADC Drive	0Ω	DNI	301Ω	301Ω	DNI
Single-Ended Bipolar ADC Drive	0Ω	DNI	DNI	0Ω	0Ω
Unipolar ADC Drive	DNI	0Ω	301Ω	301Ω	0Ω

*DNI = Do not install

QUICK START PROCEDURE

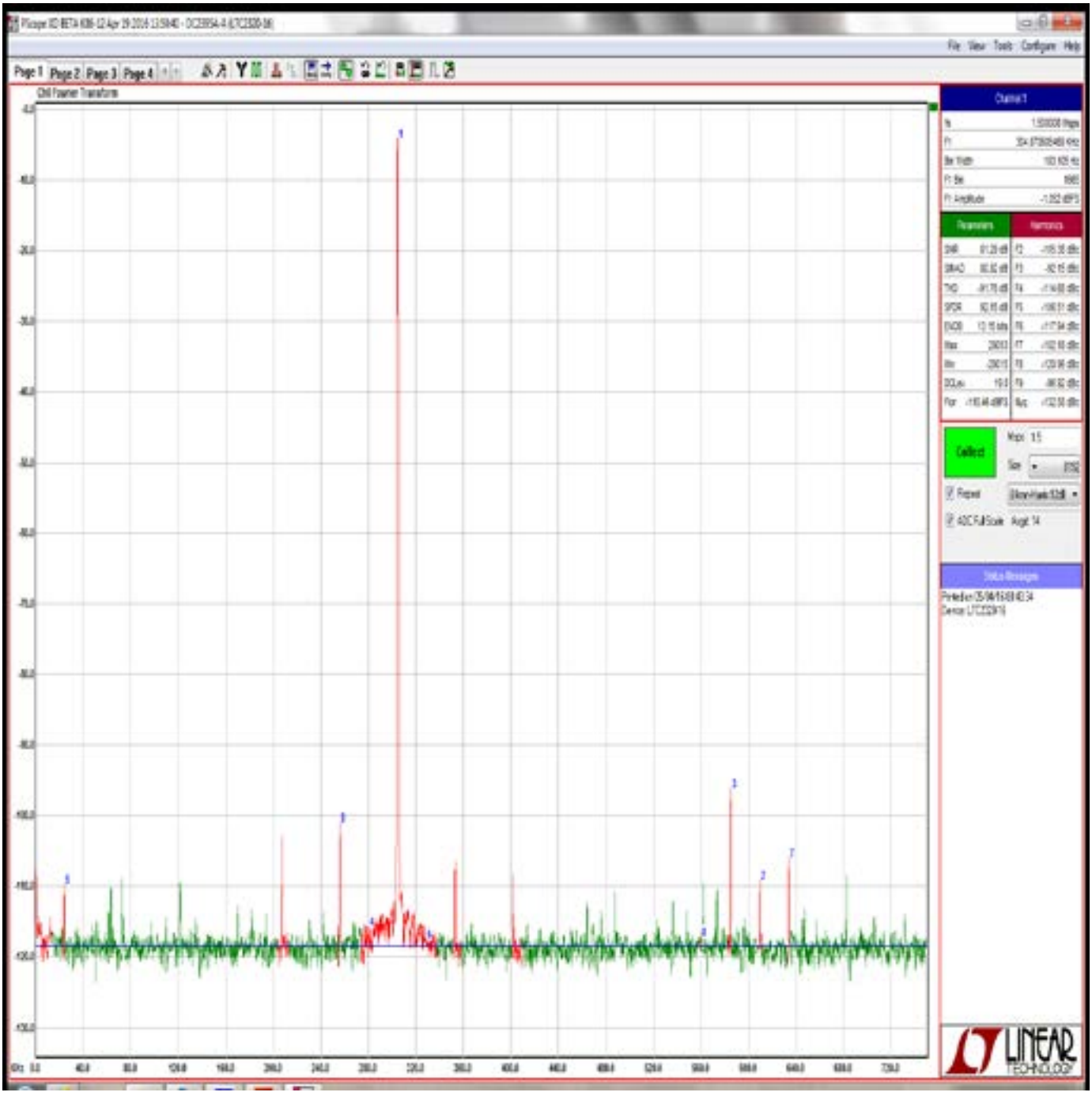

Figure 2. DC2395A PScope Screenshot

QUICK START PROCEDURE

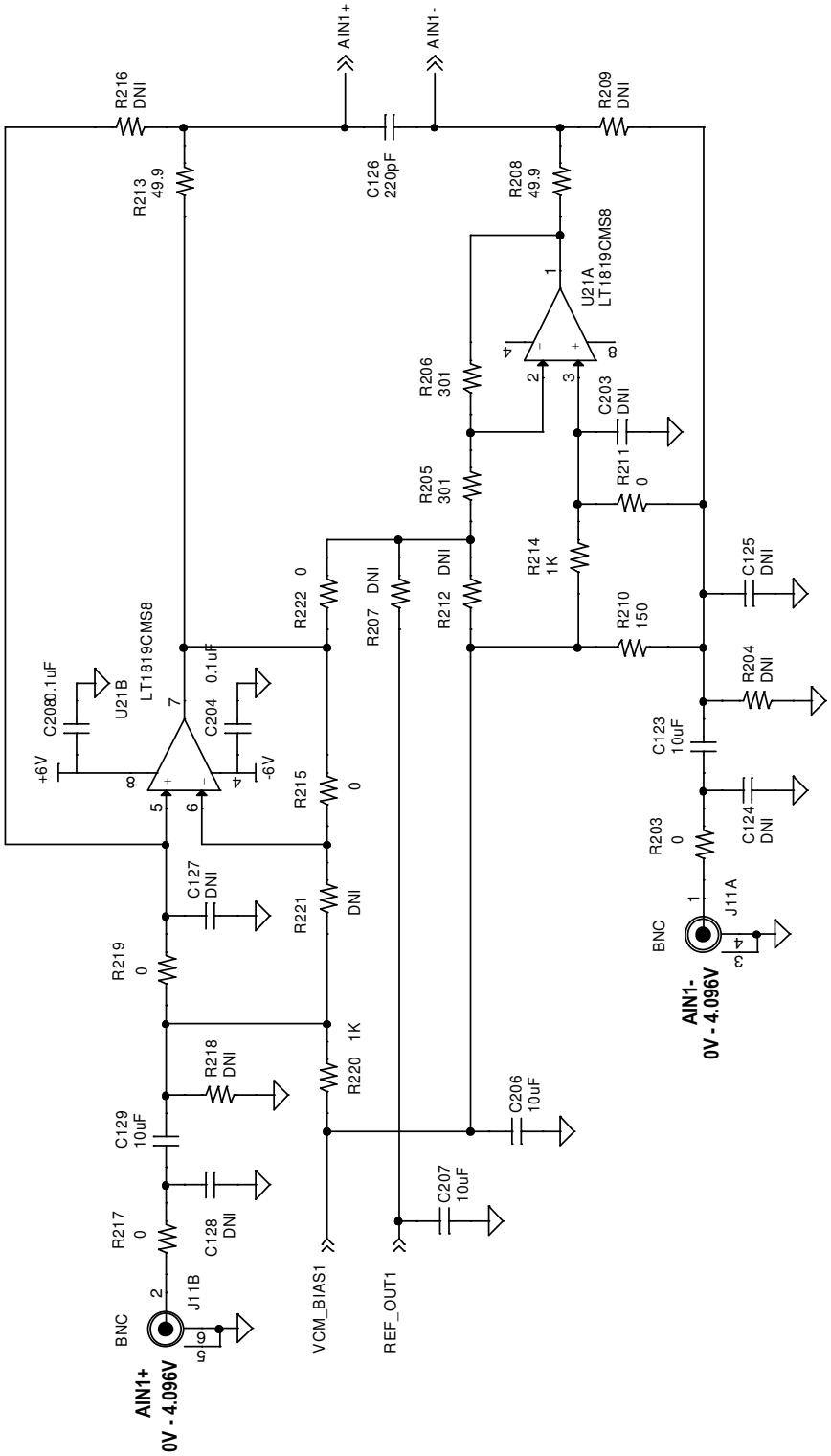

Figure 3. Example Input Circuit, Single-Ended Differential ADC Drive

HARDWARE SETUP

SIGNAL CONNECTIONS

J2 FPGA Program: Factory use only.

J4 JTAG: Factory use only.

J11 Ch1 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch1$^+$ input, and the lower BNC as the Ch1$^-$ input.

J10 Ch2 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch2$^+$ input, and the lower BNC as the Ch2$^-$ input.

J8 Ch3 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch3$^+$ input, and the lower BNC as the Ch3$^-$ input.

J7 Ch4 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch4$^+$ input, and the lower BNC as the Ch4$^-$ input.

J6 Ch5 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch5$^+$ input, and the lower BNC as the Ch5$^-$ input.

J5 Ch6 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch6$^+$ input, and the lower BNC as the Ch6$^-$ input.

J3 Ch7 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch7$^+$ input, and the lower BNC as the Ch7$^-$ input.

J1 Ch8 Input: In the single-ended configuration, use the upper BNC connector as the signal input. For differential operation, use the upper BNC as the Ch8+ input, and the lower BNC as the Ch8$^-$ input.

J9 CLK: This input has a 50Ω termination resistor, and is intended to be driven by a low jitter 10dBm sine or square wave. To achieve the full AC performance of this part, the clock jitter should be kept under 2ps. This input is capacitively coupled so that the input clock can be either 0V to 2.5V or ±1.25V. This eliminates the need for level shifting. To run at the maximum conversion rate, apply the frequency specified in the Table 1.

JP1 VCCIO: Use this jumper to select the VCCIO supply voltage. The default setting is **2.5V**. The **1.8V** setting selects a 1.8V supply voltage.

JP2 VDD: Use this jumper to select the VDD supply voltage. The default setting is **5V**. The **3.3V** setting selects a 3.3V supply voltage.

JP5 REF INT: Set for INT when using the internal reference. Set for EXT to disable the internal REFOUT1-4 buffers for use with external voltage references.

JP11 REF1: Set for ONB to use onboard voltage reference. Set for EXT to use external reference applied at E14.

JP10 REF2: Set for ONB to use onboard voltage reference. Set for EXT to use external reference applied at E13.

JP4 REF3: Set for ONB to use onboard voltage reference. Set for EXT to use external reference applied at E12.

JP3 REF4: Set for ONB to use onboard voltage reference. Set for EXT to use external reference applied at E11.

HARDWARE SETUP

JP8 SDR/DDR: Set for SDR for single data rate operation. Set for DDR for double data rate operation.

JP6 CMOS/LVDS: Use this jumper to select the data output format from the LTC2325. The default setting is **CMOS**. The output data will not be valid if the jumper is moved to the **LVDS** position unless the following changes have been made:

Install 100Ω S0402 resistors at R113, 114, 117, 118, 124, 239

Reprogram the CPLD through J2 using the programming file LTC2325_lvds.pof found at:

http://www.linear.com/demo/DC2395A

Move JP6 to the **LVDS** position.

JP7 EEPROM: Factory use only.

JP9 OSC: Use this jumper to enable the onboard encode clock source. The default setting is **OFF**. The **ON** setting energizes this source. Refer to the DC2395A schematic for additional passive elements required to use the onboard source.

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