40 W adapter demo board

Using the new 700 V CoolMOS™ P7 and ICE2QS03G quasi-resonant PWM controller

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Scope and purpose

The demo board described in this application note provides a test platform for the new 700 V CoolMOS™ P7 series of high voltage MOSFETs. The adapter uses the ICE2QS03G, a second generation current mode control quasi-resonant flyback controller and an IPA70R600P7S 700 V CoolMOS™ P7 series power MOSFET. This application note is intended for those that have experience with flyback converter designs and will not go in depth regarding the overall design process, but will cover specific design aspects for this controller and 700 V CoolMOS™ P7 in charger and adapter applications. It will also look at the overall benefits that the 700 V CoolMOS™ P7 presents for switch mode power supplies. For a detailed introduction on flyback converter design please read Design guide for QR Flyback converter [1].

Intended audience

Power supply design engineers

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1 Description

This 40 W adapter demo board is intended to be a form, fit, and function test platform for charger and adapter applications to show the operation of the 700 V CoolMOS™ P7 as well as the overall controller design. The demo board is designed around a quasi-resonant flyback topology for improved switching losses that allows higher power density designs and lower radiated and conducted emissions. A 40 W universal input isolated flyback demo board with a 19 V output based on the ICE2QS03G controller and the CoolMOS™ P7 MOSFET is described in this application note and some test results are presented.

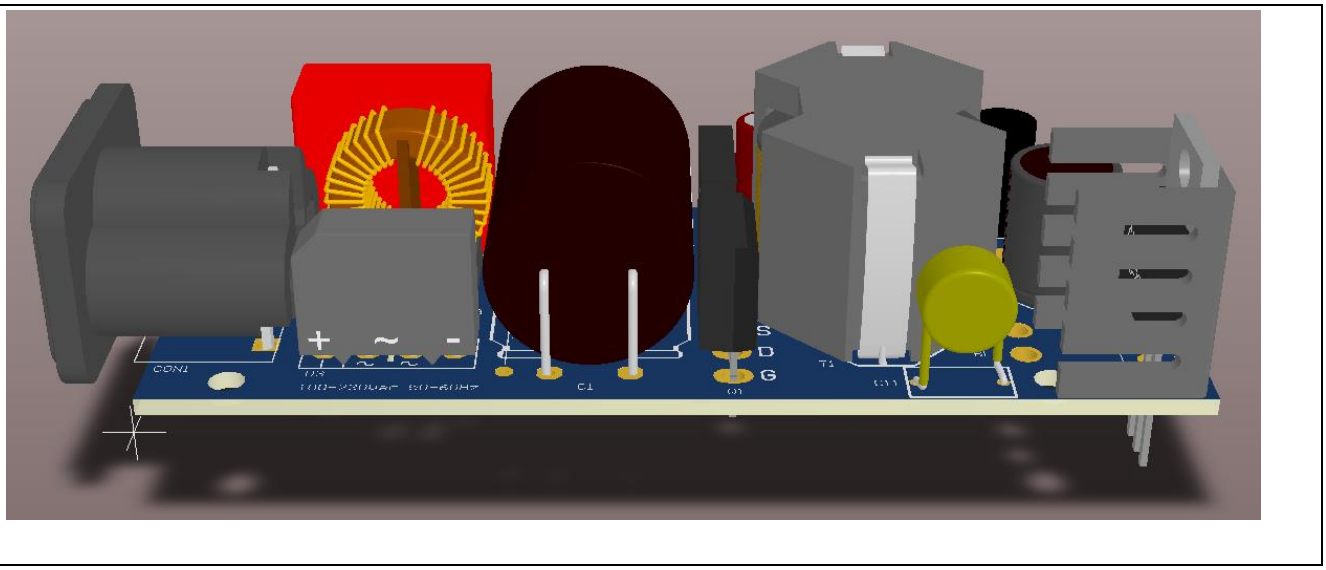

Figure 1 40 W flyback demo board

2 Quasi-resonant flyback overview

The quasi-resonant (QR) flyback offers improved efficiency and electro-magnetic interference (EMI) performance over the traditional fixed frequency flyback converter by reducing switching losses. This is accomplished by controlling the turn-on time of the primary MOSFET (Q_{pri} in Figure 3). In a flyback operating in discontinuous conduction mode (DCM), the energy is first stored in the primary side when the primary MOSFET (Q_{pri}) is turned on allowing the primary current to ramp up. The primary MOSFET (Q_{pri}) turns-off and the energy stored in the transformer transfers into the secondary side capacitor. The energy that is left in the primary inductance (L_{pri}) after transferring the energy to the secondary then resonates with the combined output capacitance of the MOSFET($C_{DS\_parasitic}$) consisting of the MOSFET output capacitance (C_{OSS}), stray drain source capacitance from the transformer and layout, and any additional added external drain source capacitance on this node. In a fixed frequency flyback the switch turn-on happens regardless of the MOSFET drain source voltage (V_{DS}). If switching occurs at a higher V_{DS} (Figure 2), this leads to more switching losses (E_{OSS} losses). The QR flyback waits to turn on Q_{pri} until the V_{DS} voltage reaches the minimum possible voltage shown in Figure 2 and then turns-on the MOSFET.

$$P_{sw\_on} = 0.5 f_{sw} C_{OSS} V_{DS}^2$$

Since the turn-on switching losses are a function of V^2 (as shown above), this reduces the overall system switching losses. This has the added benefit of lowering the amount of switched energy which helps reduce switching noise from the converter, resulting in lower radiated and conducted emissions.

The 700 V CoolMOS™ P7 technology generates improvements in the operation of QR flyback converters through having lower output capacitance (C_{OSS}) that helps to reduce the losses of the device during turn-on. The improvements that 700 V CoolMOS™ P7 offers will be further addressed in Section 4.

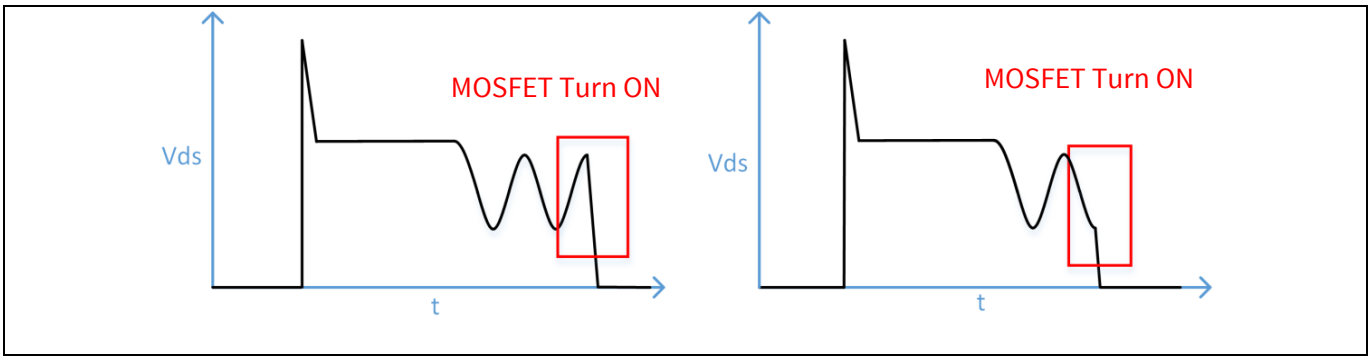

Figure 2 Fixed frequency flyback primary MOSFET drain source waveform (left) vs. a QR flyback primary MOSFET drain source waveform (right).

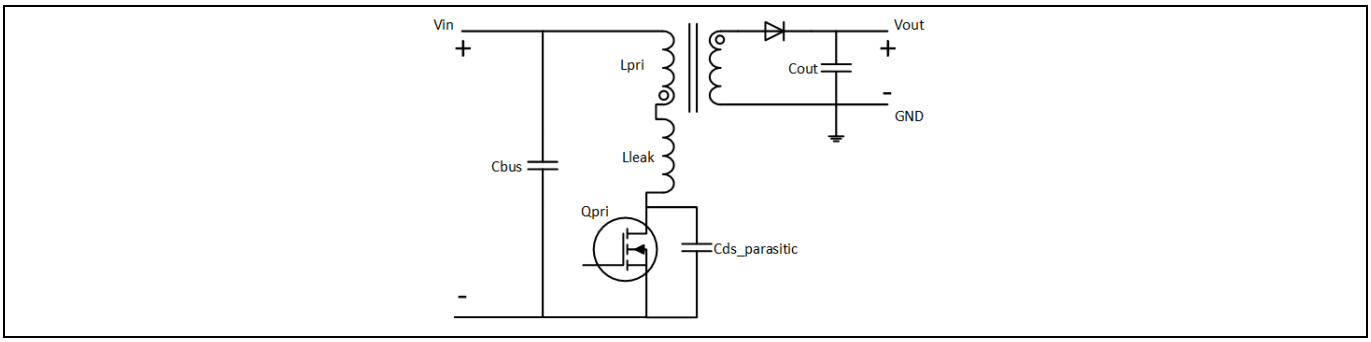

Figure 3 Simplified flyback schematic

3 ICE2QS03G functional overview

The ICE2QS03G PWM controller is a second-generation quasi-resonant flyback controller IC developed by Infineon Technologies. Typical applications include TV-sets, DVD-players, set-top boxes, netbook adapters, home audio, and printer applications. This controller implements switching at the lowest ringing voltage and also includes pulse skipping at light loads for maximum efficiency across a wide range of loads.

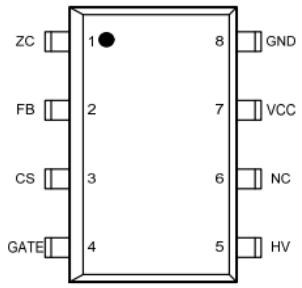

Figure 4 ICE2QS03G pinout

Table 1 ICE2QS03G pin description

Pin	Name	Description
1	Zero Crossing (ZC)	Detects the minimum trough (valley) voltage for turn-on for the primary switch turn-on time
2	Feedback (FB)	Voltage feedback for output regulation
3	Current Sense (CS)	Primary side current sense for short circuit protection and current mode control
4	Gate drive output (GATE)	MOSFET gate driver pin
5	High Voltage (HV)	Connects to the bus voltage for the initial startup through the high voltage startup cell
6	No Connect (NC)	No connection
7	Power supply (VCC)	Positive IC for the power supply
8	Ground (GND)	Controller ground

4 700 V CoolMOS™ P7 benefits for adapters

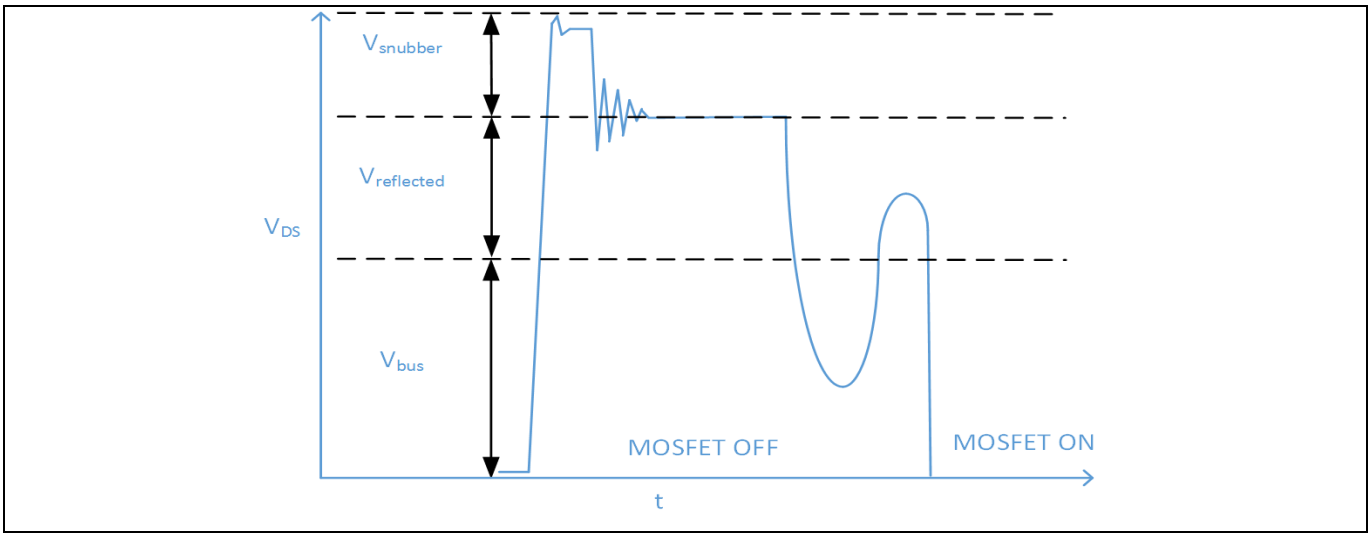

Figure 5 The MOSFET drain source voltage in a flyback converter is the sum of the bus voltage (V_{bus}), reflected voltage ($V_{reflected}$), and snubber voltage ($V_{snubber}$).

The 700 V CoolMOS™ P7 provides several benefits for charger and adapter applications when compared to 600 V and 650 V MOSFETs. The additional breakdown voltage can be used to increase the efficiency of designs, increase the allowable AC input voltage, or increase the surge capabilities of designs. The P7 family of devices also has better performance when comparing switching losses to previous generations of MOSFETs.

A 700 V breakdown voltage allows for a higher combination of bus voltage, reflected voltage, and snubber voltage than can be achieved with 600 V or 650 V devices. This allows for increasing the snubber and reflected voltage in order to lower the switching losses of a converter. It is also possible to use this extra voltage margin to allow for bus voltages extending beyond the typical 265 V_{AC} high line. The device can also be used as a drop in replacement for 600 V and 650 V devices to give additional margin for abnormal conditions such as surge and output short circuit conditions in existing designs that need improved margins. This additional 50 – 100 V of drain source breakdown voltage gives designers more flexibility to improve the overall design.

The P7 family of devices also has an improved switching performance that is better than existing Infineon and competitor devices. One switching loss mechanism is the E_{OSS} of the MOSFET. The E_{OSS} is the main loss contributor for the turn-on of the MOSFET in a QR flyback. The energy that is stored in the output capacitance of the MOSFET needs to be discharged every cycle before the MOSFET is turned on. As shown in Figure 6, the output capacitance energy storage of the 700 V CoolMOS™ P7 is better when compared to equivalent competitor devices. This improvement is most significant at higher AC input voltages.

Additional details about the 700 V CoolMOS™ P7 device improvements such as the reduced gate charge (Q_g), $R_{DS(on)}$ temperature dependency, Q_{OSS}, and transfer characteristics can be found in the CoolMOS™ 700V P7 Application note [3].

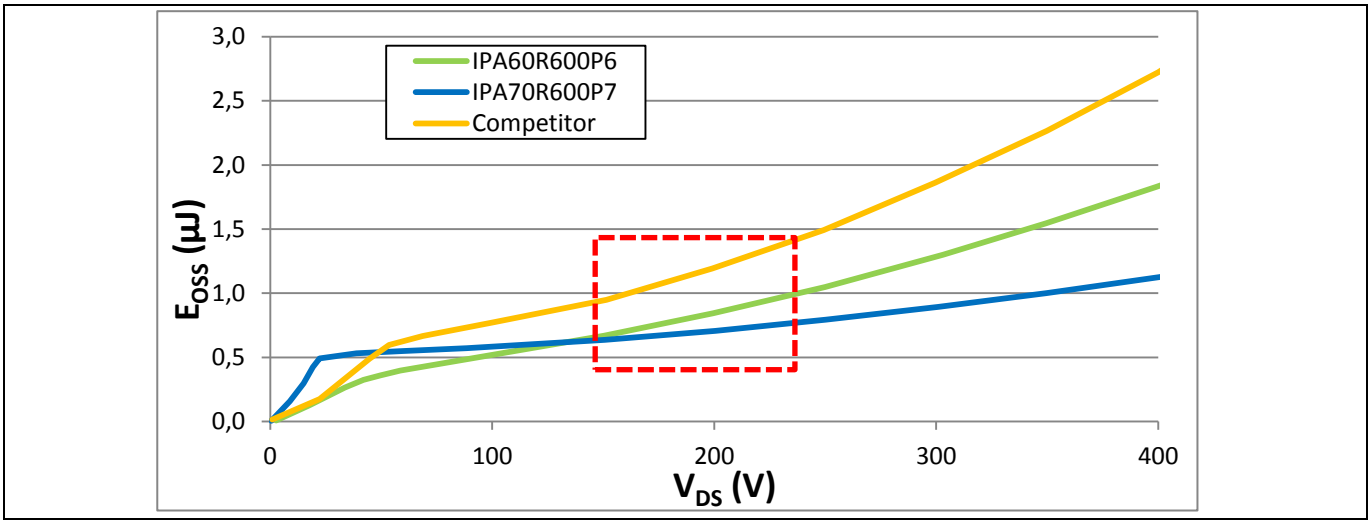

Figure 6 **E_{oss} comparison of a P6 700 V 600 mΩ MOSFET, a P7 700 V 600 mΩ MOSFET, and a competitor's 700 V 600 mΩ device. It can be seen that the amount of energy stored in the output capacitance during a typical QR high line turn on of 200 V is reduced by 0.5 µJ every switching cycle, which in a 100 kHz design corresponds to 50 mW.**

SPICE models of the P7 700 V MOSFETs are provided on the Infineon website. These models have been created with MOSFET characterization data covering different MOSFET parameters and provide a high level of accuracy. Below, Figure 7 shows the difference between the Infineon 40 W adapter's measured waveforms and the simulated waveforms. These models can be used to better understand the loss mechanisms that are responsible for power dissipation in the primary MOSFET of the Flyback converter and help to optimize designs.

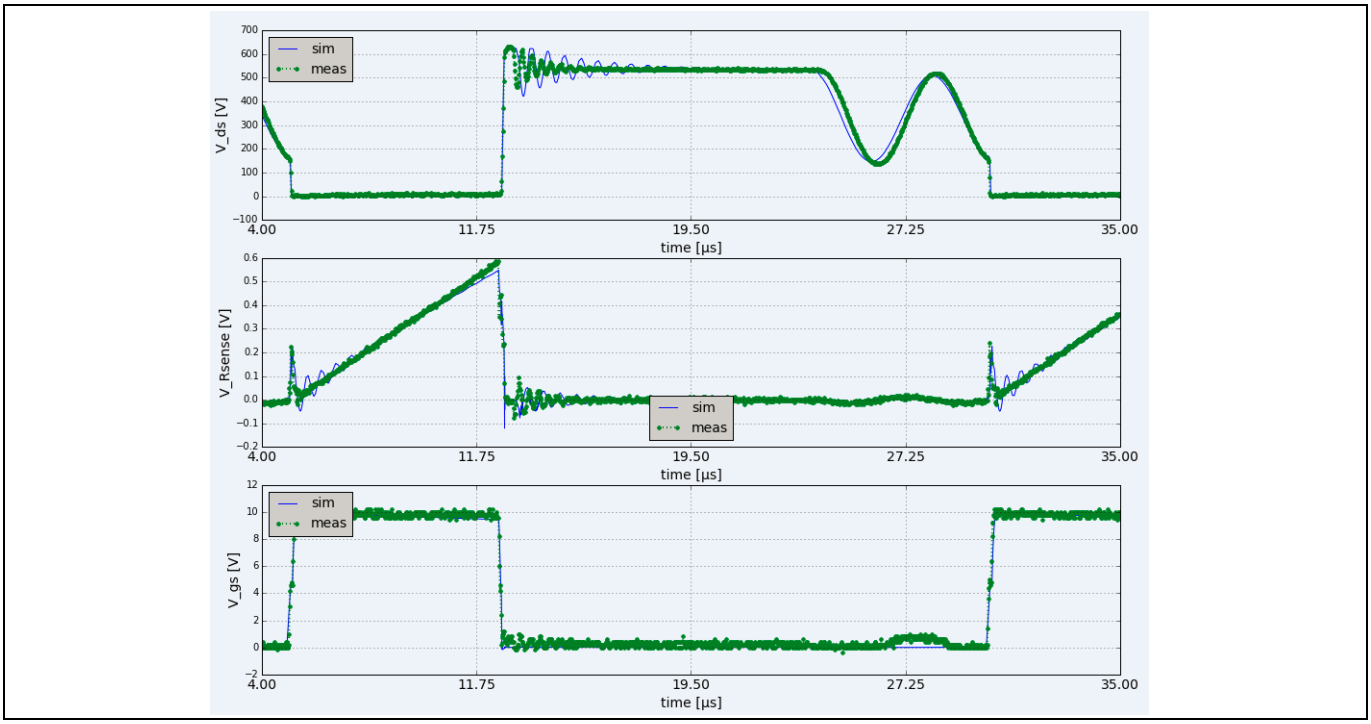

Figure 7 **Simulated switching vs. measured switching at 230 V_{AC} operation in the Infineon 40 W adapter.**

5 Design considerations

5.1 700 V MOSFET and design changes

This section will compare the Infineon 35 W adapter design using an Infineon 600 V C6 MOSFET with the Infineon 700 V CoolMOS™ P7 based 40 W adapter to show the differences between the two designs.

The flyback MOSFET was changed from the CoolMOS™ C6 family of devices to the P7 700 V IPA70R600P7S in order to have the best performance from the latest generation of Infineon devices. With the same $R_{DS(on)}$, the switching characteristics of the MOSFET are improved. In this particular design the peak drain source voltage was increased from 526 V to 560 V by slightly reducing the reflected voltage and increasing the snubber clamp voltage leading to a reduction in snubber energy dissipation. Reducing the switching losses helps to improve the high line and light load efficiency of the 40 W adapter. Even with increasing the drain source voltage, the calculated breakdown voltage margin increased from 12 percent to 20 percent. The output diode was also replaced with a lower cost, lower voltage drop diode in order to reduce the full load power losses.

The reflected voltage was decreased from the Infineon 35 W adaptor in order to reduce the snubber losses. The RCD snubber resistor value was also increased to further reduce the snubber loss, which causes the maximum drain source peak voltage to increase. As shown in Table 2, the turns ratio is reduced by 20 V in order to reduce the reflected voltage, which helps to reduce the energy that is dissipated across the snubber network as shown in the equation below:

$$P_{snubber} = \frac{(V_{snubber}+V_{reflected})^2}{R_{snubber}}$$

Table 2

Parameter	Symbol	600 V design	700 V P7 design
Transformer primary turns	N_P	66 turns	87 turns
Transformer secondary turns	N_S	11 turns	17 turns
Output voltage	V_{output}	19 V	19 V
Transformer reflected voltage	$V_{reflected}$	117 V	97 V

The primary side resistor, capacitor, and diode (RCD) snubber network resistor power dissipation was reduced allowing the snubber voltage to reach a higher level and thus lowering the amount of energy that is dissipated in the snubber resistor. This comes into effect especially at lower power levels where the conduction loss is no longer the dominant source of power losses. The snubber clamping voltage can be calculated using the equation below:

$$V_{snubber} = \frac{1}{2}\left(\sqrt{V_{reflected}^2 + 2\frac{L_{leakage}I_{Pri}^2 R_{snubber}}{T_S}} - V_{reflected}\right)$$

Table 3 shows that by increasing the snubber resistor from 54 kΩ to 99 kΩ the snubber voltage increases from 40.1 V to 97 V.

Table 3

Parameter	Symbol	600 V design	700 V P7 design
Leakage inductance	$L_{leakage}$	25 µH	25 µH
Peak primary current under load at high line	I_{pri}	0.43 A	0.62 A
Snubber resistor	$R_{snubber}$	54 kΩ	99 kΩ
Switching period	T_s	28.6 µs	28.6 µs

Parameter	Symbol	600 V design	700 V P7 design
Snubber voltage	$V_{snubber}$	40.1 V	97 V

Table 4 sums up the different voltage components of the V_{DS} waveform to arrive at the total calculated peak MOSFET V_{DS}. As shown in Figure 5, the total drain source voltage of the MOSFET is the sum of the bus voltage, the reflected voltage, and the snubber voltage. Even with increasing the overall drain source voltage (V_{DS}) by 34 V we still have an increase in margin from the MOSFET breakdown voltage. In this new design the margin has increased from 12 percent to 20 percent. This increases the overall margin from the MOSFET breakdown voltage while still increasing the peak drain source voltage. In reality, when measured under worst-case conditions this 20 perecent margin corresponds to 599 V or 15 percent margin. The difference between measured and calculated peak voltages comes from the fact that the snubber voltage equation above assumes an infinite snubber capacitor value. Because of this discrepancy, the drain source peak voltage at full load and high line should be empirically verified in the design.

Table 4

Parameter	Symbol	600 V design	700 V P7 design
Primary bus voltage @265 V_{AC}	V_{bus}	373 V	373 V
Reflected voltage	$V_{reflected}$	117 V	97 V
Snubber voltage	$V_{snubber}$	40.1 V	90 V
Drain source voltage maximum	V_{DS_max}	526 V	560 V
Margin from breakdown voltage	V_{DS_margin}	12 %	20 %

In order to increase the power level from 35 W to 40 W, the output diode of the power supply needed less power dissipation at full load. A diode with a lower forward voltage drop was selected that improves the output power dissipation by 150 mW, even when operated at a higher output power levels and thus a higher output current. This reduces the temperature sufficiently to allow increasing the total output power.

Table 5

Parameter	Symbol	600 V design	700 V P7 design
Output current	I_{output}	1.84 A	2.11 A
Diode forward voltage	$V_{forward}$	0.55 V	0.40 V
Diode conduction losses	P_{dio}	1.01 W	0.84 A

With all of these changes made to the design, the overall efficiency improvement can be seen in Figure 8 and Figure 9 below. The light load benefits come from the P7 700 V switching loss improvements and RCD snubber changes. The P7 switching loss improvements can be seen by looking at the IPA60R600P6 to IPA70R600P7S delta efficiency curves shown in Figure 10 and Figure 11. The full load efficiency improvements come from changing to a better output diode with a lower forward voltage drop. By making these changes, the power level of the design was increased without switching to a lower $R_{DS(on)}$ device which would have cause an increase in the overall BOM cost.

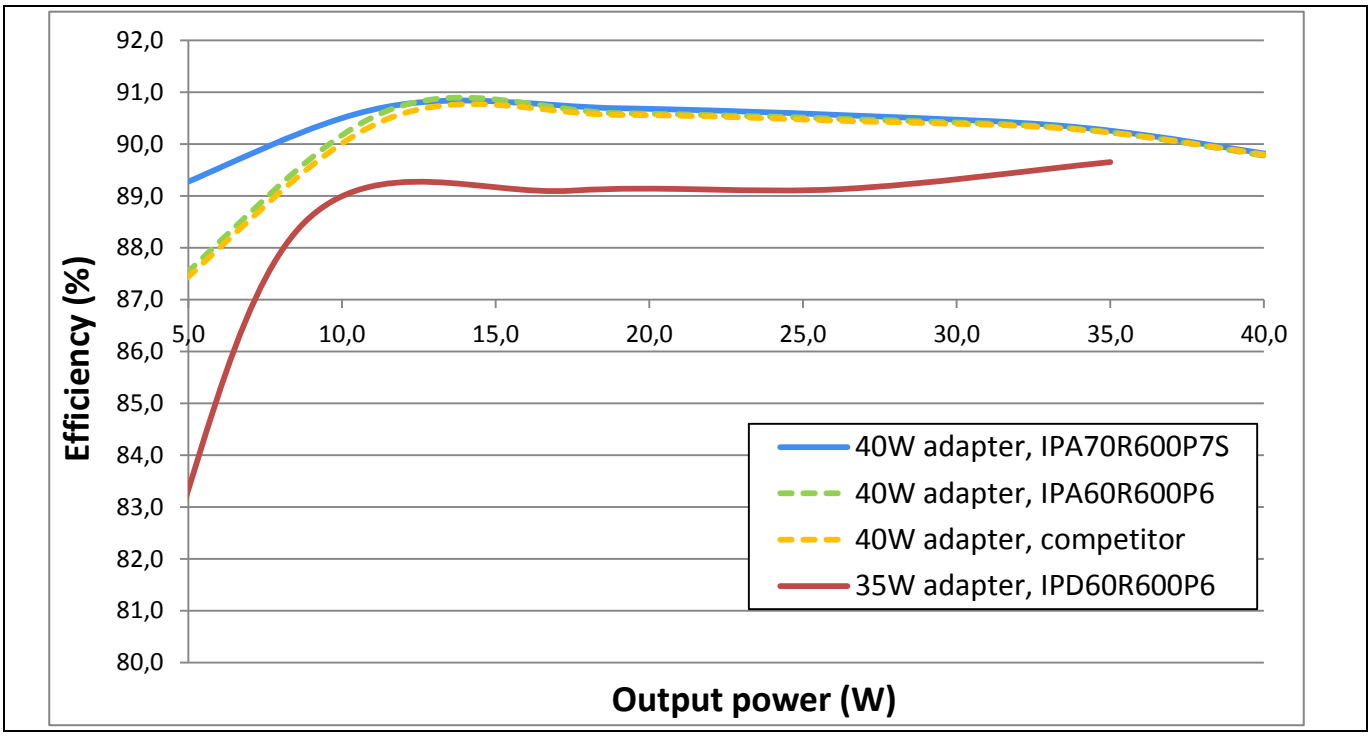

Figure 8 40 W adapter efficiency at 120 V_{AC} using IPA70R600P7S efficiency vs. a 35 W adapter design using a P6 device.

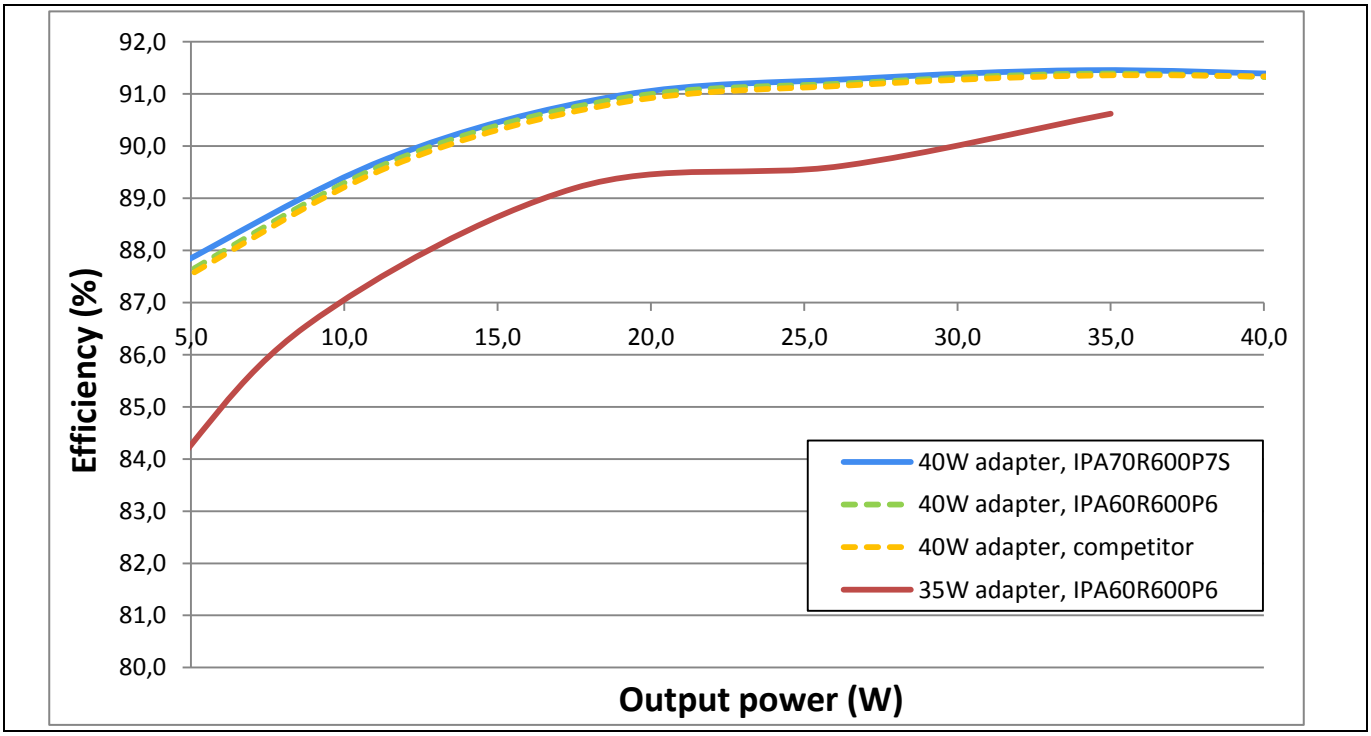

Figure 9 40 W adapter efficiency at 230 V_{AC} using IPA70R600P7S efficiency vs. a 35 W adapter design using a P6 device.

Figure 10 and Figure 11 below show the benefits of changing from IPA60R600P7 or a competitor's device to a P7 device. The efficiency graphs below are done as efficiency deltas relative to the P7 IPA70R600P7S in order to make the efficiency differences clearer. The 100 V_{AC} and full load efficiency difference ends up reducing the mold compound temperature by 2.9 °C.

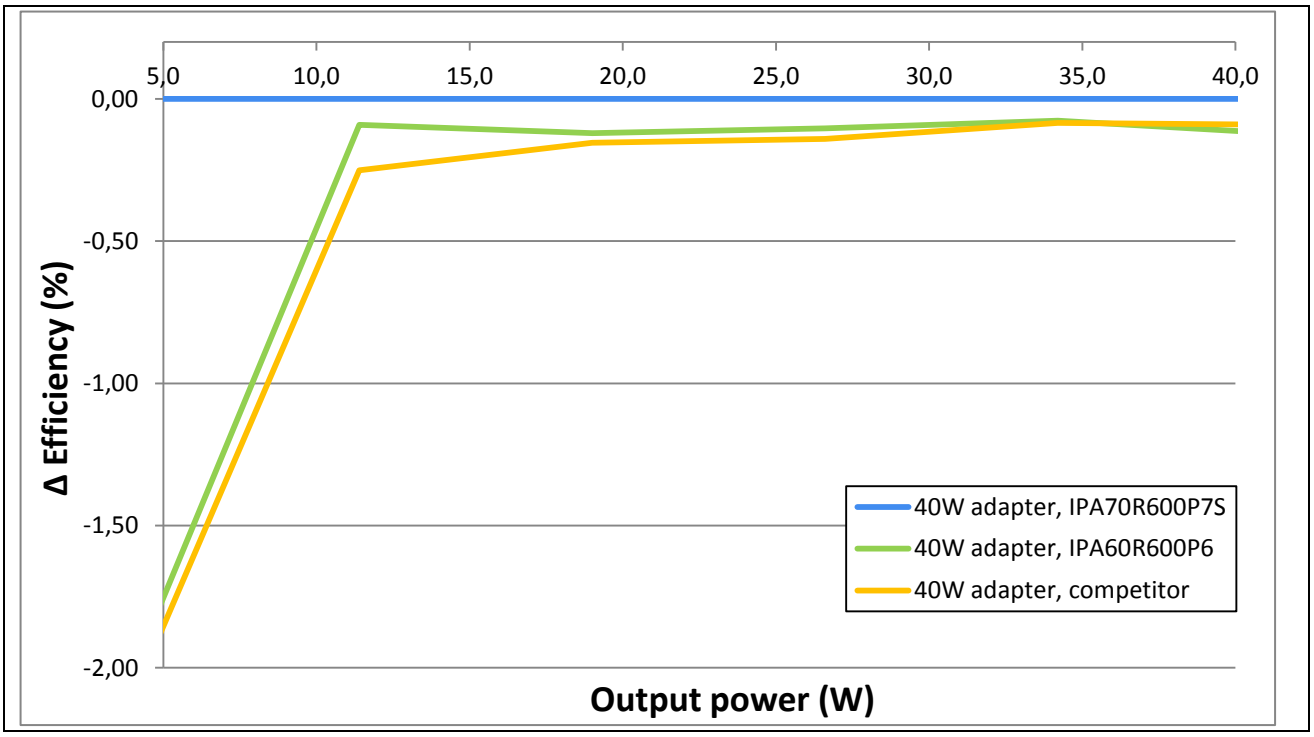

Figure 10 Efficiency of the 40 W adapter at 120 V_{AC} showing the P6 and competitor's devices referenced to the P7 MOSFET.

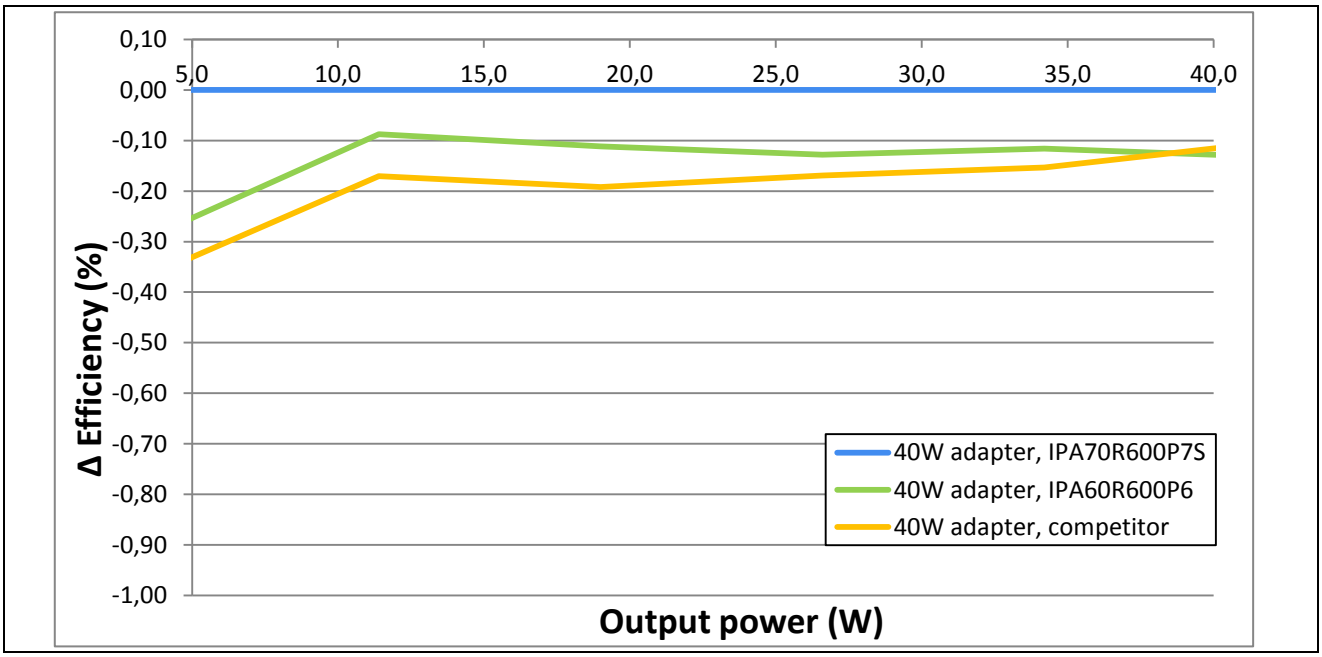

Figure 11 Efficiency of the 40 W adapter at 230 V_{AC} showing the P6 and competitor's devices referenced to the P7 MOSFET.

5.2 Thermal performance improvement

The worst-case nominal thermal conditions for the system under steady state operation occur at 100 V_{AC} and full output power (40 W). Table 10 shows the thermal improvement of P7 700 V when used in the 40 W adapter at 100 V_{AC} and 40 W of output power due to the improvement in efficiency shown in the previous section. As shown below, the mold compound temperature of the P7 700 V device is 2.9 °C lower. Table 11 shows the maximum temperature under the worst-case operating conditions for these components when using the IPA70R600P7S. These component temperatures are the limiting factor for the overall power density of the converter and this can help to increase power density or improve thermal margins in designs.

Table 6 Flyback MOSFET thermal rise with 100 V_{AC}, 40 W output

Device	Temperature rise	Temperature Δ referenced to P7
Competition	51.3 °C	**+2.0 °C**
IPA60R600P6	52.2 °C	**+2.9 °C**
IPA70R600P7S	**49.3 °C**	**0.0°C**

Table 7 Maximum component thermal rise at 100 V_{AC}, 40W output

Ref. Des.	Component description	Maximum temperature rise
Q1	Flyback MOSFET	61.7 °C
D3	Bridge rectifier	54.9 °C
L1	Common Mode Choke	59.3 °C
T1	Flyback transformer	67.8 °C
D2	Flyback output diode	53.6 °C
R22, R23, R28	Flyback snubber resistors	79.2 °C

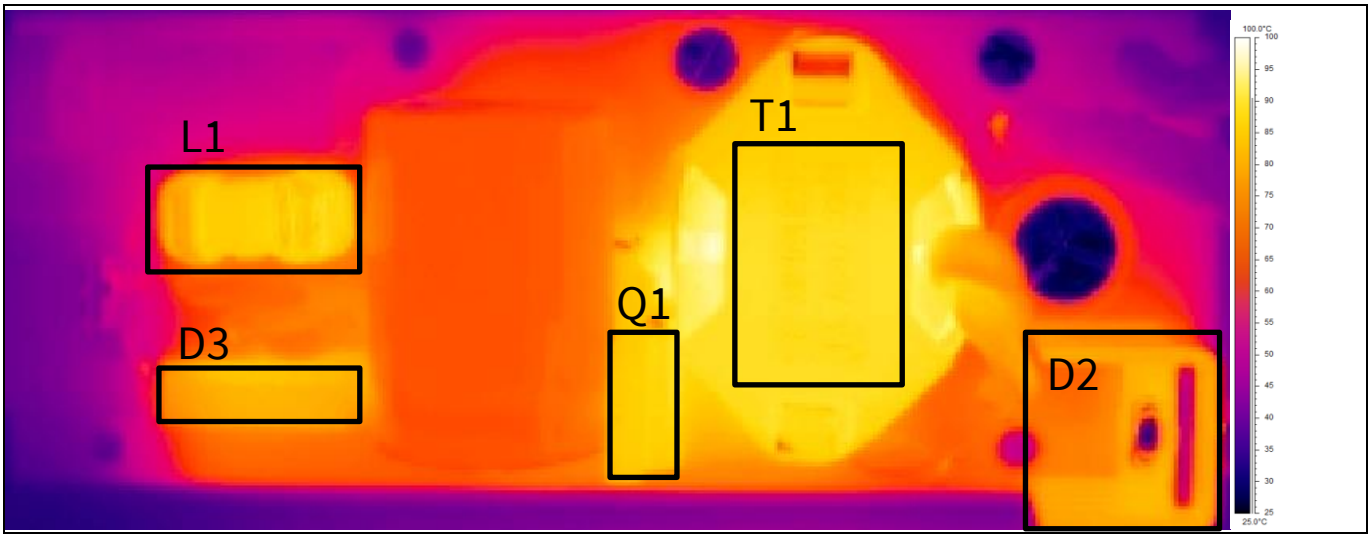

Figure 12 100 V_{AC} input, full load, top side. The line filter and bridge rectifier are hottest at this point due to higher AC input currents.

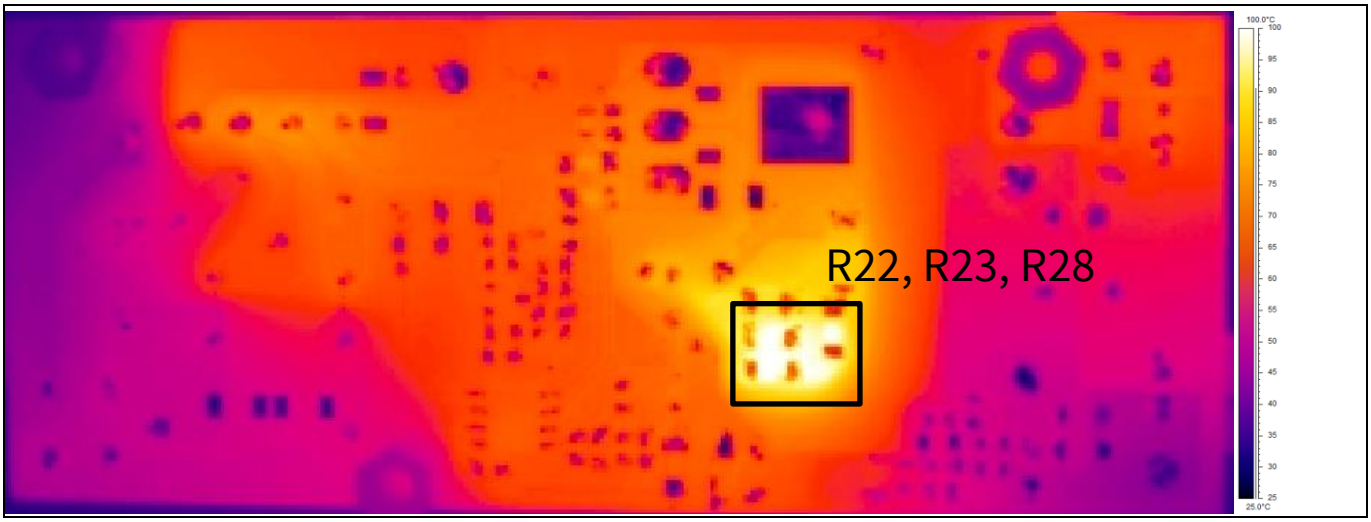

Figure 13 100 V_{AC} input, full load, bottom side. The snubber resistors are the hottest components.

5.3 UVLO circuit

The under voltage lock out (UVLO) circuit provides a mechanism to shut down the power supply when the AC line input voltage is lower than the specified voltage range. The UVLO event is detected by sensing the voltage level at U2's (TL431) REF pin (V_{REF_typ} = 2.5 V) through the voltage divider resistors (R12, R13, R14, and R17 in Figure 12) from the bulk capacitor C1. Q2 acts as a switch to enter or leave UVLO mode by controlling the FB pin voltage. Q3, together with R17, acts as voltage hysteresis for the UVLO circuit and U2 (TL431) act as a comparator. The system enters the UVLO mode by controlling the FB pin voltage of U1 to 0 V (when the voltage input level goes back to input voltage range), V_{REF} increases to 2.5 V (then switches Q2 and Q3 off) and V_{cc} hits 18 V, the UVLO mode is released. The calculation for the UVLO circuit is shown below:

V_{REF}= 2.5 V

R12 = 4.99 MΩ R13 = 4.99 MΩ R14 = 330 kΩ R17 = 681 kΩ

$$V_{bulk\_enterUVLO} = \frac{(R12 + R13 + R14)Vref}{R14}$$

$$V_{bulk\_leaveUVLO} = \frac{\left[\left(\frac{R14R17}{R14 + R17}\right) + R12 + R13\right]Vref}{\left(\frac{R14R17}{R14 + R17}\right)}$$

$$V_{bulk\_enterUVLO} = 77.8\ V_{DC}$$

$$V_{bulk\_leaveUVLO} = 114.3\ V_{DC}$$

The 'enter UVLO' threshold is set at 77.8 V_{DC} to allow for the BUS capacitance voltage to droop under 90 V_{AC} at full load operation with some margin to avoid false triggering.

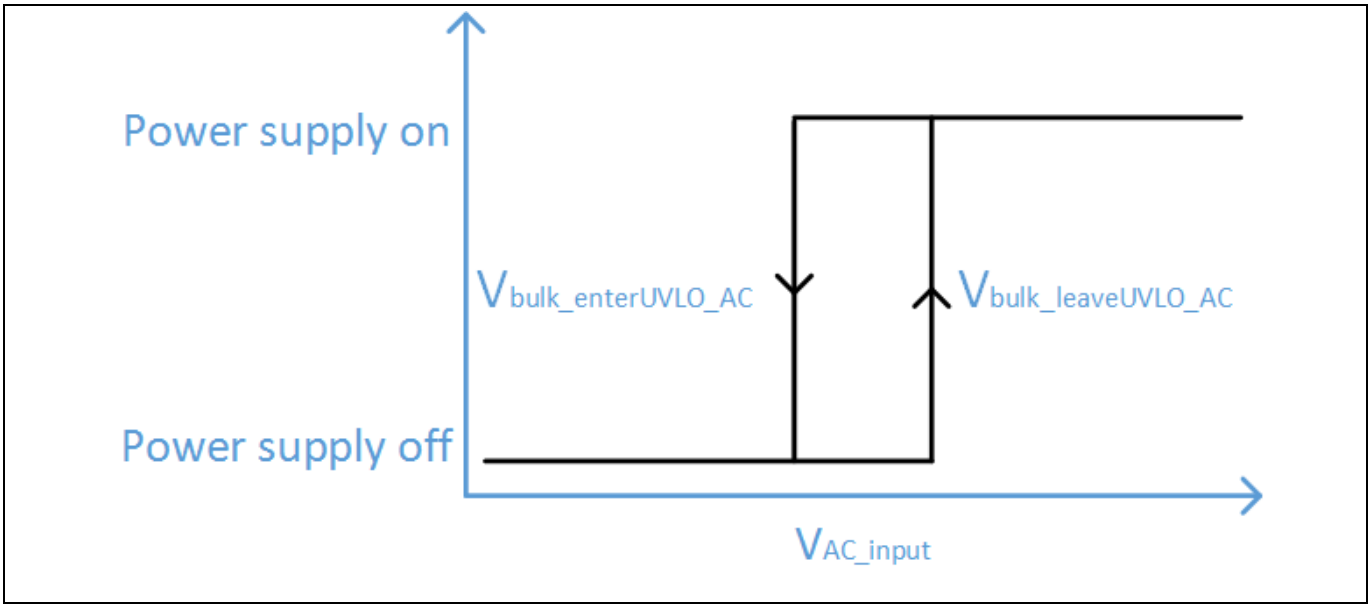

Figure 14 Power supply status vs. AC input voltage showing the hysteretic behavior of the UVLO circuit.

6 Demo board overview

6.1 Demo board pictures

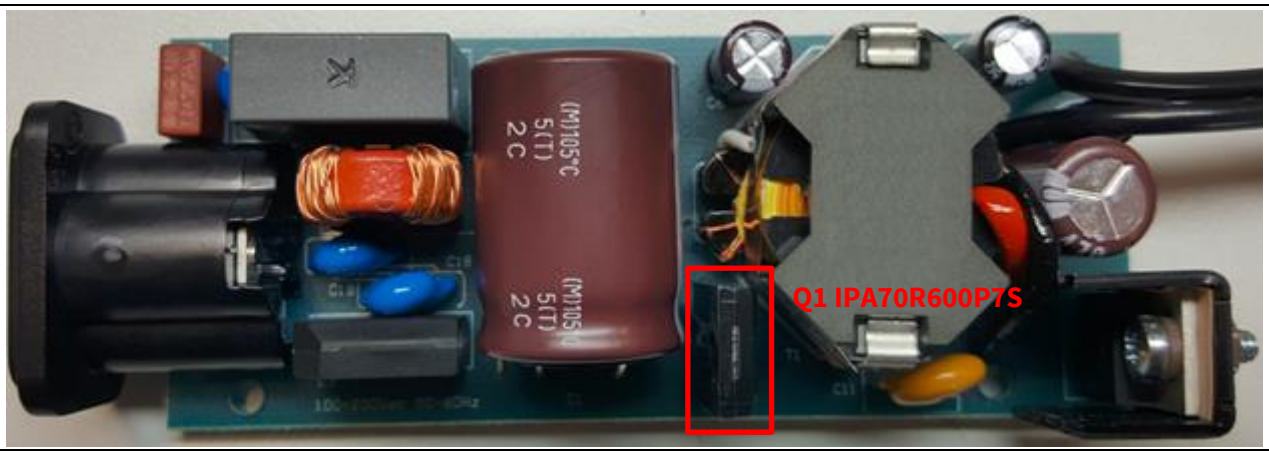

Figure 15 Top side of 40 W Infineon adapter with a TO-220 FullPAK populated

6.2 Demo board specifications

Table 8

Section	Parameter	Specification
Input ratings	Input voltage	90 V_{AC} – 265 V_{AC}
	Input frequency	47 Hz – 63 Hz
	Input current at 100 V_{AC}, 40 W	0.85 A maximum
	Power factor	0.53 @100 V_{AC} 0.36 @265 V_{AC}
	Peak efficiency 230 V_{AC}, 40 W Peak efficiency 120 V_{AC}, 40 W	91.3% 89.6%
	Surge	2 kV IEC61000-4-5
Output ratings	Nominal output voltage	19.0 V
	Tolerance	2%
	Output current	2.10 A
	Output power	40 W
	Line regulation	0.5%
	Load regulation	0.5%
	Output ripple	<200 mV_{PP}
	Quiescent power draw	55 mW @100 V_{AC} 111 mW @265 V_{AC}
	Switching frequency	25 kHz– 60 kHz
Mechanical	Dimensions	Length: 10.0 cm (3.94 in.) Width: 3.7 cm (1.46 in.) Height: 2.6 cm (1.02 in.)
Environmental	Ambient operating temperature	-25°C to 50°C

6.3 Demo board features

- **Fold back point protection** - For a QR flyback converter, the maximum possible output power is increased when a constant current limit value is used across the entire mains input voltage range. This is usually not desired as this will increase the cost of the transformer and output diode in the case of output over power conditions. The internal fold back protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of the ZC pin, during the MOSFET on-time. As the result, the maximum current limit adjusts with the AC line voltage.
- **V_{CC} over voltage and under voltage protection** - During normal operation, the V_{cc} voltage is continuously monitored. When the V_{cc} voltage increases to VVCC OVP or V_{cc} voltage falls below the under voltage lock out level VVCC off, the IC will enter into auto restart mode.
- **Over load/open loop protection** - In the case of an open control loop, the feedback voltage is pulled up with an internal block. After a fixed blanking time, the IC enters into auto restart mode. In case of a secondary short-circuit or overload, the regulation voltage V_{FB} will also be pulled up, the same protection is applied and the IC will auto restart.
- **Adjustable output overvoltage protection** - During the off-time of the power switch, the voltage at the zero-crossing pin, ZC, is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7 V for a preset period of 100 µs, the IC is latched off.
- **Auto restart for over temperature protection** - The IC has a built-in over temperature protection function. When the controller's temperature reaches 140 °C, the IC will shut down the switch and enters into auto restart. This can protect the power MOSFET from overheating.
- **Short winding protection** - The source current of the MOSFET is sensed via external resistors, R15 and R16. If the voltage at the current sensing pin is higher than the preset threshold VCSSW of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch off, a spike blanking time of 190 ns is integrated in the output of internal comparator.

6.4 Schematic

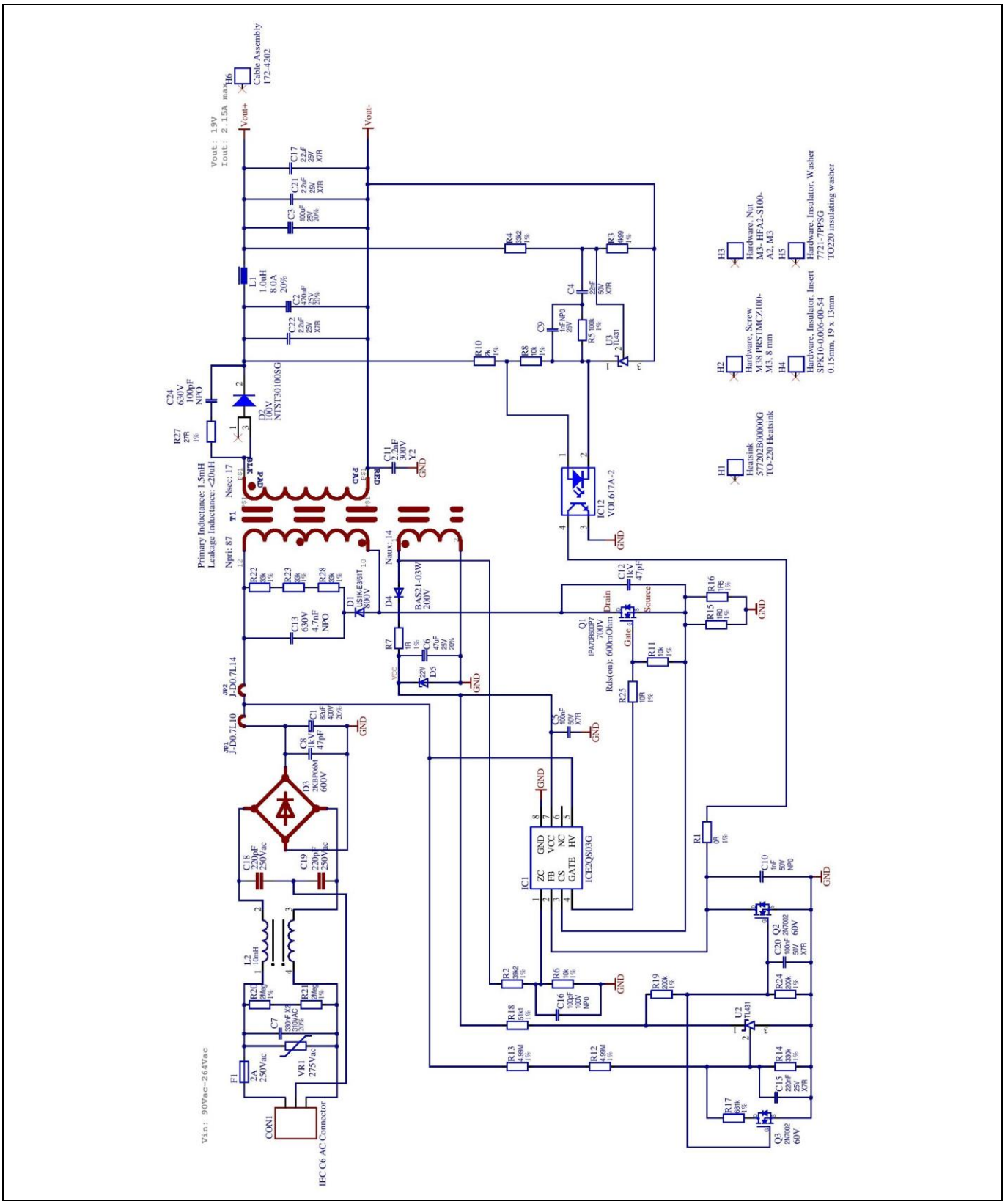

Figure 16 40 W adapter schematic

6.5 BOM with Infineon components in bold

Table 9

Reference	Description	Part number	Manufacturer
C1	Electrolytic capacitor, 82 uF, 20%, 400 V	EKXG401ELL820MM25S	United Chemi-Con
C2	Electrolytic capacitor, 470 uF, 20%, 25 V	EKZE250ELL471MJ16S	United Chemi-Con
C3	Electrolytic capacitor, 100 uF, 20%, 25 V	EEU-FR1E101	Panasonic
C4	Capacitor ceramic, 22 nF, X7R, 50 V, CAP0805W	VJ0805Y223KNAAO	Vishay
C5, C20	Capacitor ceramic, 100 nF, X7R, 50 V, CAP0805W	C2012X7R2A104K125AA	TDK
C6	Electrolytic capacitor, 47uF, 20%, 25V, 5 mm	UPM1E470MED	Nichicon
C7	Foil capacitor, 330 nF X2, 20%, 310 V_{AC}, C_Foil 15 mm - V2	R463I33305002K	Kemet
C10	Capacitor ceramic, 1nF, NP0, 50 V, CAP0805W	CGA4C2C0G1H102J060AA	TDK
C11	Capacitor Y2, 2.2 nF, Y2, 300 V, CAP-DISC 7.5 mm	AY2222M35Y5US63L7	Vishay
C13	Capacitor ceramic, 4.7 nF, NPO, 630 V, CAP1206W	C1206C472JBGACTU	Kemet
C15	Capacitor ceramic, 220 nF, X7R, 25 V, CAP0805W	C2012X7R1H224K125AA	TDK
C16	Capacitor ceramic, 100pF, NP0, 100 V, CAP0805W	CGA4C2C0G2A101J060AA	TDK
C17, C21, C22	Capacitor ceramic, 2.2 uF, X7R, 25 V, CAP1206W	C3216X7R1E225K160AA	TDK
C18, C19	220pF/250 V_{AC}, 220pF, 250 V_{ac}, C075-045X100	VY2221K29Y5SS63V0	Vishay
C24	Capacitor ceramic, 100 pF, NPO, 630 V, CAP1206W	CGA5C4C0G2J101J060AA	TDK
CON1	ST-04A, IEC C6 AC Connector, ST-A04	6160.0003	Schurter
D1	Diode, US1K-E3/61T, 600V, SMA	US1K-E3/61T	Vishay
D2	Diode, NTST30100SG, 100V, TO220_standing	NTST30100SG	OnSemi
D3	2KBP06M, 2KBP06M, 600V, KBPM	2KBP06M-E4/51	Vishay
D4	**Diode, BAS21-03W, 200V, SOD323**	**BAS21-03W**	**Infineon**
D5	Diode, 22V Zener, SOD323	BZX384-C22	NXP
F1	T2, 2 A, 250 V_{ac}, Fuse small	40012000440	Littelfuse
H1	Heatsink, TO-220 Heatsink	577202B00000G	Aavid thermalloy
H2	Hardware, Screw, M3, 8 mm	M38 PRSTMCZ100-	DURATOOL

Reference	Description	Part number	Manufacturer
H3	Hardware, Nut, A2, M3	M3- HFA2-S100-	DURATOOL
H4	Hardware, insulator, Insert, 0.15 mm, 19 x 13 mm	SPK10-0.006-00-54	Bergquist
H5	Hardware, insulator, washer, TO220 insulating washer	7721-7PPSG	AAVID THERMALLOY
H6	Cable assembly	172-4202	Memory Protection Devices, Inc.
IC1	**QR PWM controller**	**ICE2QS03G**	**Infineon**
IC12	VOL617A-2, VOL617A-2, LSOP 4pin	VOL617A-2X001T	Vishay
L1	Choke, 1.0 uH, 20%, INDUCTOR 4 u7 4,2 A	7447462010	Wurth
L2	Inductance, 10 mH, Inductor common mode small	744821110	Wurth
Q1	**NMOS, IPA70R600P7S, 700 V, TO220FP**	**IPA70R600P7S**	**Infineon**
Q2, Q3	**NMOS, 2N7002, 60 V, SOT23**	**2N7002**	**Infineon**
R1	Resistor, 0R, 1%, RES0805R	CRCW08050000Z0EA	Vishay
R2	Resistor, 39k2, 1%, RES0805R	ERJ6ENF3922V	Panasonic
R3	Resistor, 4k99, 1%, RES0805R	CRCW08054K99FKEA	Vishay
R4	Resistor, 33k2, 1%, RES0805R	CRCW080533K2FKEA	Vishay
R5	Resistor, 100k, 1%, RES0805R	CRCW0805100KFKEA	Vishay
R6, R8, R11	Resistor, 10k, 1%, RES0805R	CRCW080510K0FKEA	Vishay
R7, R15	Resistor, 1R, 1%, RES1206W	CRCW12061R00FKEA	Vishay
R10	Resistor, 2k, 1%, RES0805R	CRCW08052K00FKEA	Vishay
R12, R13	Resistor, 4.99M, 1%, RES1206W	CRCW12064M99FKEB	Vishay
R14	Resistor, 330k, 1%, RES0805R	CRCW0805330KFKEA	Vishay
R16	Resistor, 1R5, 1%, RES1206W	CRCW12061R50JNEAIF	Vishay
R17	Resistor, 681k, 1%, RES0805R	CRCW0805681KFKEA	Vishay
R18	Resistor, 51k1, 1%, RES0805R	ERJ6ENF5112V	Panasonic
R19, R24	Resistor, 200k, 1%, RES0805R	CRCW0805200KFKEA	Vishay
R22, R23, R28	Resistor, 33k, 1%, RES1206W	CRCW120633K0FKEA	Vishay
R25	Resistor, 10R, 1%, RES1206W	CRCW120610R0FKEA	Vishay
R27	Resistor, 27R, 1%, RES1206W	CRCW120627R0FKEA	Vishay
T1	Transformer, RM10	ICE160487(spec_700V_v1)	I.C.E. Transformers
U2, U3	Reference IC, TL431	TL431ACDBZT	TI
VR1	Varistor, 8.6J, 275Vac	B72205S0271K101	EPCOS

6.6 PCB layout

The PCB was designed using Altium Designer 16. Schematic and board files are available on request.

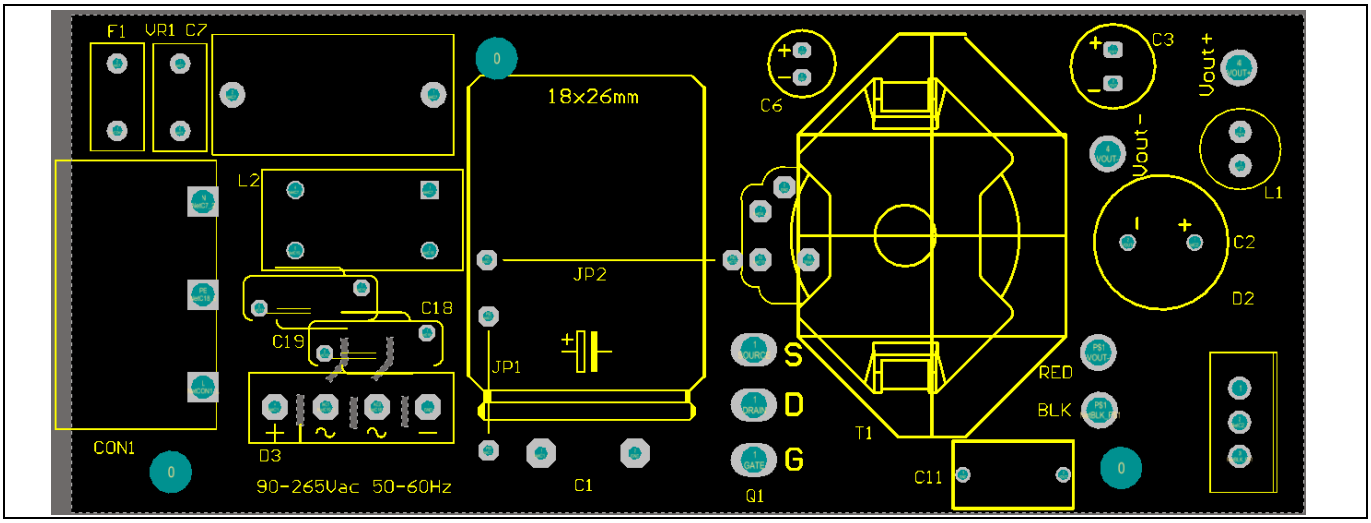

Figure 17 Board layout top

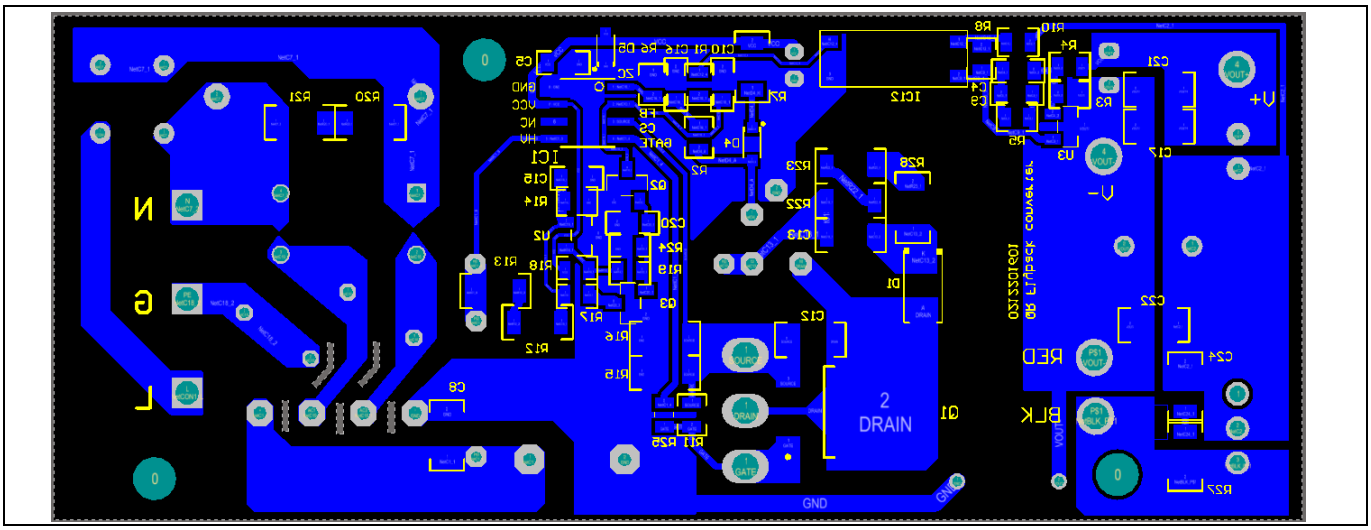

Figure 18 Board layout bottom

6.7 Transformer construction

The transformer for the 40 W adapter was built by I.C.E. Transformers: http://www.icetransformers.com/

Table 10 Transformer specification

Manufacturer	I.C.E. Transformers
Core size	RM10
Core material	3C95
Bobbin	8 pin RM10 vertical
Primary inductance	1500 µH measured from pin 6 to pin 4 @10kHz
Leakage inductance	< 25 µH measured from pin 6 to pin 4 @10kHz pins S-,S+,1, and 2 shorted

*100% of components are Hi-Pot tested to 4.2 kV primary to secondary for 1 minute

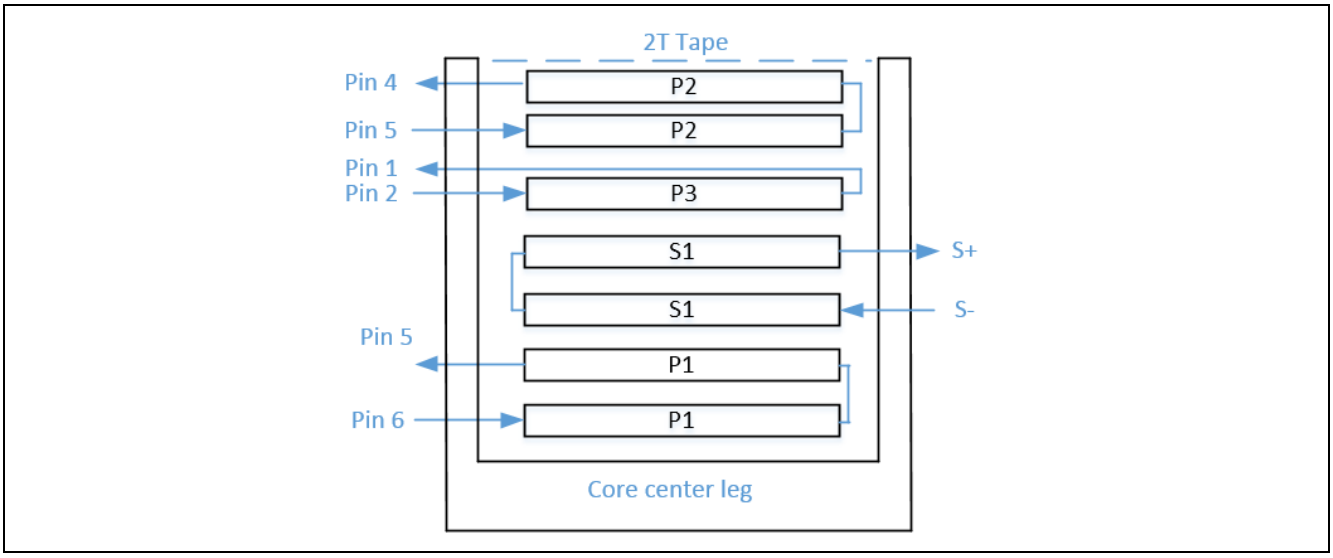

Figure 19 Transformer windings stackup

1. S- in red tube, S+ in black tube
2. S- length ***30 mm***, solder length 5 mm
3. S+ length ***30 mm***, solder length 5 mm
4. Cut pin 3, pin 5, core clip PCB mount pins, and secondary pins.
5. Add a flux band of 8mm copper foil with 2 layers of tape and 3mm of cuffing on each side. Add around the core with the tape side facing out. Using ϕ0.35 mm solder to pin 2.
6. Vacuum varnish the entire assembly.
7. Cut the core clamp pins off of the transformer.

Table 11 Transformer windings stackup

Name	Start	Stop	Turns	Wire gauge	Layer	Winding
P1	6	5	58	1 x ϕ0.35 mm	Primary	Evenly spaced
S1	S-	S+	17	2 x ϕ 0.5 mm triple insulated	Secondary	Evenly spaced
P3	2	1	14	1 x ϕ0.15 mm, with margin tape	Auxiliary	Evenly spaced
P2	5	4	29	1 x ϕ0.35 mm	Primary	Evenly spaced
T1			2	tape		

7 Measurements

7.1 High line and low line operation

Figure 20 **High line (265 V_{AC}), no load. The ICE2QS03G is operating in burst mode to minimize idle power consumption. The burst mode pulse train shown above occurs every 33.8 ms. QR valley switching does not occur during burst mode due to the ICE2QS03G changing operating modes at light load. V_{DS} maximum is only 553 V in burst mode operation.**

CH1 (Yellow): Q1 V_{DS}
CH2 (Cyan): Q1 I_{DS}
CH3 (Magenta): Q1 V_{GS}

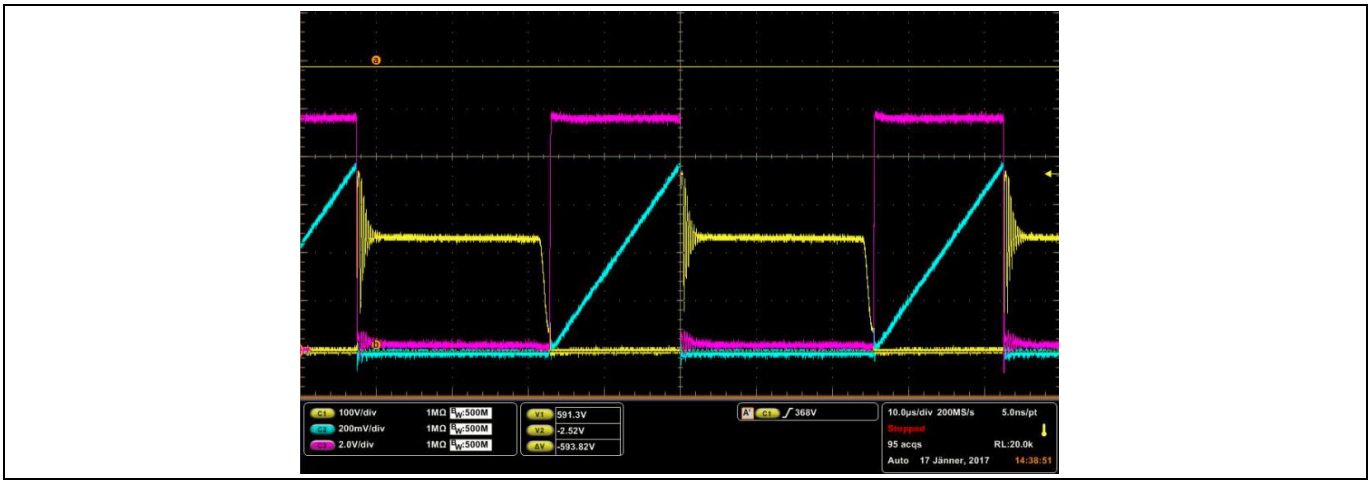

Figure 21 **Low line (100 V_{AC}), Full load (40 W). This is the peak current that the primary MOSFET Q1 will encounter during steady-state operation. The measured peak current is 1.3 A (780 mV / 0.6 Ω) giving margin from the power supply maximum current limit of 1.6 A. This is necessary for brown out conditions (90 V_{AC}) and design tolerance.**

CH1 (Yellow): Q1 V_{DS}
CH2 (Cyan): Q1 I_{DS}
CH3 (Magenta): Q1 V_{GS}

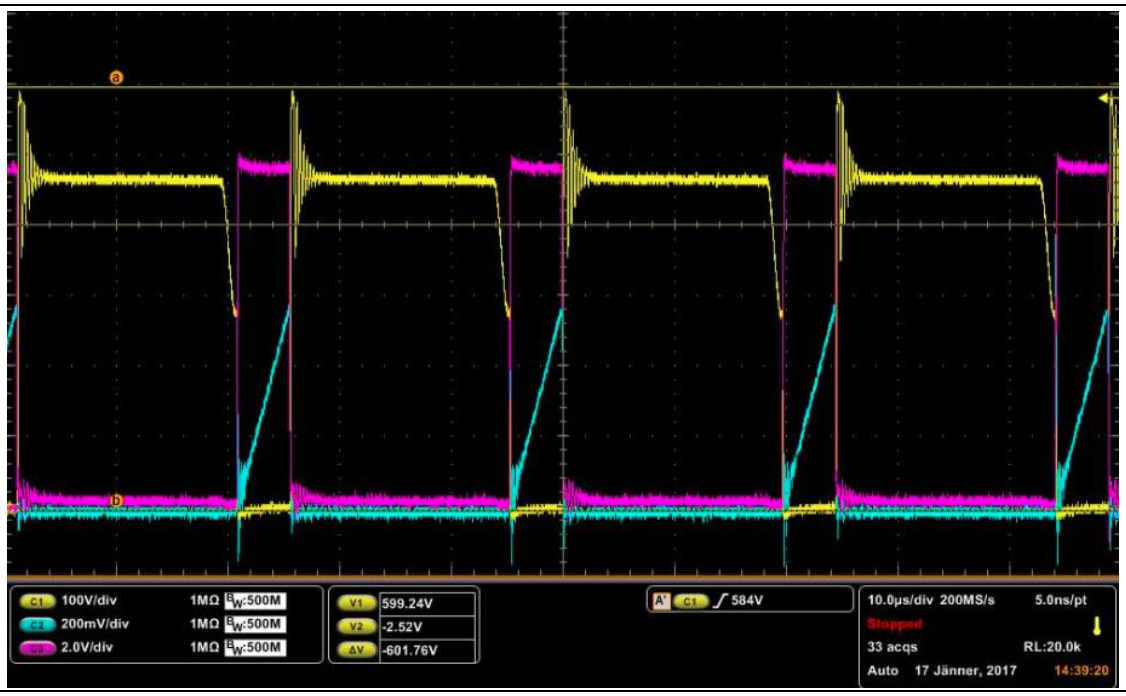

Figure 22 High line (265 V_{AC}), Full load (40 W). This shows the worst case drain source voltage of 599 V. This still gives 14.4 percent margin from the MOSFET breakdown voltage under worst case conditions. The measured peak voltage is higher than calculated due to the snubber equation not considering the RCD snubber capacitance.

CH1 (**Yellow**): Q1 V_{DS}
CH2 (**Cyan**): Q1 I_{DS}
CH3 (**Magenta**): Q1 V_{GS}

8 Conclusion

The P7 series of CoolMOS™ MOSFETs offer the best solution for flyback applications. The improvement in switching loss performance over the Infineon CoolMOS™ P6 and competitor devices in this particular design leads to 120 V_{AC} and light load (5 W) efficiency improvements of 2.0 percent and 0.3 percent at 230 V_{AC}. There is also an improvement at 35 W of 0.1 percent at both high line and low line. The improved efficiency of the P7 700 V MOSFET leads to a 2.9 °C thermal improvement at 100 V_{AC} and full load operation. The improved efficiency of the P7 700 V MOSFETs is then used to increase the 35 W adapter design to 40 W with the same $R_{DS(on)}$ value. The 700 V breakdown voltage allows for additional safety margin when compared to 650 V for improved surge robustness. The drain source voltage margin is increased by 8 percent while still increasing the drain source voltage compared to a 600 V MOSFET. These changes can be implemented in other charger and adapter designs in order to take advantage of the benefits of the P7 700 V MOSFET. This new benchmark in 700 V MOSFETs enables higher efficiency, higher power density, and more robust designs.

9 References

[1] Design Guide for QR Flyback Converter

[2] IPA70R600P7S data sheet, 700 V CoolMOS™ P7 Power Transistor

[3] 700 V CoolMOS P7™ Application Note

[4] ICE2QS03G data sheet, Infineon Technologies AG

[5] 2N7002 data sheet, Infineon Technologies AG

[6] BAS21-03W data sheet, Infineon Technologies AG

[7] ICE2QS03G design guide. [ANPS0027]

[8] Converter Design Using the Quasi-Resonant PWM Controller ICE2QS03, Infineon Technologies AG, 2006. [ANPS0003]

Revision history

Major changes since the last revision

Page or reference	Description of change

Edition 2017-01-20

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

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Document reference

ifx1

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