

Features

- Low-voltage and Standard-voltage Operation
 - 1.8 ($V_{CC} = 1.8V$ to 5.5V)
- Internally Organized 512 x 8 (4K), or 1024 x 8 (8K)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (1.8V, 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 16-byte Page (4K, 8K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra-Thin Mini-MAP (MLP 2x3), 5-lead SOT23, 8-lead TSSOP and 8-ball dBG2 Packages
- Lead-free/Halogen-free
- Die Sales: Wafer Form and Tape and Reel

Description

The AT24C04B/08B provides 4096/8192 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 512/1024 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C04B/08B is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra-Thin Mini-MAP (MLP 2x3), 5-lead SOT23, 8-lead TSSOP, and 8-ball dBG2 packages and is accessed via a Two-wire serial interface. In addition, the AT24C04B/08B is available in 1.8V (1.8V to 5.5V) version.

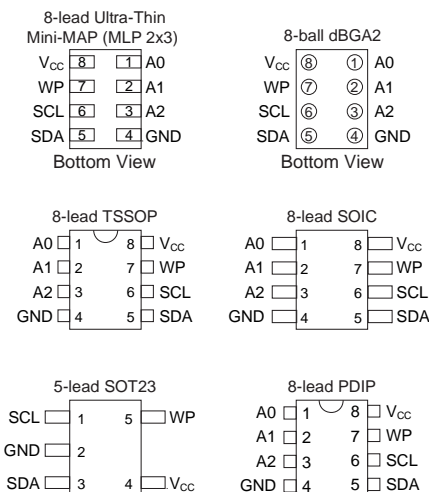
Figure 1. Pin Configurations

| Pin Name | Description |
|-----------------|--------------------|
| A0 – A2 | Address Inputs |
| SDA | Serial Data |
| SCL | Serial Clock Input |
| WP | Write Protect |
| NC | No Connect |
| GND | Ground |
| V _{CC} | Power Supply |

Note: For use of 5-lead SOT23

4K: The software A2 and A1 bits in the device address word must be set to zero to properly communicate.

8K: The software A2 bit in the device address word must be set to zero to properly communicate.



**Two-wire
Serial EEPROM**
4K (512 x 8)
8K (1024 x 8)

**AT24C04B
AT24C08B**

**Not Recommended
for New Design.
Replaced by
AT24C04C or
AT24C08C.**

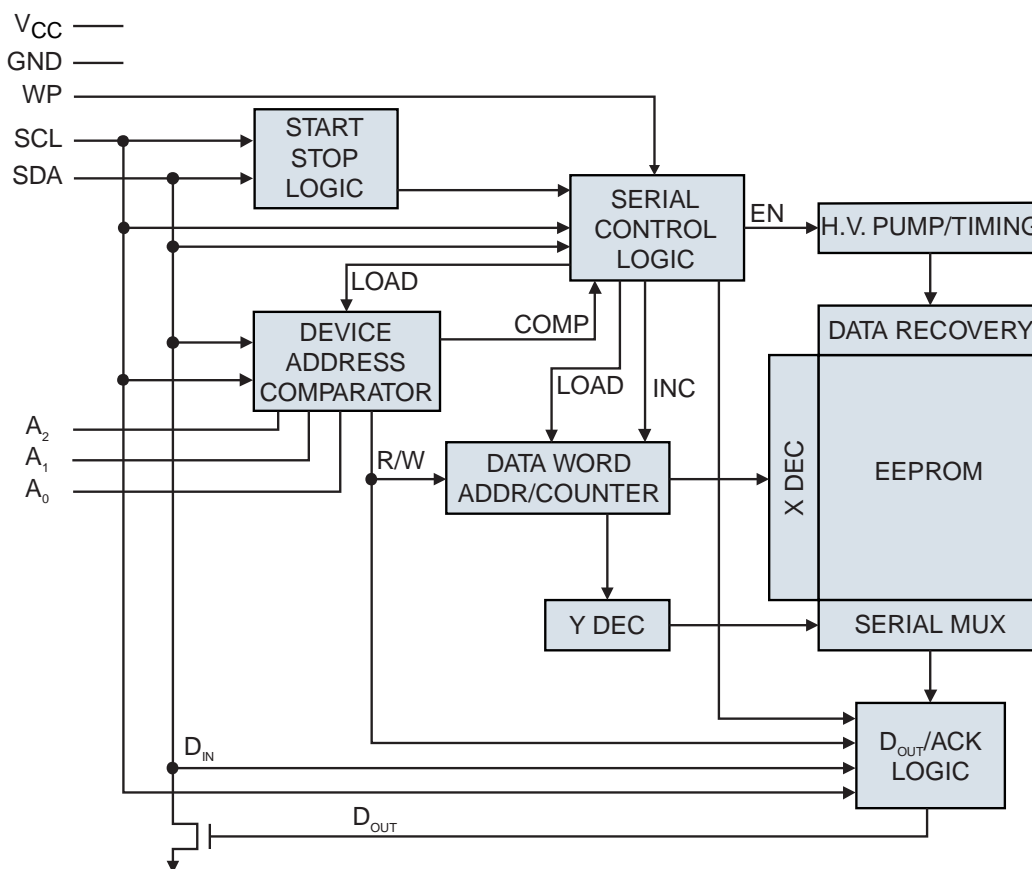


Absolute Maximum Ratings

| | |
|--|------------------|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to + 150°C |
| Voltage on Any Pin with Respect to Ground | - 0.1V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The AT24C04B uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect and can be connected to ground (device addressing is discussed in detail under the Device Addressing section).

The AT24C08B only uses the A2 input for hardware addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects and can be connected to ground (device addressing is discussed in detail under the Device Addressing section).

Table 1. Write Protect

| WP Pin Status | Part of the Array Protected |
|---------------|------------------------------|
| | 24C04B/08B |
| At V_{CC} | Full Array |
| At GND | Normal Read/Write Operations |





2. Memory Organization

AT24C04B, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08B, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

Table 2. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$

| Symbol | Test Condition | Max | Units | Conditions |
|-----------|--|-----|-------|-----------------------|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O} = 0\text{V}$ |
| C_{IN} | Input Capacitance (A_0 , A_1 , A_2 , SCL) | 6 | pF | $V_{IN} = 0\text{V}$ |

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics

Applicable over recommended operating range from:

$T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|-----------|---|--------------------------------|---------------------|------|---------------------|---------------|
| V_{CC1} | Supply Voltage | | 1.8 | | 5.5 | V |
| V_{CC2} | Supply Voltage | | 2.5 | | 5.5 | V |
| V_{CC3} | Supply Voltage | | 2.7 | | 5.5 | V |
| V_{CC4} | Supply Voltage | | 4.5 | | 5.5 | V |
| I_{CC} | Supply Current $V_{CC} = 5.0\text{V}$ | READ at 100 kHz | | 0.4 | 1.0 | mA |
| I_{CC} | Supply Current $V_{CC} = 5.0\text{V}$ | WRITE at 100 kHz | | 2.0 | 3.0 | mA |
| I_{SB1} | Supply Current $V_{CC} = 1.8\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 0.6 | 3.0 | μA |
| I_{SB2} | Supply Current $V_{CC} = 2.5\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 1.4 | 4.0 | μA |
| I_{SB3} | Supply Current $V_{CC} = 2.7\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 1.6 | 4.0 | μA |
| I_{SB4} | Supply Current $V_{CC} = 5.0\text{V}$ | $V_{IN} = V_{CC}$ or V_{SS} | | 8.0 | 18.0 | μA |
| I_{LI} | Input Leakage Current | $V_{IN} = V_{CC}$ or V_{SS} | | 0.10 | 3.0 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = V_{CC}$ or V_{SS} | | 0.05 | 3.0 | μA |
| V_{IL} | Input Low Level ⁽¹⁾ | | - 0.6 | | $V_{CC} \times 0.3$ | V |
| V_{IH} | Input High Level ⁽¹⁾ | | $V_{CC} \times 0.7$ | | $V_{CC} + 0.5$ | V |
| V_{OL2} | Output Low Level $V_{CC} = 3.0\text{V}$ | $I_{OL} = 2.1\text{ mA}$ | | | 0.4 | V |
| V_{OL1} | Output Low Level $V_{CC} = 1.8\text{V}$ | $I_{OL} = 0.15\text{ mA}$ | | | 0.2 | V |

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $CL = 1$ TTL Gate and 100 pF (unless otherwise noted)

| Symbol | Parameter | 1.8, 2.5, 2.7 | | 5.0-volt | | Units |
|--------------------------|---|---------------|-----|----------|------|---------------|
| | | Min | Max | Min | Max | |
| f_{SCL} | Clock Frequency, SCL | | 400 | | 1000 | kHz |
| t_{LOW} | Clock Pulse Width Low | 1.2 | | 0.4 | | μs |
| t_{HIGH} | Clock Pulse Width High | 0.6 | | 0.4 | | μs |
| t_I | Noise Suppression Time | | 50 | | 40 | ns |
| t_{AA} | Clock Low to Data Out Valid | 0.1 | 0.9 | 0.05 | 0.55 | μs |
| t_{BUF} | Time the bus must be free before a new transmission can start | 1.2 | | 0.5 | | μs |
| $t_{HD,STA}$ | Start Hold Time | 0.6 | | 0.25 | | μs |
| $t_{SU,STA}$ | Start Setup Time | 0.6 | | 0.25 | | μs |
| $t_{HD,DAT}$ | Data in Hold Time | 0 | | 0 | | μs |
| $t_{SU,DAT}$ | Data In Setup Time | 100 | | 100 | | ns |
| t_R | Inputs Rise Time ⁽¹⁾ | | 0.3 | | 0.3 | μs |
| t_F | Inputs Fall Time ⁽¹⁾ | | 300 | | 100 | ns |
| $T_{SU,STO}$ | Stop Setup Time | 0.6 | | .25 | | μs |
| t_{DH} | Data Out Hold Time | 50 | | 50 | | ns |
| t_{WR} | Write Cycle Time | | 5 | | 5 | ms |
| Endurance ⁽¹⁾ | 5.0V, 25°C , Byte Mode | 1M | | 1M | | Write cycles |

Note: 1. This parameter is ensured by characterization only.

3. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see [Figure 6](#)). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see [Figure 7](#)).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see [Figure 7](#)).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

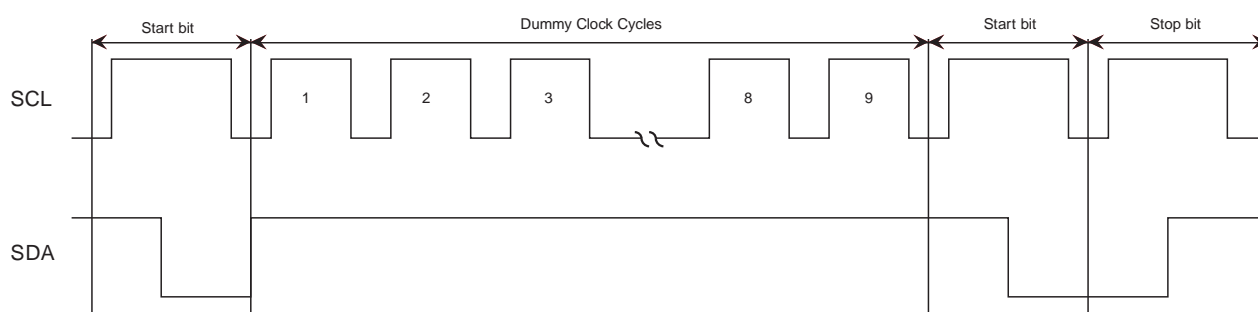
STANDBY MODE: The AT24C04B/08B features a low-power standby mode which is enabled:

- (a) Upon power-up and
- (b) After the receipt of the STOP bit and the completion of any internal operations.

2-WIRE SOFTWARE RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

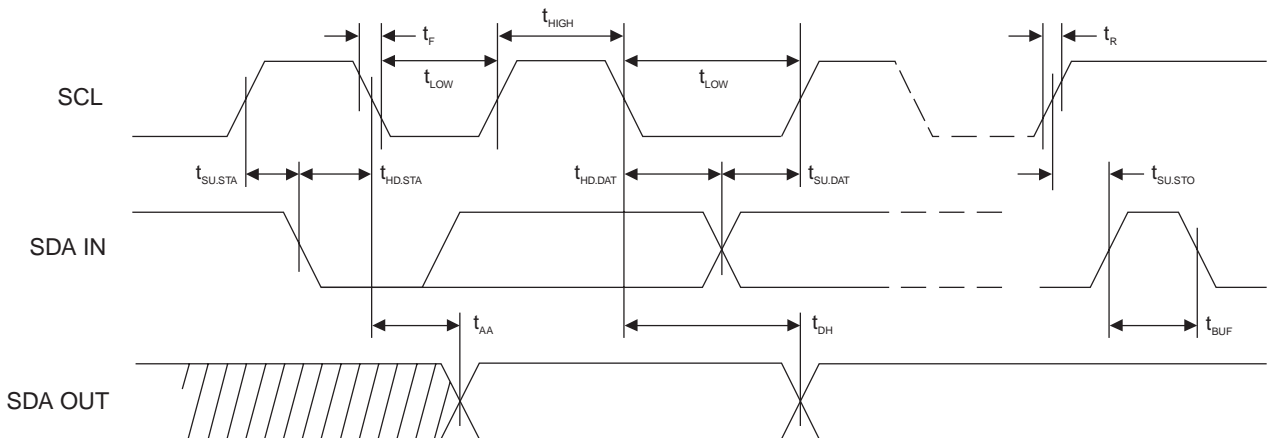
- (a) Create a start bit condition,
- (b) Clock 9 cycles,
- (c) Create another start bit followed by a stop bit condition as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 3. Software reset



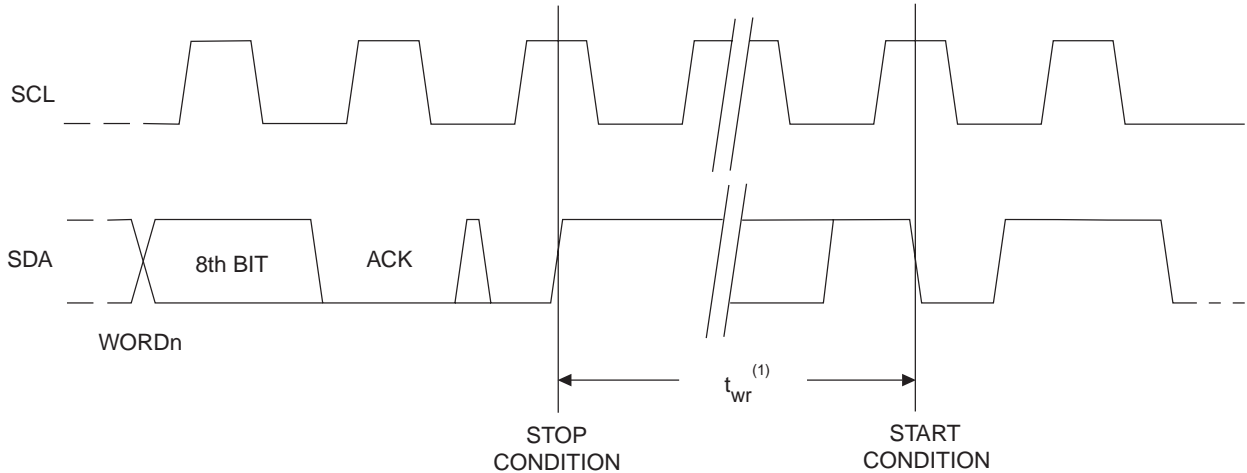
4. Bus Timing

Figure 4. SCL: Serial Clock, SDA: Serial Data I/O®



5. Write Cycle Timing

Figure 5. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 6. Data Validity

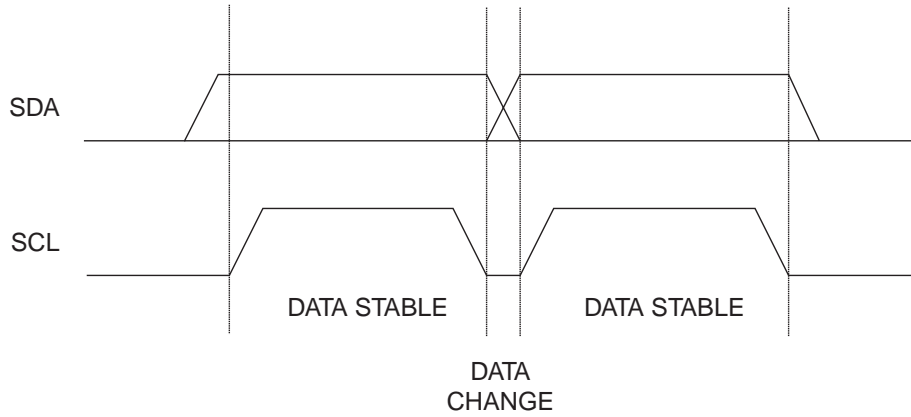


Figure 7. Start and Stop Definition

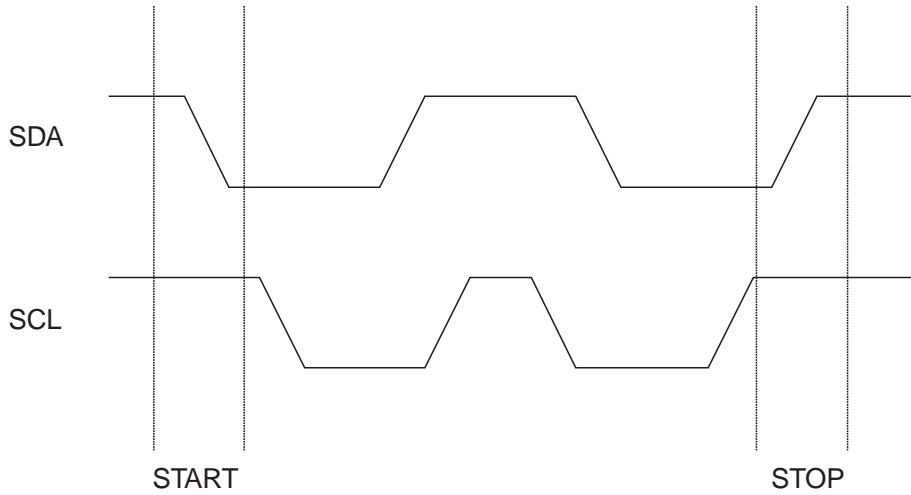
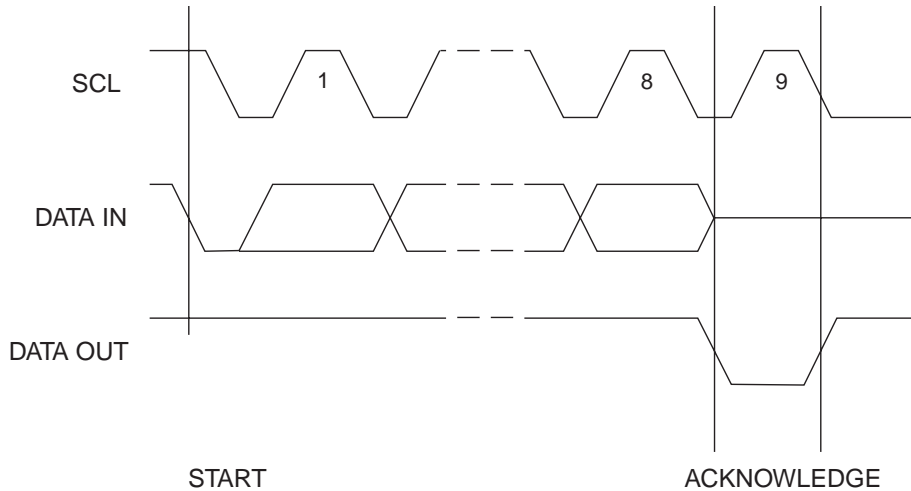


Figure 8. Output Acknowledge



6. Device Addressing

The 4K and 8K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to [Figure 9](#)).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

For the SOT23 Package Offering:

The 4K EEPROM software A2 and A1 bits in the device address word must be set to zero to properly communicate.

The 8K EEPROM software A2 bit in the device address word must be set to zero to properly communicate.

7. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see [Figure 10](#)).

PAGE WRITE: The 4K/8K EEPROM is capable of an 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition. (see [Figure 11](#)).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.



8. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see [Figure 12](#)).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 13](#)).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 14](#)).

Figure 9. Device Address

| | | | | | | | | |
|----|---|---|---|---|----------------|----------------|----|-----|
| 4K | 1 | 0 | 1 | 0 | A ₂ | A ₁ | P0 | R/W |
| 8K | 1 | 0 | 1 | 0 | A ₂ | P ₁ | P0 | R/W |

Figure 10. Byte Write

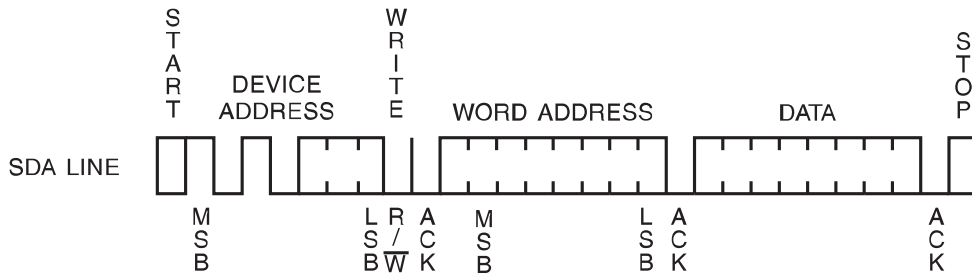


Figure 11. Page Write

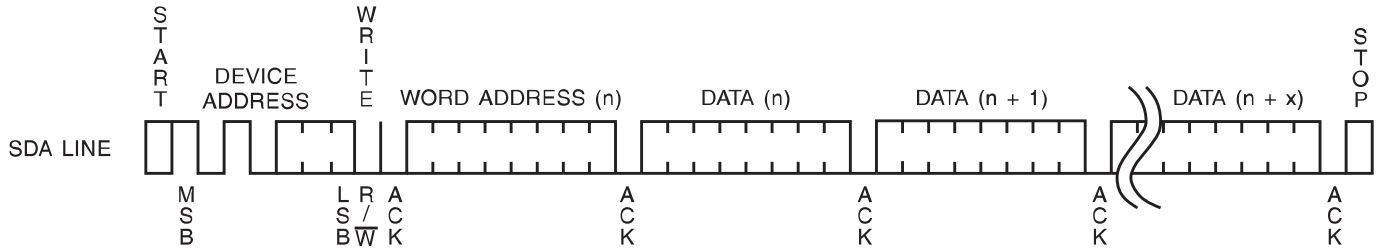


Figure 12. Current Address Read

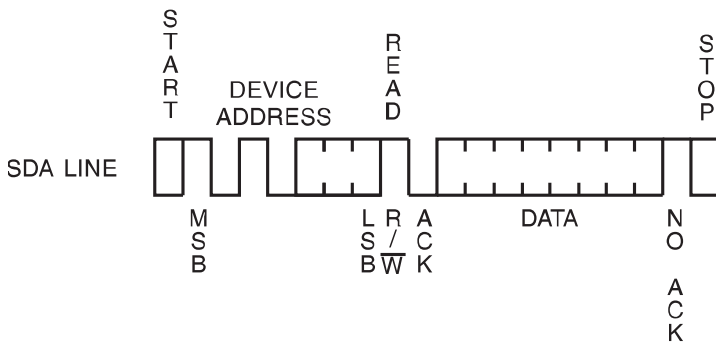


Figure 13. Random Read

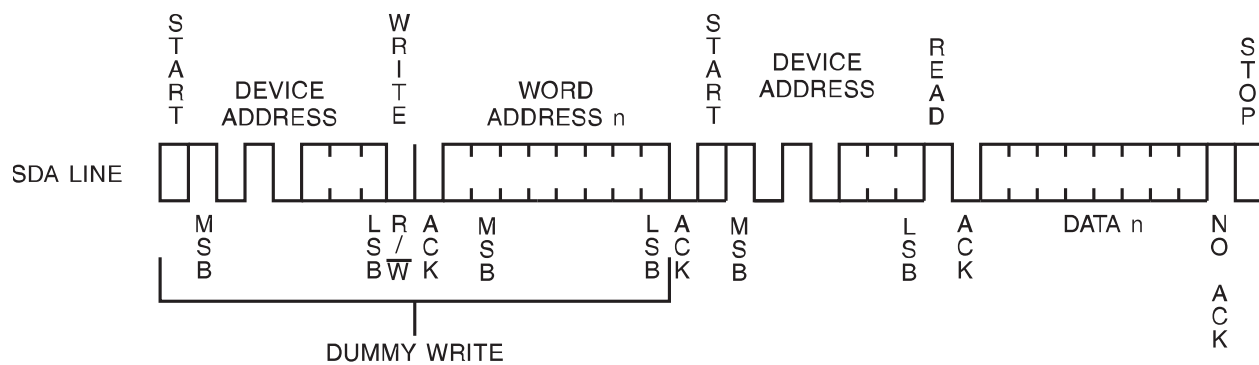
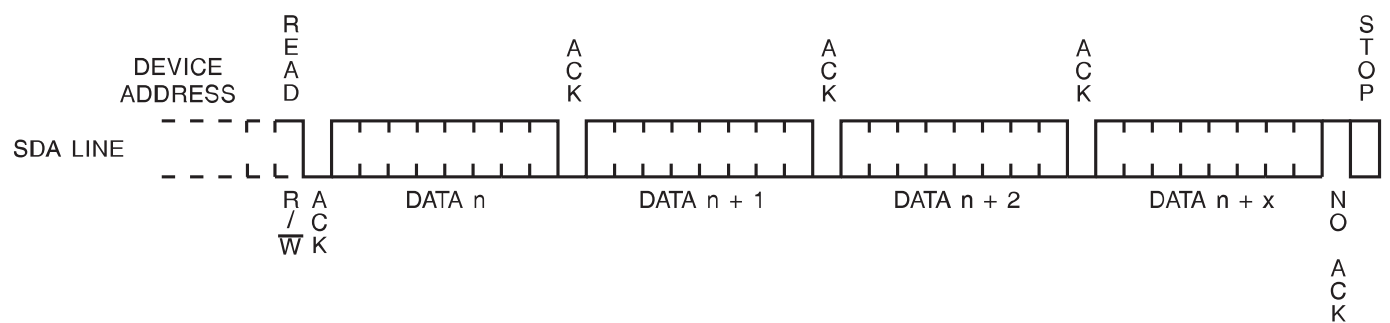


Figure 14. Sequential Read



9. AT24C04B Ordering Information

Table 5. Ordering Information

| Ordering Code | Voltage | Package | Operational range |
|---|---------|----------|--|
| AT24C04B-PU (Bulk form only) | 1.8 | 8P3 | Lead-free/Halogen-free/ Industrial Temperature (-40°C to 85°C) |
| AT24C04BN-SH-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C04BN-SH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C04B-TH-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C04B-TH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C04BY6-YH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8Y6 | |
| AT24C04B-TSU-T ⁽²⁾ | 1.8 | 5TS1 | |
| AT24C04BU3-UU-T ⁽²⁾ | 1.8 | 8U3-1 | Industrial Temperature (-40°C to 85°C) |
| AT24C04B-W-11 ⁽³⁾ | 1.8 | Die Sale | |

- Note:**
1. “-B” denotes bulk.
 2. “-T” denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP, SOT23, and dBG2 = 5K per reel.
 3. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Please contact Serial Interface Marketing.

| Package Type | |
|--------------|--|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8A2 | 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) |
| 8Y6 | 8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm) |
| 5TS1 | 5-lead, 2.90 mm x 1.60 mm Body, Plastic Thin Shrink Small Outline Package (SOT23) |
| 8U3-1 | 8-ball, die Ball Grid Array Package (dBG2) |
| Options | |
| -1.8 | Low-voltage (1.8V to 5.5V) |





10. AT24C08B Ordering Information

Table 6. Ordering Information

| Ordering Code | Voltage | Package | Operational range |
|---|---------|----------|--|
| AT24C08B-PU (Bulk form only) | 1.8 | 8P3 | Lead-free/Halogen-free/ Industrial Temperature (-40°C to 85°C) |
| AT24C08BN-SH-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C08BN-SH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8S1 | |
| AT24C08B-TH-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C08B-TH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8A2 | |
| AT24C08BY6-YH-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8 | 8Y6 | |
| AT24C08B-TSU-T ⁽²⁾ | 1.8 | 5TS1 | |
| AT24C08BU3-UU-T ⁽²⁾ | 1.8 | 8U3-1 | Industrial Temperature (-40°C to 85°C) |
| AT24C08B-W-11 ⁽³⁾ | 1.8 | Die Sale | |

- Note:**
1. “-B” denotes bulk.
 2. “-T” denotes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP, SOT23, and dBGa2 = 5K per reel.
 3. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Please contact Serial Interface Marketing.

| Package Type | |
|--------------|--|
| 8P3 | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 8A2 | 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) |
| 8Y6 | 8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm) |
| 5TS1 | 5-lead, 2.90 mm x 1.60 mm Body, Plastic Thin Shrink Small Outline Package (SOT23) |
| 8U3-1 | 8-ball, die Ball Grid Array Package (dBGa2) |
| Options | |
| -1.8 | Low-voltage (1.8V to 5.5V) |

11. Part Marketing Scheme

11.1. AT24C04B Device Package Marking

8-PDIP

Seal Year

| | |
|-----------------------------|-----------|
| Top Mark | Seal Week |
| | |
| --- --- --- --- --- --- --- | |
| A T M L U Y W W | |
| --- --- --- --- --- --- --- | |
| 0 4 B 1 | |
| * Lot Number | |
| --- --- --- --- --- --- --- | |
| | |
| Pin 1 Indicator (Dot) | |

| | |
|---------------|----------------|
| Y = SEAL YEAR | WW = SEAL WEEK |
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |
| | 02 = Week 2 |
| | 04 = Week 4 |
| | :: : :::: : |
| | :: : :::: :: |
| | 50 = Week 50 |
| | 52 = Week 52 |

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

8-SOIC

Seal Year

| | |
|-----------------------------|-----------|
| Top Mark | Seal Week |
| | |
| --- --- --- --- --- --- --- | |
| A T M L H Y W W | |
| --- --- --- --- --- --- --- | |
| 0 4 B 1 | |
| * Lot Number | |
| --- --- --- --- --- --- --- | |
| | |
| Pin 1 Indicator (Dot) | |

| | |
|---------------|----------------|
| Y = SEAL YEAR | WW = SEAL WEEK |
| 6: 2006 | 0: 2010 |
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| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |
| | 02 = Week 2 |
| | 04 = Week 4 |
| | :: : :::: : |
| | :: : :::: :: |
| | 50 = Week 50 |
| | 52 = Week 52 |

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

8-TSSOP

Top Mark

Pin 1 Indicator (Dot)

| |
|-----------------|
| |
| --- --- --- --- |
| * H Y W W |
| --- --- --- --- |
| 0 4 B 1 |
| --- --- --- --- |

| | |
|---------------|----------------|
| Y = SEAL YEAR | WW = SEAL WEEK |
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |
| | 02 = Week 2 |
| | 04 = Week 4 |
| | :: : :::: : |
| | :: : :::: :: |
| | 50 = Week 50 |
| | 52 = Week 52 |

Bottom Mark

| |
|-----------------------------|
| --- --- --- --- --- --- --- |
| P H |
| --- --- --- --- --- --- --- |
| A A A A A A A A |
| <- Pin 1 Indicator |





8-Ultra Thin Mini Map

Top Mark

```
|---|---|---|
  0   4   B
|---|---|---|
  H   1
|---|---|---|
  Y   X   X
|---|---|---|
  *
```

Pin 1 Indicator (Dot)

Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH
NSEB TRACE CODE LOG BOOK.
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR

| | | | |
|----|------|----|------|
| 6: | 2006 | 0: | 2010 |
| 7: | 2007 | 1: | 2011 |
| 8: | 2008 | 2: | 2012 |
| 9: | 2009 | 3: | 2013 |

ULA

Top Mark

```
|---|---|---|
  0   4   B
|---|---|---|
  Y   X   X
|---|---|---|
  *
```

Pin 1 Indicator (Dot)

Y = BUILD YEAR

| | | | |
|------|-----|------|-------|
| 2006 | = 6 | 2008 | = 8 |
| 2007 | = 7 | Etc. | . . . |

XX = ATMEL LOT NUMBER TO COORESPOND WITH
NSEB TRACE CODE LOG BOOK.

(e.g. XX = AA, AB, AC,...AX, AY, AZ)

SOT23

Top Mark

```

      |---|---|---|---|
Line 1 ----->  4   B   1   B   U
      |---|---|---|---|
                  *
                  |
  
```

XX = Device
 V = Voltage Indicator
 W = Write Protect Feature
 U = Material Set

Pin 1 Indicator (Dot)

Bottom Mark

```

      |---|---|---|---|
      Y   M   T   C
      |---|---|---|---|
  
```

Y = One Digit Year Code
 M = Seal Month
 (Use Alpha Designator A-L)
 TC = Trace Code

dBGA2

Top Mark

```

Line 1 ----->  04BU
Line 2 ----->  YMTC
                  | <--- Pin 1 This Corner
  
```

XXX = Device
 U = Material Set
 Y = One Digit Year Code
 M = Seal Month (Use Alpha Designator A-L)
 TC = Trace Code



11.2. AT24C08B Device Package Marking

dBGA2

Top Mark

```
Line 1 ----->    08BU
Line 2 ----->    YMXX
                |<--- Pin 1 This Corner
```

Y = ONE DIGIT YEAR CODE

| | |
|---------|---------|
| 8: 2008 | 1: 2011 |
| 9: 2009 | 2: 2012 |
| 0: 2010 | 3: 2013 |

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)

A = JANUARY
B = FEBRUARY
" " " " " " " " " "
J = OCTOBER
K = NOVEMBER
L = DECEMBER

XX = TRACE CODE (ATMEL LOT NUMBERS TO CORRESPOND WITH ATK TRACE CODE LOG BOOK)

8-Ultra Thin Mini MAP

Top Mark

```
|---|---|---|
  0  8  B
|---|---|---|
  H  1
|---|---|---|
  Y  X  X
|---|---|---|
  *
  |
  Pin 1 Indicator (Dot)
```

Y = YEAR OF ASSEMBLY

XX = TRACE ATMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK.
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR

| | |
|---------|---------|
| 6: 2006 | 0: 2010 |
| 7: 2007 | 1: 2011 |
| 8: 2008 | 2: 2012 |
| 9: 2009 | 3: 2013 |

8-PDIP and 8-SOIC

Seal Year

```

Top Mark          | Seal Week
                  | | |
|---|---|---|---|---|---|---|
  A   T   M   L   H   Y   W   W
|---|---|---|---|---|---|---|
  0   8   B       1
  *   Lot Number
|---|---|---|---|---|---|---|
  |
Pin 1 Indicator (Dot)

Y = SEAL YEAR      WW = SEAL WEEK
8:  2008           2:  2012           02 = Week 2
9:  2009           3:  2013           04 = Week 4
0:  2010           4:  2014           :: : :::: :
1:  2011           5:  2015           :: : :::: :
                                   50 = Week 50
                                   52 = Week 52

```

SOT23

```

Top Mark
Line 1 -----> |---|---|---|---|
                  8   B   1   B   U
                  |---|---|---|---|
                  *
                  |
Pin 1 Indicator (Dot)

```

BACKSIDE MARKING

```

|---|---|---|---|
  Y   M   X   X
|---|---|---|---|

```

Y = ONE DIGIT YEAR CODE

```

4:  2004           7:  2007
5:  2005           8:  2008
6:  2006           9:  2009

```

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)

```

A = JANUARY
B = FEBRUARY
" " " " " " " "
J = OCTOBER
K = NOVEMBER
L = DECEMBER

```

XX = TRACE CODE (ATMEL LOT NUMBERS TO CORRESPOND WITH TRACE CODE LOG BOOK)



8-TSSOP

Pin 1 Indicator (Dot)

```
|
|---|---|---|---|
*   H   Y   W   W
|---|---|---|---|
0   8   B       1
|---|---|---|---|
```

Bottom Mark

```
|---|---|---|---|---|---|
C   O   O
|---|---|---|---|---|---|
A   A   A   A   A   A   A
<- Pin 1 Indicator
```

COO = Country of Origin

Y = SEAL YEAR

| | | | |
|----|------|----|------|
| 6: | 2006 | 0: | 2010 |
| 7: | 2007 | 1: | 2011 |
| 8: | 2008 | 2: | 2012 |
| 9: | 2009 | 3: | 2013 |

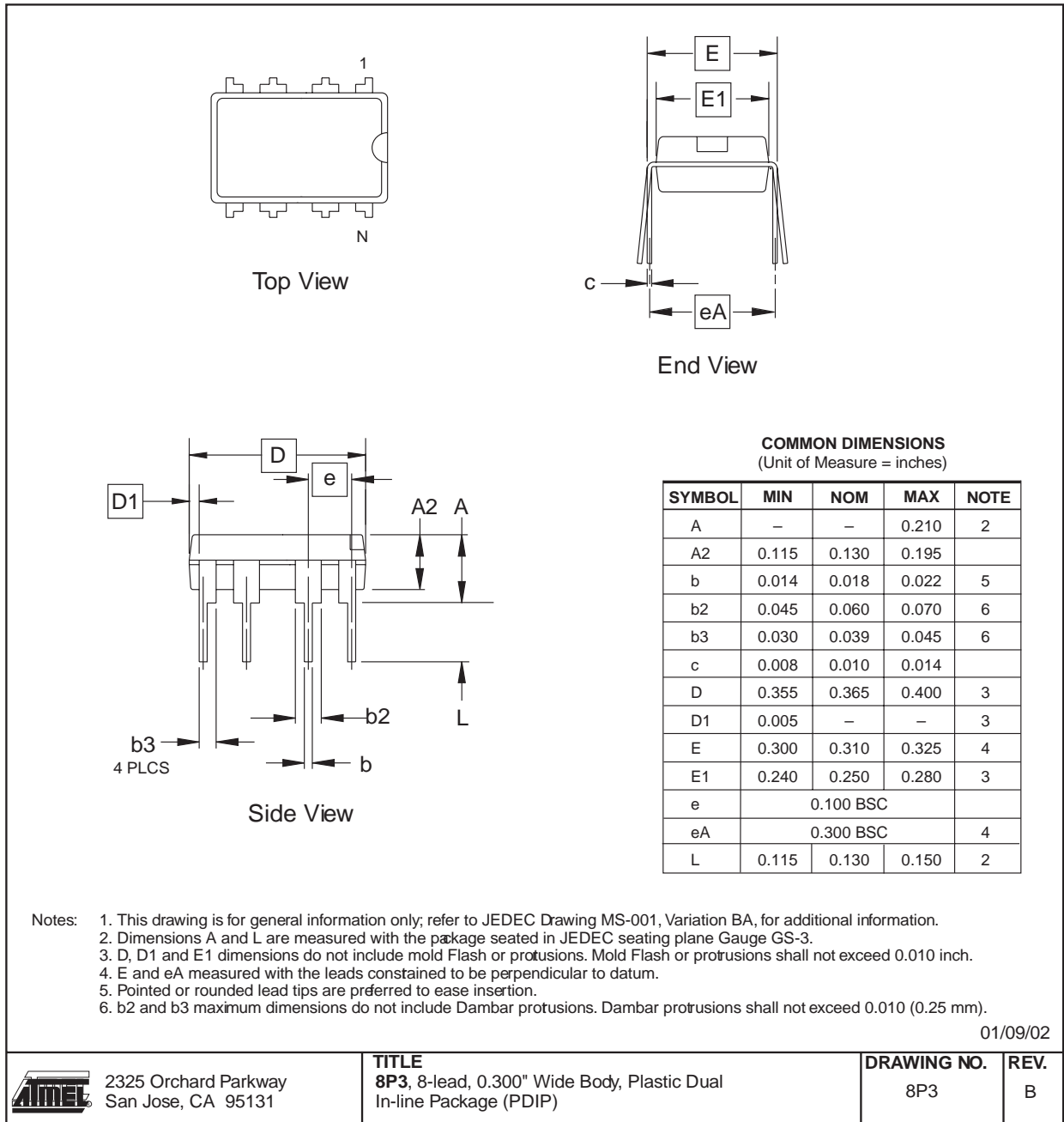
WW = SEAL WEEK

| | |
|----------|---------|
| 02 = | Week 2 |
| 04 = | Week 4 |
| :: : ::: | : |
| :: : ::: | :: |
| 50 = | Week 50 |
| 52 = | Week 52 |

12. Packaging Information

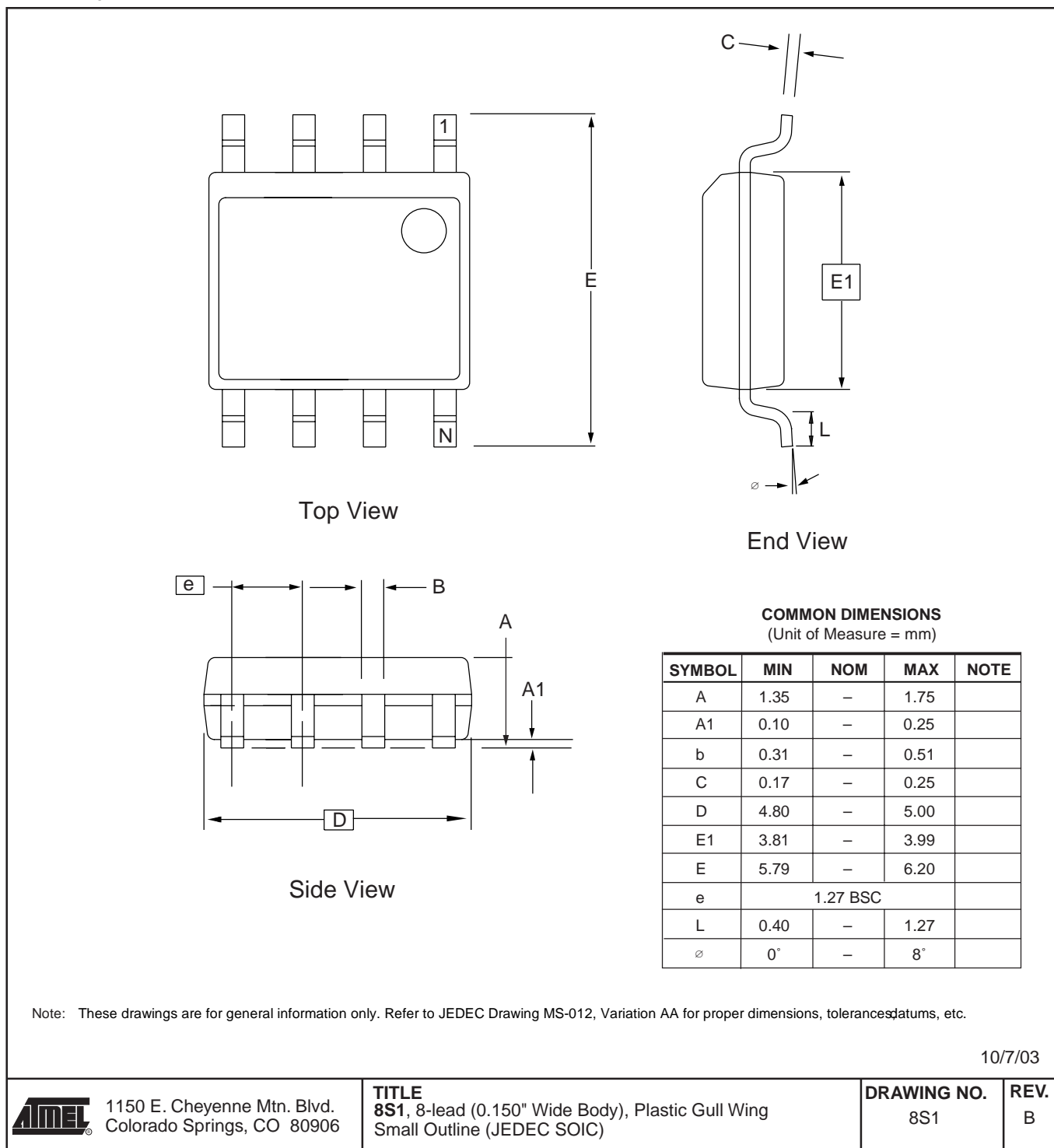
8P3 – PDIP

Figure 15. 8P3 – PDIP



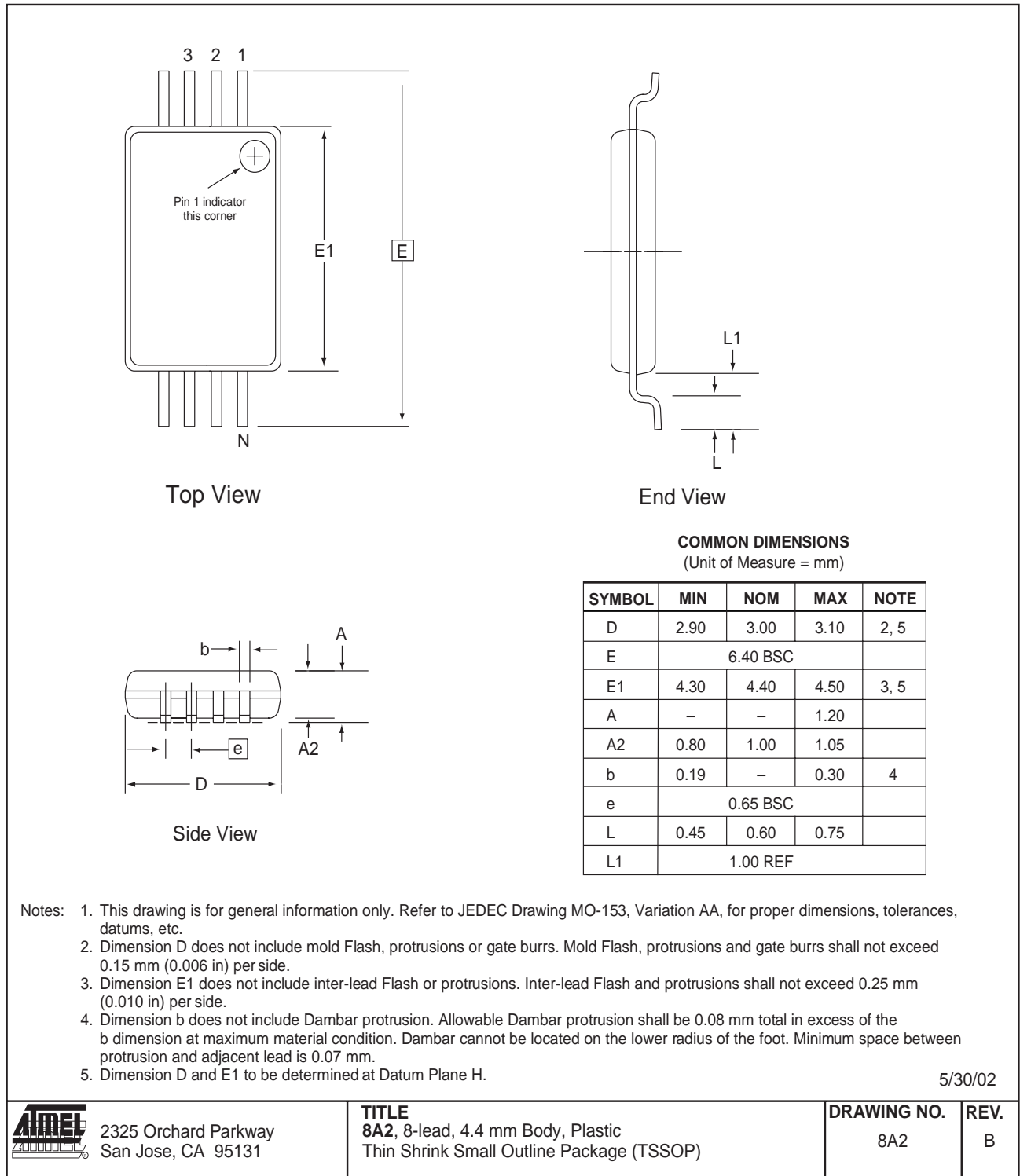
8S1 – JEDEC SOIC

Figure 16. 8S1 – JEDEC SOIC



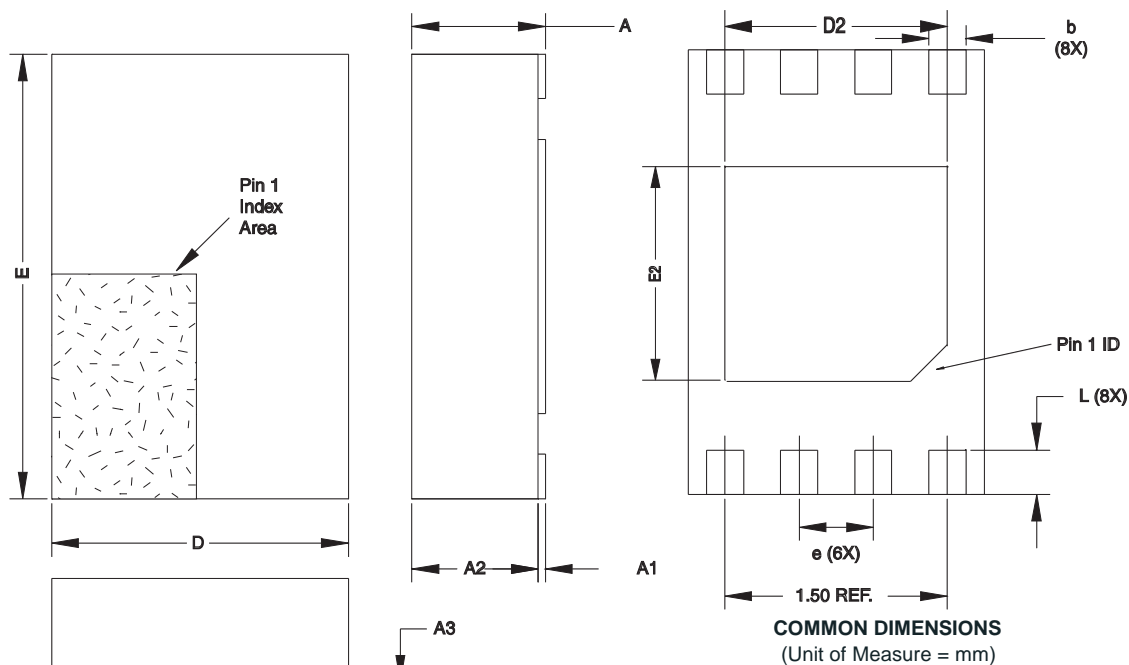
8A2 – TSSOP

Figure 17. 8A2 – TSSOP



8Y6 – Mini Map

Figure 18. 8Y6 – Mini Map



| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------|----------|------|------|
| D | | 2.00 BSC | | |
| E | | 3.00 BSC | | |
| D2 | 1.40 | 1.50 | 1.60 | |
| E2 | - | - | 1.40 | |
| A | - | - | 0.60 | |
| A1 | 0.0 | 0.02 | 0.05 | |
| A2 | - | - | 0.55 | |
| A3 | | 0.20 REF | | |
| L | 0.20 | 0.30 | 0.40 | |
| e | | 0.50 BSC | | |
| b | 0.20 | 0.25 | 0.30 | 2 |

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
 2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
 3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

10/16/07



2325 Orchard Parkway
San Jose, CA 95131

TITLE

8Y6, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Ultra Thin Mini-Map,
Dual No Lead Package (DFN) ,(MLP 2x3)

DRAWING NO.

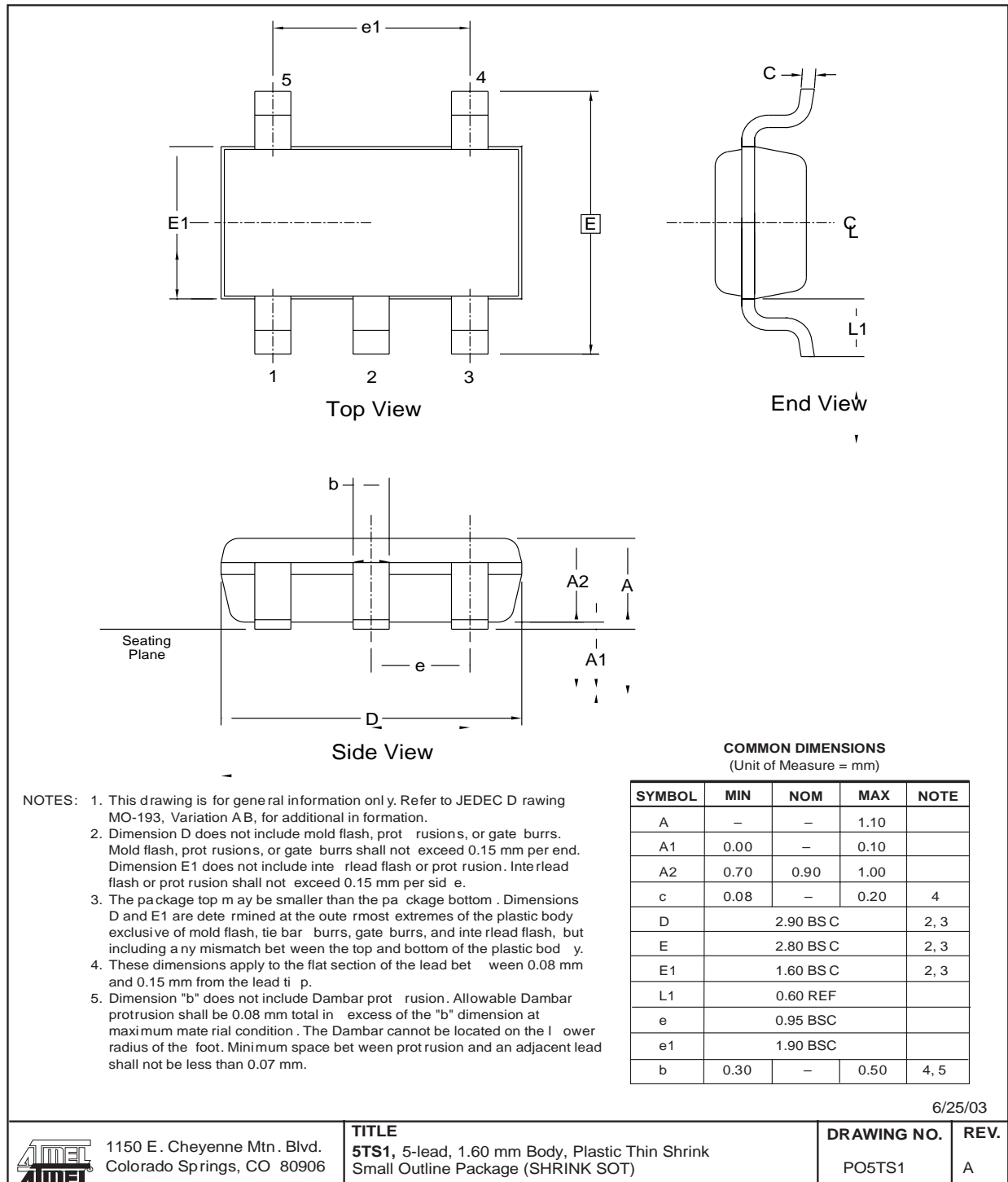
8Y6

REV.

D

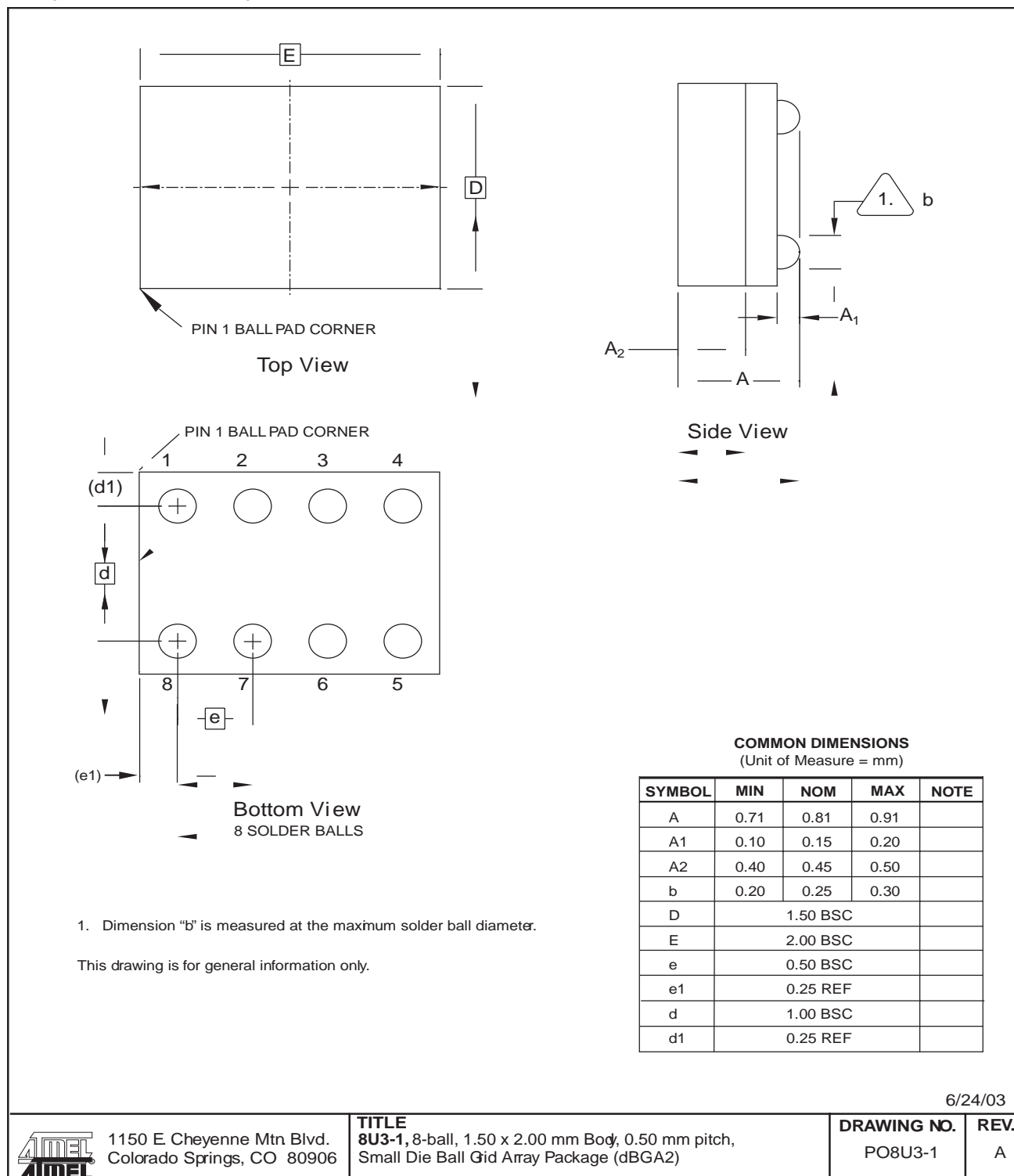
5TS1 – SOT23

Figure 19. 5TS1 – SOT23



8U3-1 – Dbga2

Figure 20. 8U3-1 – Dbga2



13. Revision History

Table 7. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|---|
| 5226G | 07/2012 | Not recommended for new design. Use AT24C04C/08C. |
| 5226G | 11/2009 | Corrected AC Characteristics, T_{AA} minimum value from 0.55 to 0.05 |
| 5226F | 5/2009 | Corrected AT24C08B Part Marking Scheme |
| 5226E | 12/2008 | Add AT24C08B Device Package Marking Details and removed Bumped wafer offering. |
| 5226D | 08/2008 | Update into MS Format. |
| 5226D | 07/2008 | Removed 'Preliminary' status |
| 5226C | 02/2008 | Text changes on page 4 and 9 |
| 5226B | 08/2007 | Updated to new template Updated common Figures Added Package Marking tables |
| 5226A | 06/2007 | Initial document release |





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