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JTAG-HS3™ Programming Cable for Xilinx® FPGAs

Revised March 13, 2019
This manual applies to the JTAG-HS3 rev. A

Overview

The JTAG-HS3 programming cable is a high-speed programming/debugging solution for Xilinx FPGAs and SoCs. It is fully compatible will all Xilinx Tools, and can be seamlessly driven from iMPACT, ChipScope™, EDK, and Vivado™. The HS3 attaches to target boards using Xilinx's 2x7, 2mm programming header.

The PC powers the JTAG-HS3 through the USB port and will recognize it as a Digilent programming cable when connected, even if the cable is not attached to the target board. The HS3 has a separate Vref pin to supply the JTAG signal buffers. The high speed 24mA three-state buffers allow the HS3 to drive target boards with signal voltages from 1.8V to 5V and bus speeds up to 30MBit/sec (see Fig. 1). To function correctly, the HS3's Vref pin must be tied to the same voltage supply (VCCO_0) that drives the JTAG port on the FPGA.

The JTAG-HS3

Features include:

- Small, complete, all-in-one JTAG programming/debugging solution for Xilinx FPGAs and SoCs
- Plugs directly into standard Xilinx JTAG header
- Separate Vref drives JTAG signal voltages; Vref can be any voltage between 1.8V and 5V
- High-Speed USB2 port that can drive JTAG bus up to 30Mbit/sec (frequency adjustable by user)
- Compatible with Xilinx ISE® 14.1 and newer, Xilinx Vivado 2013.3 and newer
- Uses micro_AB USB2 connector
- Open drain buffer on pin 14 allows debugging software to reset the processor core of Xilinx's Zynq® platform

The JTAG bus can be shared with other devices as the HS3 signals are held in high-impedance, except when actively driven during programming. The HS3 uses a standard Type-A to Micro-USB cable that attaches to the end of the module opposite the system board connector. The HS3 is small and light, allowing it to be held firmly in place by the system board connector (see Fig. 2).

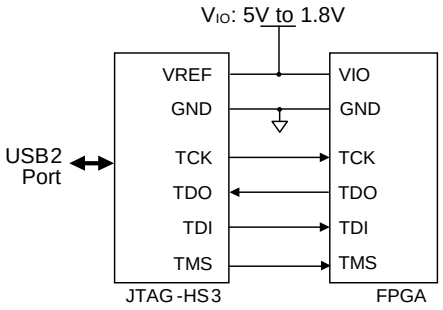

Figure 1. Diagram of signal voltages and connections.

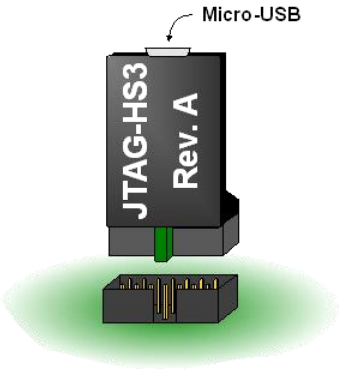

Figure 2. Xilinx JTAG header. Dual row, 2mm, 14 pin.

1 Software Support

The JTAG-HS3 has been designed to work seamlessly with Xilinx's ISE (iMPACT, ChipScope, EDK) and Vivado tool suites. The most recent versions of ISE and Vivado include all of the drivers, libraries, and plugins necessary to communicate with the JTAG-HS3. At the time of writing, the following Xilinx software included support for the HS3: Vivado 2014.1+, Vivado 2013.3+, and ISE 14.1+.

The HS3 is also compatible with ISE 13.1 – 13.4. However, these versions of ISE do not include all of the libraries, drivers, and plugins necessary to communicate with the HS3. In order to use the JTAG-HS3 with these versions of ISE, version 2.5.2 or higher of the Digilent Plugin for Xilinx Tools package must be downloaded from the Digilent website, and the ISE13 plugin must be manually installed as described in the included documentation. The JTAG-HS3 is not compatible with Xilinx Vivado 2013.1 or Vivado 2013.2.

In addition to working with the Xilinx Tools, the HS3 is also supported by Digilent's Adept software and the Adept SDK (the SDK is available to download free from Digilent's website). Adept includes a full-featured programming environment and a set of public APIs that allow user applications to directly drive the JTAG chain. Using the Adept SDK, custom applications can be created to drive JTAG ports on virtually any device. Please see the Adept SDK reference manual for more information.

2 Xilinx Zynq-7000 and SoC Support

The Xilinx Tools occasionally require the processor core of the Zynq-7000 to be reset during debug operations. The Zynq platform processor has a pin dedicated for this purpose (PS_SRST_B). Driving the PS_SRST_B pin low causes the processor to reset while maintaining any existing break points and watch points. The JTAG-HS3 is capable of driving this pin low under the instruction of Xilinx's SDK during debugging operations. In order for this to work, pin 14 of Xilinx JTAG header on the target board must be connected to the PS_SRST_B pin of the Zynq (see Figs. 3 & 4).

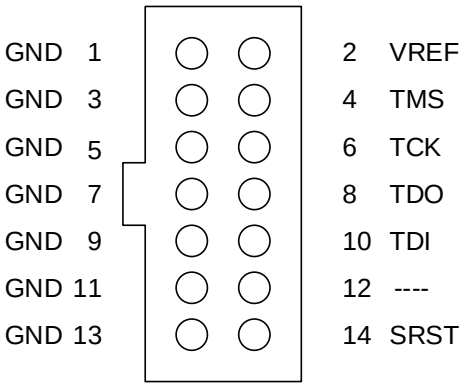

Figure 3. JTAG-HS3 pinout (seen looking out of the connector).

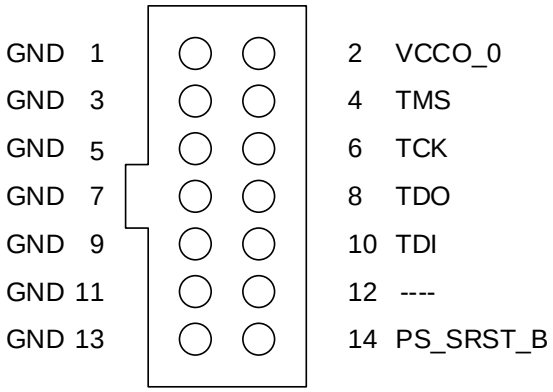

Figure 4. Xilinx System Board Header (seen looking into the connector).

The JTAG-HS3 uses an open drain buffer to drive pin 14 of the Xilinx JTAG header (see Fig. 5). This allows the HS3 to drive the PS_SRST_B pin when VCC_MIO1 is referenced to a different voltage than VCCO_0 (see Fig. 6).

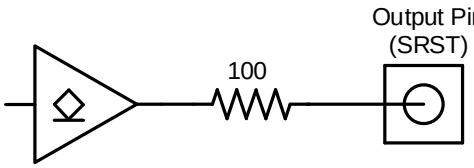

Figure 5. JTAG-HS3 pin 14 output buffer.

Should an accidental short occur between pin 14 and GND, the 100 ohm series resistor protects the buffer from being damaged. While this resistor protects the buffer from being damaged, it also limits the drive strength of the buffer. Therefore, it is necessary for the pull-up resistor (R_{PU}) used to establish the voltage level on PS_SRST_B to be greater than or equal to 1.5K ohms. At the time of writing, Xilinx ZC702, Xilinx ZC706, and Avnet® MicroZed™ all feature 10K pull-ups on pin 14 of the their respective Xilinx JTAG headers. For compatibility with other evaluation platforms, please consult the manufacturer's schematic.

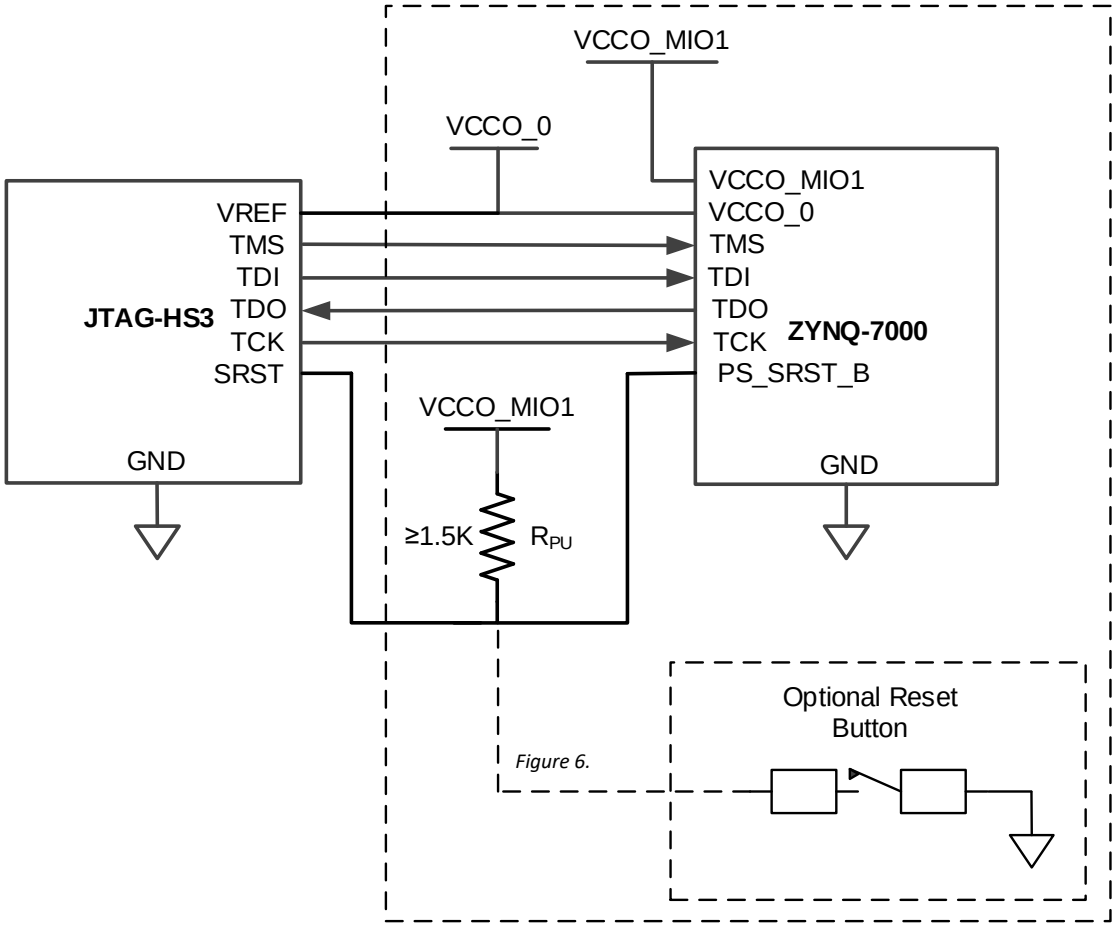

Figure 6.

Figure 6. System board components.

3 Supported Target Devices

The JTAG-HS3 is capable of targeting the following Xilinx devices:

- Xilinx FPGAs
- Xilinx Zynq-7000
- Xilinx CoolRunner™/CoolRunner-II CPLDs
- Xilinx Platform Flash ISP configuration PROMs
- Select third-party SPI PROMs
- Select third-party BPI PROMs

The following devices cannot be targeted by the JTAG-HS3:

- Xilinx 9500/9500XL CPLDs
- Xilinx 1700 and 18V00 ISP configuration PROMs
- Xilinx FPGA eFUSE programming

Remote device configuration is not supported for the JTAG-HS3 when used with Xilinx's iMPACT software.

Note: Please see the "Introduction to Indirect Programming – SPI or BPI Flash Memory" help topic in iMPACT for a list of supported FPGA/PROM combinations.

Note: Please see the "Configuration Memory Support" section of Xilinx UG908 for a list of the FPGA/PROM combinations that Vivado supports.

4 Design Notes

The JTAG-HS3 uses high speed three-state buffers to drive the TMS, TDI, and TCK signals. These buffers are capable of sourcing or sinking a maximum of 50 mA of current. The HS3 has 100 ohm resistors between the output of the buffers and the I/O pins to ensure the cable does not exceed the maximum limit. To further limit short circuit, additional current resistance may be placed in series with the I/O pins of the HS3 and the target board. However, Digilent recommends limiting the amount of additional resistance to 100 ohms or less as higher resistance may result in degraded operation.

5 Programming Solutions Comparison Chart

	 JTAG-USB	 JTAG-HS1	 JTAG-HS2	 JTAG-HS3
Max Speed	1.6 MHz	30 MHz	30 MHz	30 MHz
Voltage Range	1.8V – 5V	1.8V – 5V	1.8V – 5V	1.8V – 5V
Xilinx Native Support	ISE 13.2+ Vivado 2014.2+	ISE 13.2+ Vivado 2012.1+	ISE 13.2+ Vivado 2012.1+	ISE 14.1+ Vivado 2013.3+
Xilinx Plug-in Support	ISE 12.1+	ISE 12.1+	ISE 12.1+	ISE 12.1+
Digilent Adept Support	YES	YES	YES	YES
PC Interface	USB	USB	USB	USB
Connector Interface	6-pin	6-pin, 14-pin	6-pin, 14-pin	14-pin
4-Wire JTAG	YES	YES	YES	YES
2-Wire JTAG	NO	NO	YES	NO
Zynq-7000 PS_SRST Support	NO	NO	NO	YES
SPI Support	YES	YES	YES	NO

6 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
Vref	I/O reference/supply voltage		-0.5	6	V
VIO	Signal Voltage		-0.5	6	V
I_{IK},I_{OK}	TMS, TCK, TDI, TDO DC Input/Output Diode Current	VIO < -0.5V		-50	mA
		VIO > 6V		+20	
I_{OUT}	DC Output Current			±50	mA
T_{STG}	Storage Temperature		-20	+120	ºC
ESD	Human Body Model JESD22-A114			2000	V
	Charge Device Model JESD22-C101			500	V

7 DC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vref	I/O reference/supply voltage	1.65	1.8/2.5/3.3	5.5	Volts
TDO	Input High Voltage (V_{IH})	1.4		5.5	Volts
	Input Low Voltage (V_{IL})	0		0.45	Volts
TMS, TCK, TDI	Output High (V_{OH})	0.75 x Vref	0.90 x Vref	Vref	Volts
	Output Low (V_{OL})	0	0.05 x Vref	0.15 x Vref	Volts
SRST	Output Low (V_{OL}) (R_{PU} = 1.5K ohm)	0	0.4	0.55	Volts
T_A	Operating Temperature	0		70	ºC

8 AC Operating Characteristics

The JTAG-HS3 JTAG signals operate according to the timing diagram in Fig. 7. The HS3 supports TCK frequencies from 30 MHz to 8 KHz at integer divisions of 30 MHz from 1 to 3750. Common frequencies include 30 MHz, 15 MHz, 10 MHz, 7.5 MHz, and 6 MHz (see Table 4).

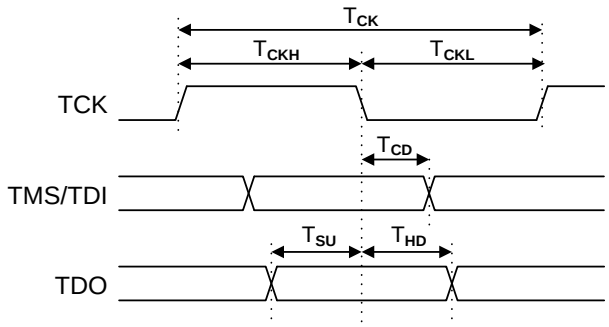

Figure 7. Timing diagram.

Symbol	Parameter	Min	Max
T_{CK}	T_{CK} period	33ns	125µs
T_{CKH}, T_{CKL}	T_{CLK} pulse width	16.6ns	62.5µs
T_{CD}	T_{CLK} to TMS, TDI	0	15ns
T_{SU}	TDO Setup time	19ns	
T_{HD}	TDO Hold time	0	

Table 4. JTAG-HS3 Frequency support.

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