

N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	20	0.390 at V _{GS} = 4.5 V	0.7	0.55
		0.510 at V _{GS} = 2.7 V	0.5	
		0.578 at V _{GS} = 2.5 V	0.5	
P-Channel	- 20	0.850 at V _{GS} = - 4.5 V	- 0.5	0.95
		1.35 at V _{GS} = - 2.7 V	- 0.5	
		1.48 at V _{GS} = - 2.5 V	- 0.3	

FEATURES

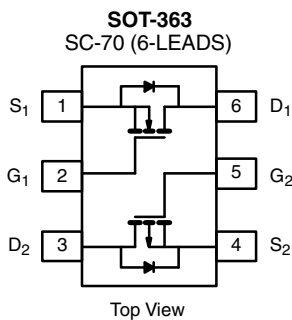
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



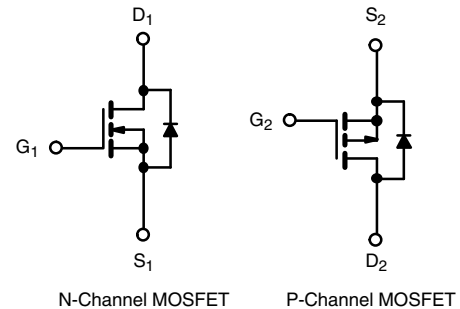
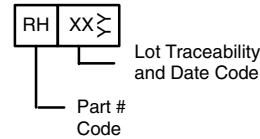
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch
- DC/DC Converter



Marking Code



Ordering Information: Si1553CDL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	20	- 20	V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	0.7	- 0.5	A
		T _C = 70 °C	0.6	- 0.4	
		T _A = 25 °C	0.7 ^{b, c}	- 0.4 ^{b, c}	
		T _A = 70 °C	0.5 ^{b, c}	- 0.4 ^{b, c}	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	0.3	- 0.3	A
		T _A = 25 °C	0.2 ^{b, c}	- 0.2 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	2	- 1	W	
Maximum Power Dissipation	P _D	T _C = 25 °C	0.34	0.34	W
		T _C = 70 °C	0.22	0.22	
		T _A = 25 °C	0.29 ^{b, c}	0.29 ^{b, c}	
		T _A = 70 °C	0.18 ^{b, c}	0.18 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	365	438	365	438	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	308	370	308	370	

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under steady state conditions is 486 °C/W (N-Channel) and 486 °C/W (P-Channel).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	20			V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-20				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		24		mV/ $^\circ\text{C}$	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-13			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-1.8			
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		2.3			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch			± 100	nA	
			P-Ch			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10		
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 5\text{ V}$	N-Ch	2			A	
		$V_{DS} = -5\text{ V}, V_{GS} = -5\text{ V}$	P-Ch	-1				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}$	N-Ch		0.325	0.390	Ω	
		$V_{GS} = -4.5\text{ V}, I_D = -0.4\text{ A}$	P-Ch		0.708	0.850		
		$V_{GS} = 2.7\text{ V}, I_D = 0.4\text{ A}$	N-Ch		0.425	0.510		
		$V_{GS} = -2.7\text{ V}, I_D = -0.2\text{ A}$	P-Ch		1.13	1.35		
		$V_{GS} = 2.5\text{ V}, I_D = 0.4\text{ A}$	N-Ch		0.462	0.578		
		$V_{GS} = -2.5\text{ V}, I_D = -0.2\text{ A}$	P-Ch		1.23	1.48		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 0.7\text{ A}$	N-Ch		1.5		S	
		$V_{DS} = -15\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.8			
Dynamic^a								
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		38		pF	
			P-Ch		43			
Output Capacitance	C_{oss}		P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		14		
				P-Ch		16		
Reverse Transfer Capacitance	C_{rss}			N-Ch		6		
				P-Ch		10		
Total Gate Charge	Q_g		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 0.7\text{ A}$	N-Ch		1.2	1.8	nC
				P-Ch		1.9	3	
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$	N-Ch		0.55	1.1		
			P-Ch		0.95	1.5		
Gate-Source Charge	Q_{gs}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -0.4\text{ A}$	N-Ch		0.15			
			P-Ch		0.25			
Gate-Drain Charge	Q_{gd}			N-Ch		0.15		
				P-Ch		0.25		
Gate Resistance	R_g	$f = 1\text{ MHz}$		N-Ch	1.5	7.2	14.4	Ω
				P-Ch	2.1	10.3	20.6	



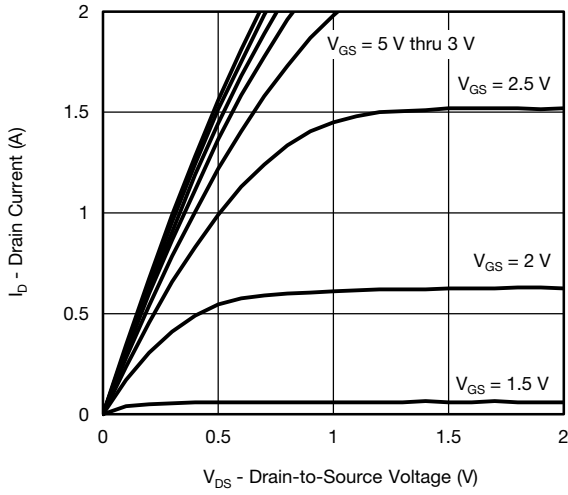
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 20\ \Omega$ $I_D \cong 0.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$ P-Channel $V_{DD} = -10\text{ V}, R_L = 25\ \Omega$ $I_D \cong -0.4\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$	N-Ch		2	4	ns
			P-Ch		2	4	
Rise Time	t_r		N-Ch		14	21	
			P-Ch		9	18	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		11	20	
			P-Ch		10	20	
Fall Time	t_f		N-Ch		7	14	
			P-Ch		7	14	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 20\ \Omega$ $I_D \cong 0.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$ P-Channel $V_{DD} = -10\text{ V}, R_L = 25\ \Omega$ $I_D \cong -0.4\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\ \Omega$	N-Ch		16	24	
			P-Ch		15	23	
Rise Time	t_r		N-Ch		22	33	
			P-Ch		15	23	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		22	33	
			P-Ch		12	20	
Fall Time	t_f		N-Ch		13	20	
			P-Ch		8	16	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			0.3	A
			P-Ch			-0.3	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			2	
			P-Ch			-1	
Body Diode Voltage	V_{SD}	$I_S = 0.5\text{ A}$ $I_S = -0.4\text{ A}$	N-Ch		0.8	1.2	V
			P-Ch		-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 0.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ P-Channel $I_F = -0.4\text{ A}, dI/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch		8	15	ns
P-Ch			12	20			
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		1	2	nC
			P-Ch		5	10	
Reverse Recovery Fall Time	t_a		N-Ch		4		ns
			P-Ch		9		
Reverse Recovery Rise Time	t_b		N-Ch		4		
			P-Ch		3		

Notes:

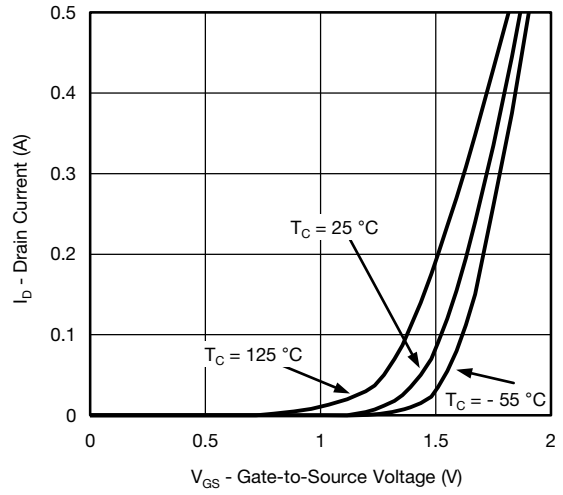
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

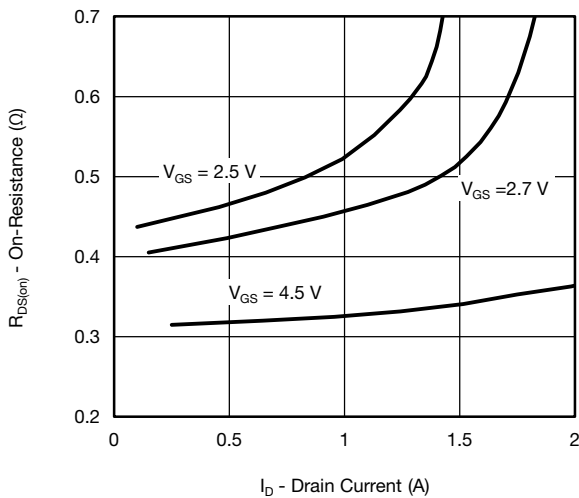
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



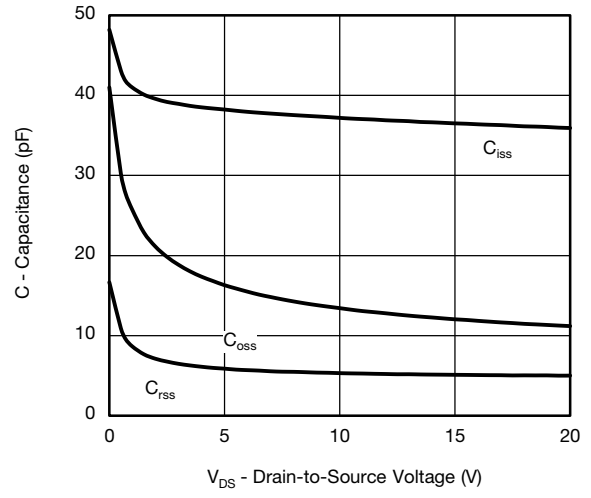
Output Characteristics



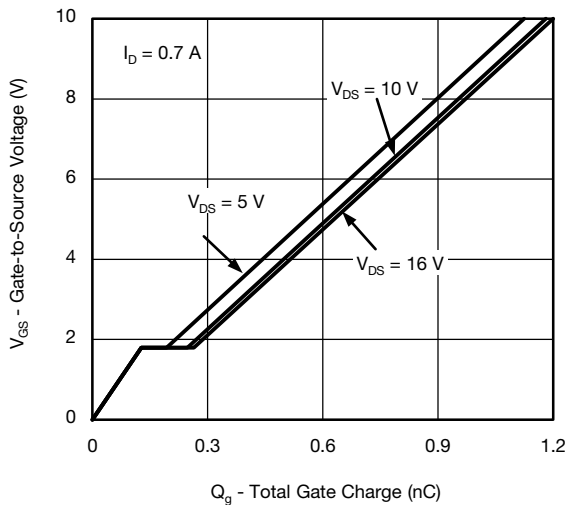
Transfer Characteristics



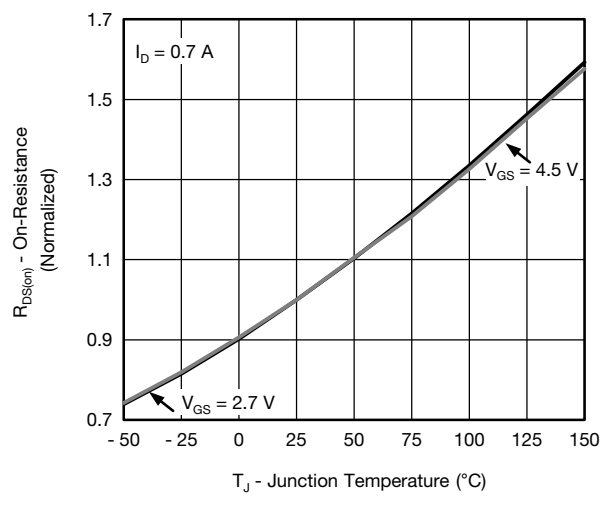
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

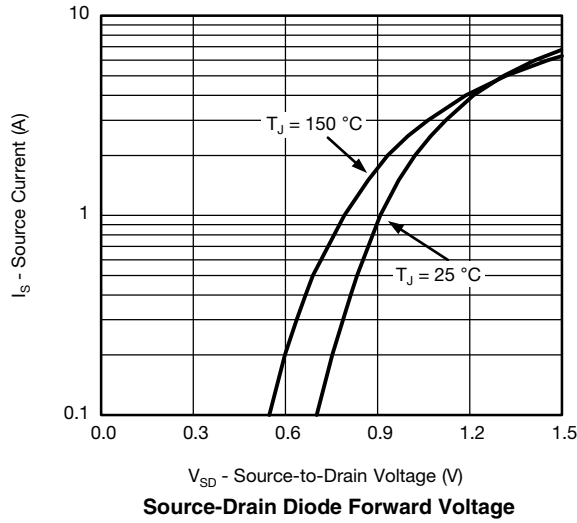


Gate Charge

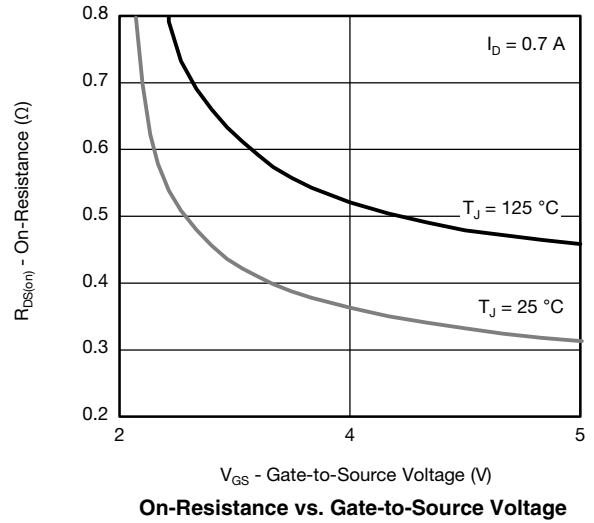


On-Resistance vs. Junction Temperature

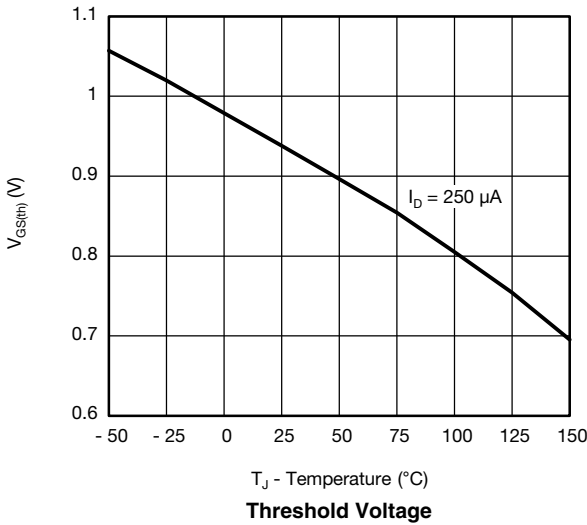
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



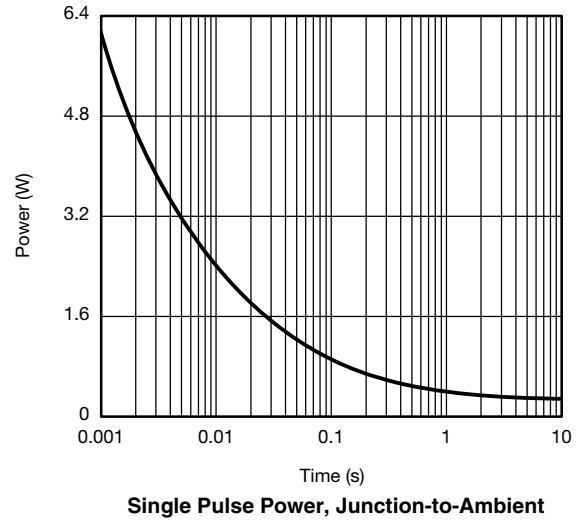
Source-Drain Diode Forward Voltage



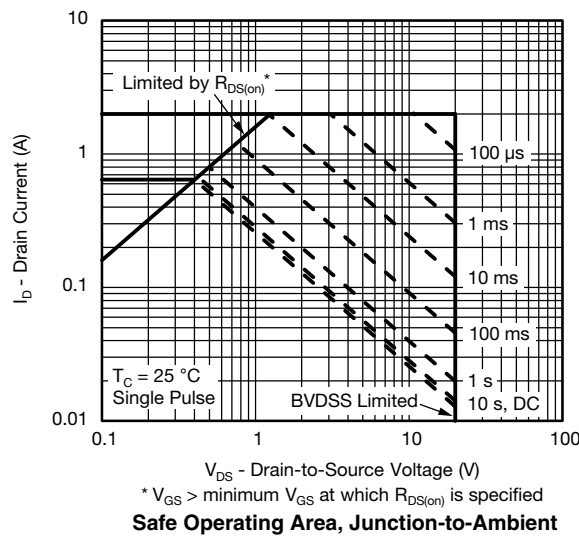
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

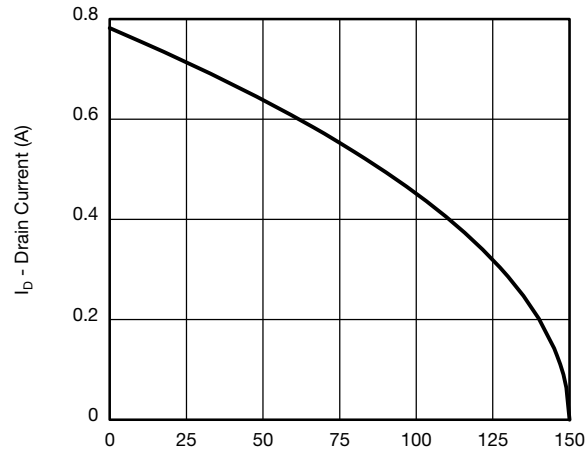


Single Pulse Power, Junction-to-Ambient



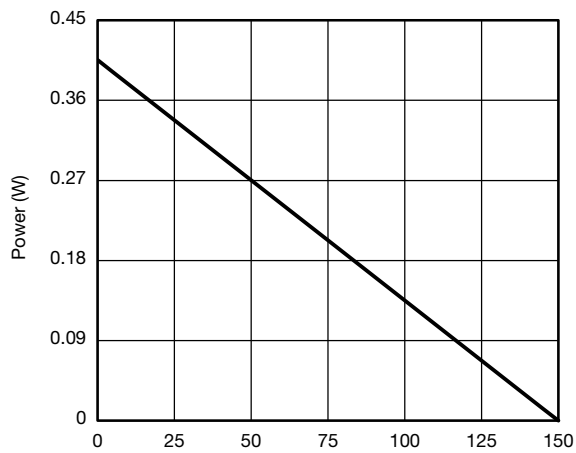
Safe Operating Area, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



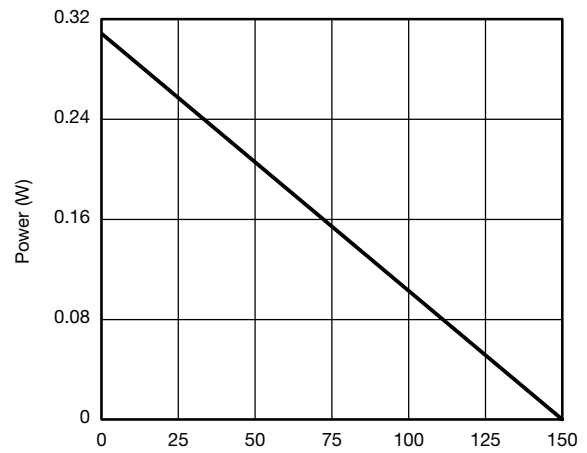
T_C - Case Temperature (°C)

Current Derating*



T_C - Case Temperature (°C)

Power Derating, Junction-to-Foot

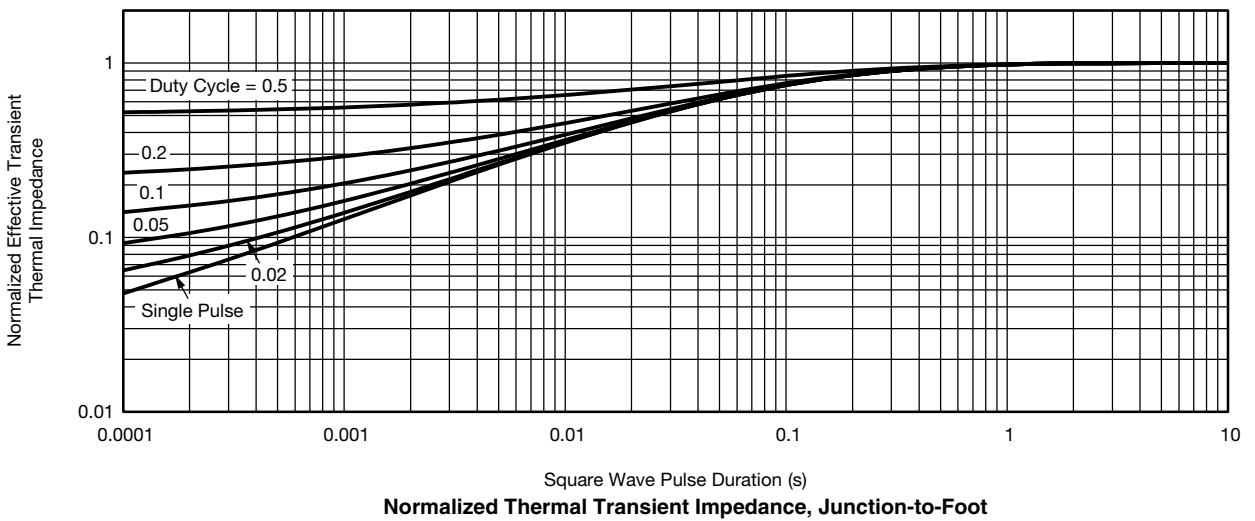
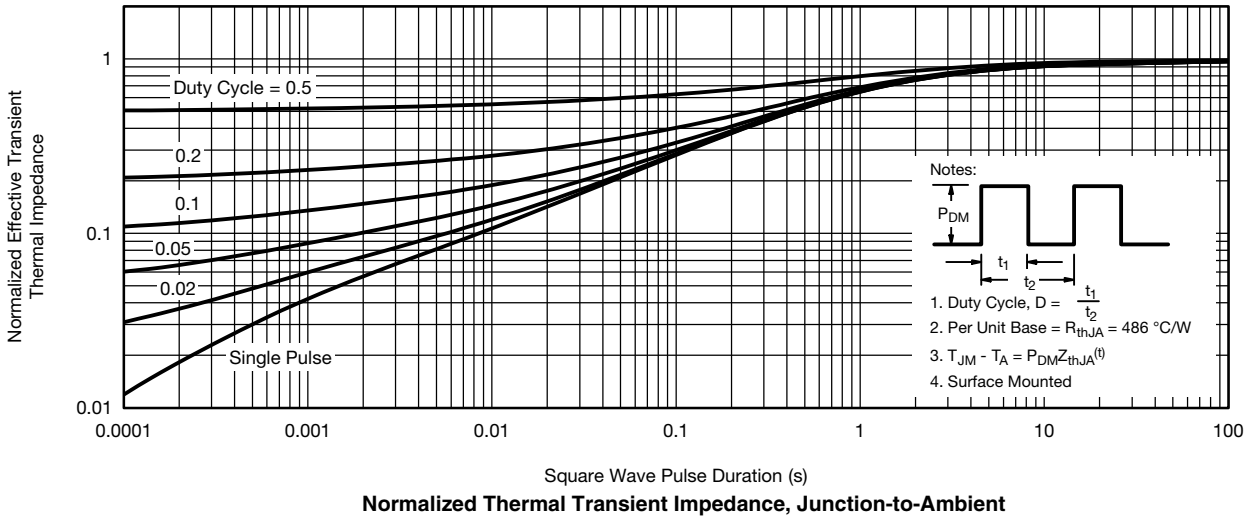


T_A - Ambient Temperature (°C)

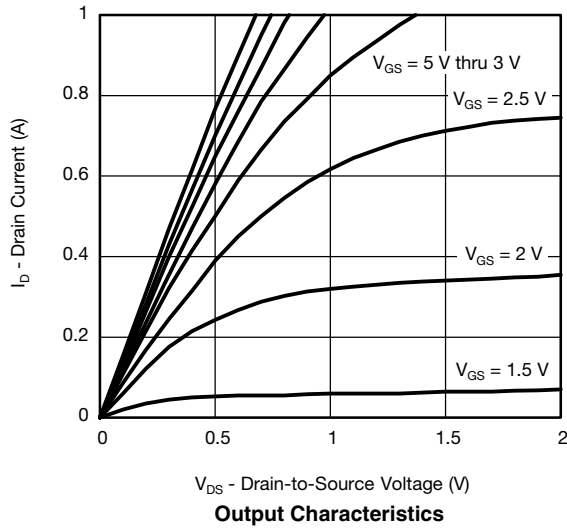
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

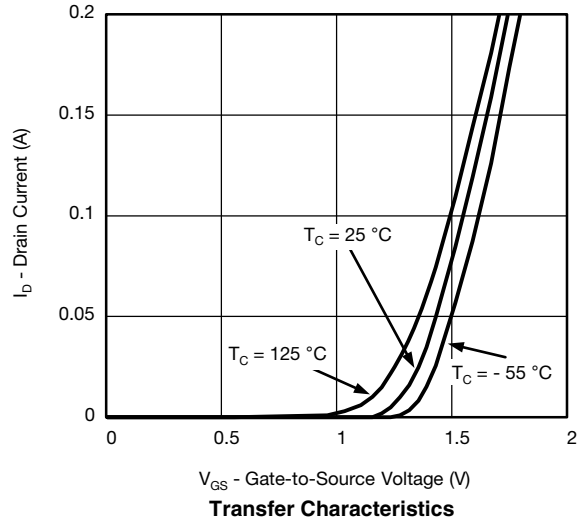
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



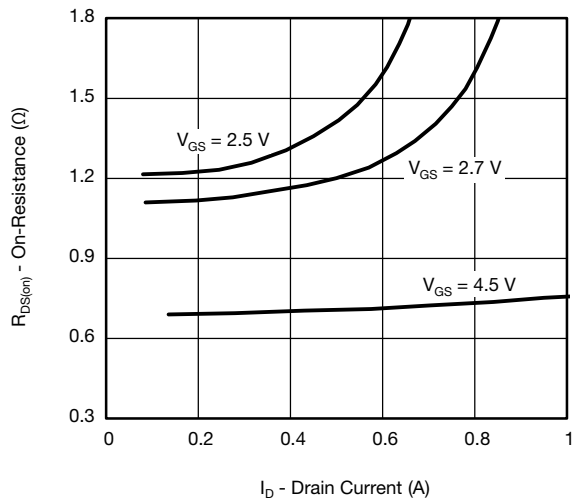
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



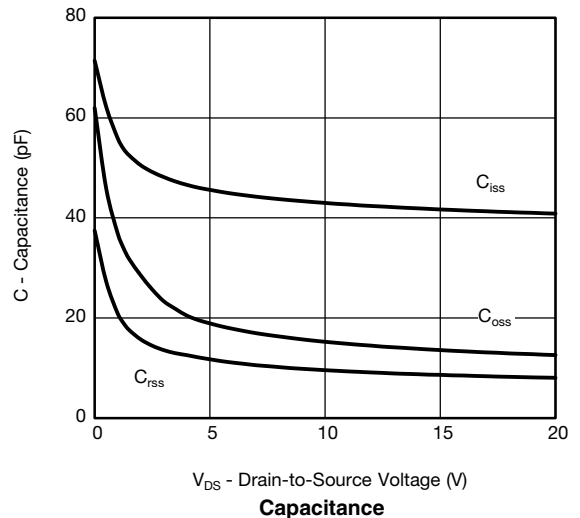
Output Characteristics



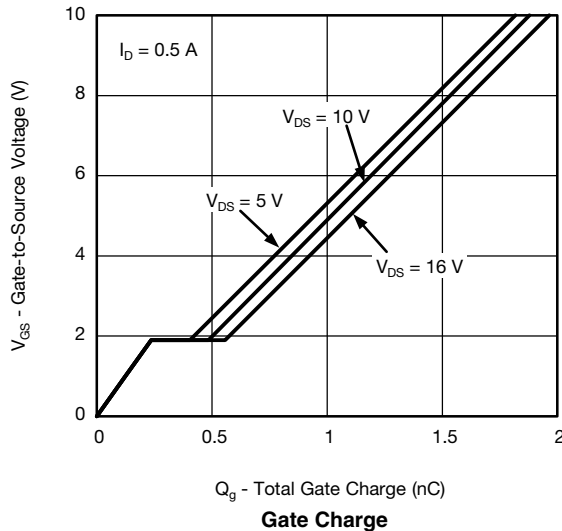
Transfer Characteristics



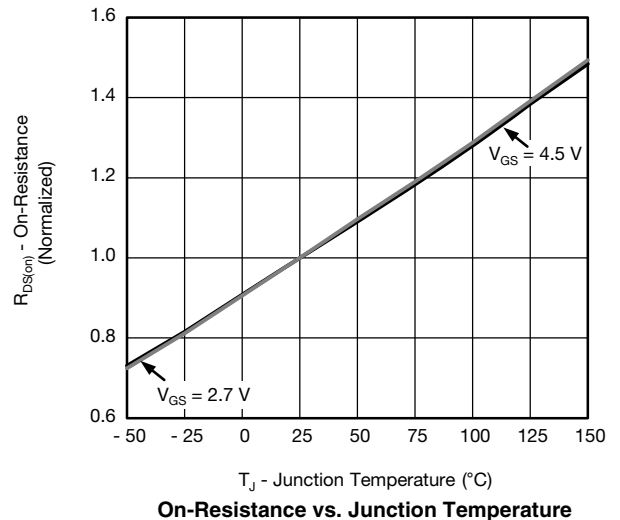
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

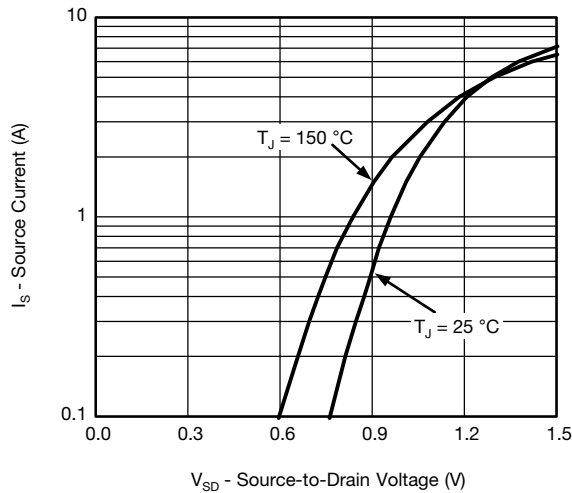


Gate Charge

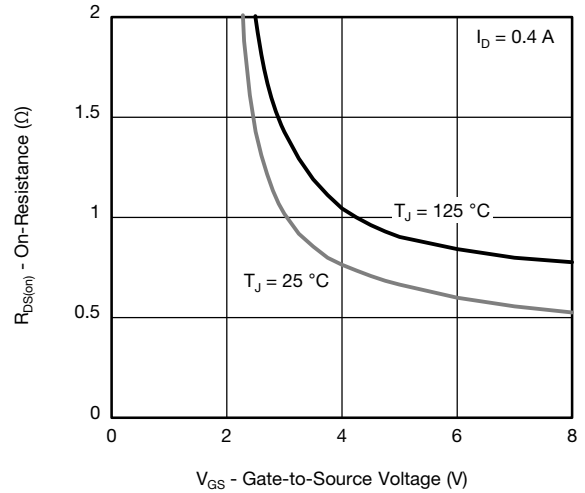


On-Resistance vs. Junction Temperature

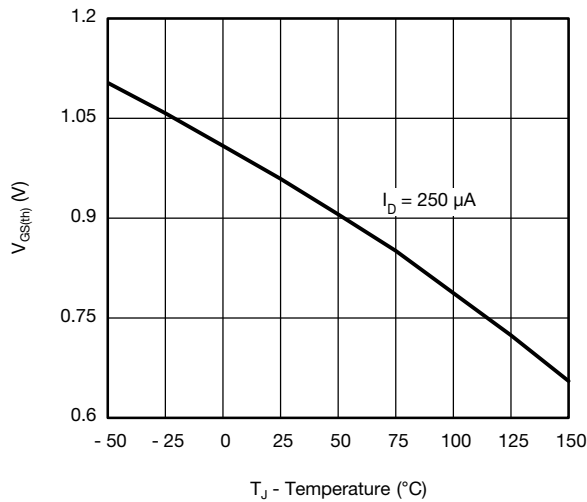
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



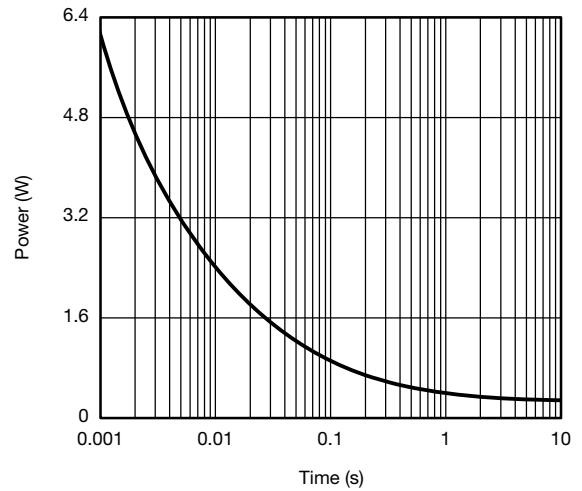
Source-Drain Diode Forward Voltage



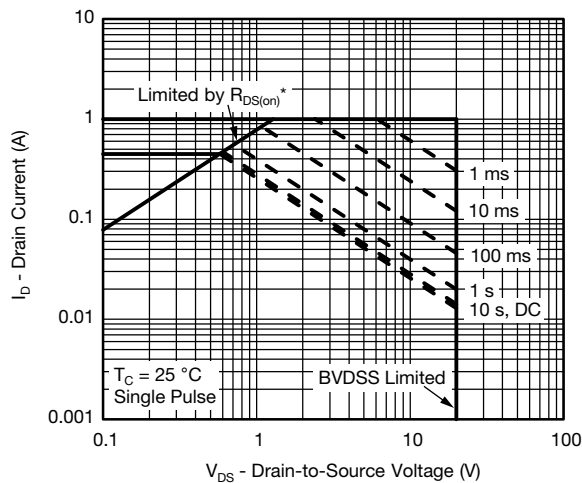
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

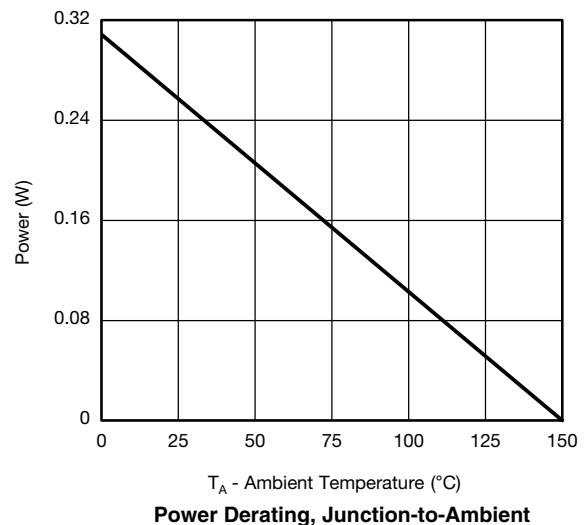
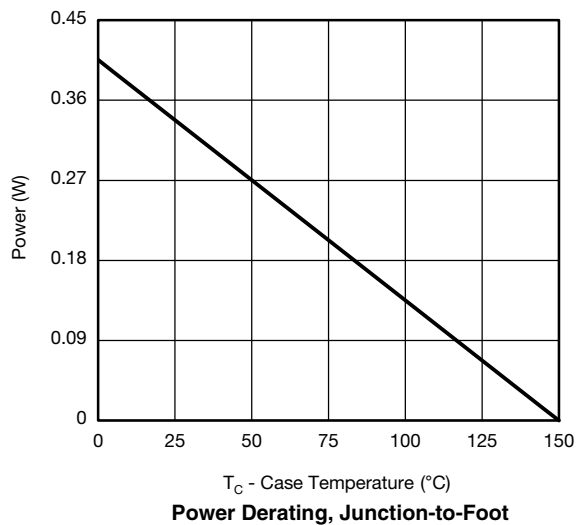
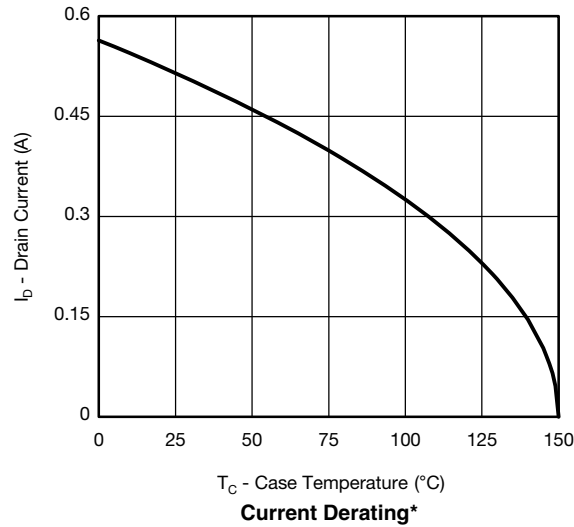


Single Pulse Power, Junction-to-Ambient



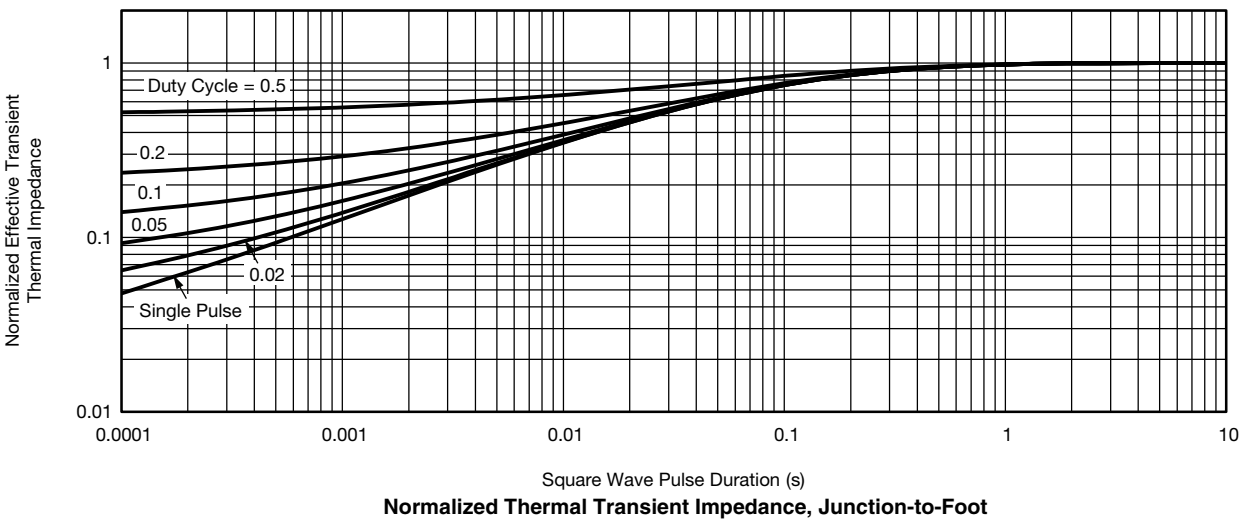
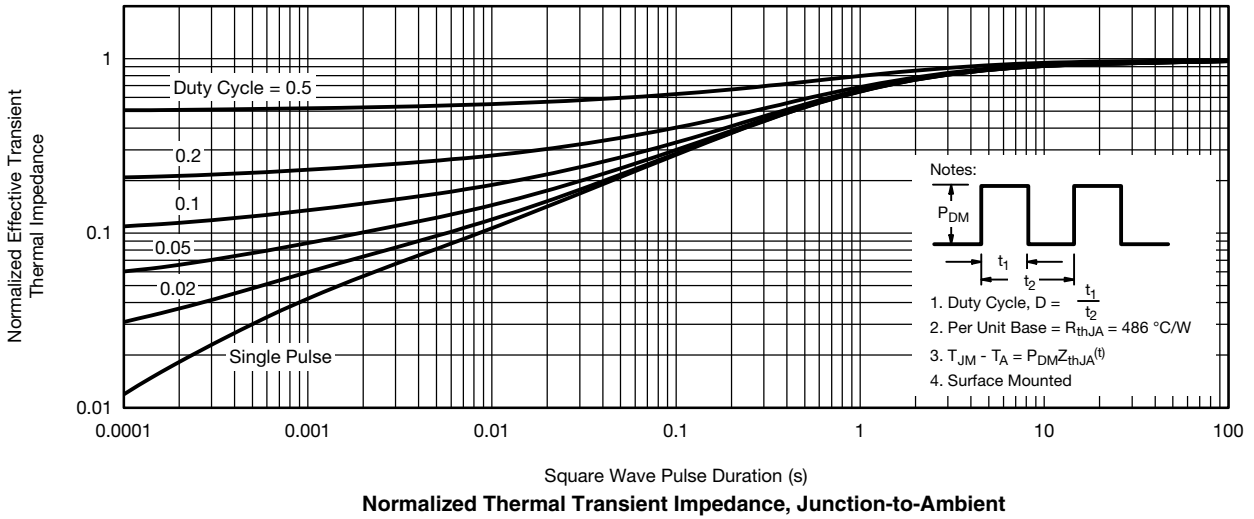
Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

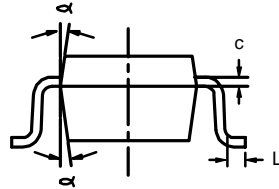
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67693.



SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

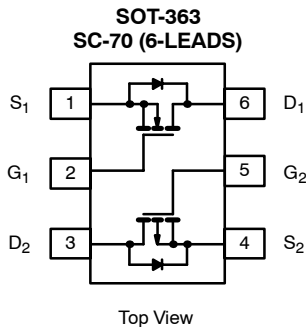


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power

applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The “foot” is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

SC-70 (6-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^{\circ}C - 25^{\circ}C}{400^{\circ}C/W}$	$P_D = \frac{150^{\circ}C - 60^{\circ}C}{400^{\circ}C/W}$
$P_D = 312 \text{ mW}$	$P_D = 225 \text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)	
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518 °C/W
2) Industry standard 1" square PCB with maximum copper both sides.	413 °C/W



FIGURE 2. Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

ASSOCIATED DOCUMENT

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (<http://www.vishay.com/doc?71334>).

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.