# Evaluation Boards for ADF7023 ISM Band Transceiver

# EVAL-ADF7023DBxZ

## Features

**Frequency bands**
- **862 MHz to 928 MHz**
- **431 MHz to 464 MHz**

**Programmable datarates and modulation**
- **1 kbps to 300 kbps**

**FSK/GFSK/OOK/MSK/GMSK modulation**

**Very low power consumption**
- **12.8 mA in PHY_RX mode (maximum front-end gain)**
- **24.1 mA in PHY_TX mode (10 dBm output, single-ended PA)**
- **0.75 µA in PHY_SLEEP mode (32 kHz RC oscillator active)**
- **1.28 µA in PHY_SLEEP mode (32 kHz XTAL oscillator active)**
- **0.33 µA in PHY_SLEEP mode (Deep Sleep Mode 1)**

**High Sensitivity**

**Programmable output power**
- **–20 dBm to +13.5 dBm (single-ended PA)**
- **–20 dBm to +10 dBm (differential PA)**

**Excellent receiver selectivity and blocker resilience**

## General Description

The ADF7023 is a very low power, high performance, highly integrated 2FSK/GFSK/OOK/MSK/GMSK transceiver designed for operation in the 862 MHz to 928 MHz and 431 MHz to 464 MHz frequency bands, which cover the worldwide license-free ISM bands at 433 MHz, 868 MHz, and 915 MHz. It is suitable for circuit applications that operate under the European ETSI EN300-220, the North American FCC (Part 15), the Chinese short-range wireless regulatory standards, or other similar regional standards.

The ADF7023 evaluation platform consists of a 4-layer PCB daughter card which plugs into the Eval-ADF7xxxMB3Z motherboard.

**Table 1 Evaluation Boards**

| Board Number | RF Frequency | Description |
|---|---|---|
| EVAL-ADF7XXXMBZ3 | - | Mother board required for evaluation of the ADF7023 daughter boards |
| Eval-ADF7023DB1Z | 868/915 MHz | Two separate matching networks: One for the single ended PA and one for the LNA |
| Eval-ADF7023DB2Z | 868/915 MHz | One combined matching network incorporating the single ended PA and LNA |
| Eval-ADF7023DB3Z | 433 MHz | Two separate matching networks: One for the single ended PA and one for the LNA |
| Eval-ADF7023DB4Z | 433 MHz | One combined matching network incorporating the single ended PA and LNA |

# TABLE OF CONTENTS



## Revision History

Date: April 18th 2013
Revision: Rev. 1.1

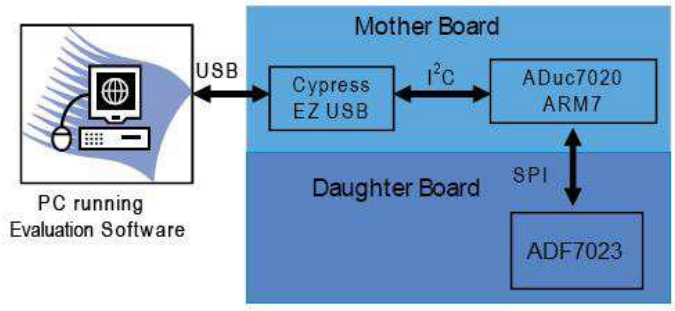
This document accompanies:

ADF7023 software release 1.5.4
Daughter boards using the layout files ADF702xDBExZ RevB and ADF702xDBFxZ RevB
Mother board version EVAL-ADF7XXX_MB3Z RevB running firmware version 2.0.2.3 or higher

# Hardware Overview

The Evaluation Platform consists of the Eval-ADF7XXXMB3Z mother board to which an appropriate daughter card may be connected. The available daughter cards are given in Table 1. Schematics for the daughter cards are given in the *ADF7023 Evaluation Board Schematics and BOMs* section of this document.

The mother board may be powered via the USB cable supplied. The 5V from the USB cable is regulated down to 3.3 V for the Cypress EZ USB IC, the ADuC7020 microcontroller and the ADF7023 transceiver. Alternatively a battery may be used to power the microcontroller and transceiver. A 3.6V battery is shipped with the boards.




**Hardware Overview**

# Getting Started

## *Installing Software*

The ADF7023 evaluation software and documentation can be installed from the Analog Devices ftp site.

(ftp.analog.com/pub/RFL/ADF7023)

The software installation should be carried out before plugging in the ADF7023 Evaluation Boards.

## *Installation Procedure*

1. Run **ADF7023 Rev1.5.4 FULL.exe** to install the evaluation software for the ADF7023. The install will place the relevant files in the folder C:\Program Files\Analog Devices BV\ADF7023. It will also create shortcuts on the start menu. Any previous versions of the software will be removed before the installation commences (Figure 1).
2. 


**Figure 1**

3. Click on "Yes" to install the software (Figure 2).

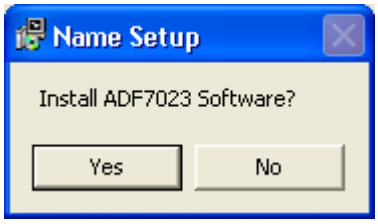



**Figure 2**

4. Click "***Next***" (Figure 3):

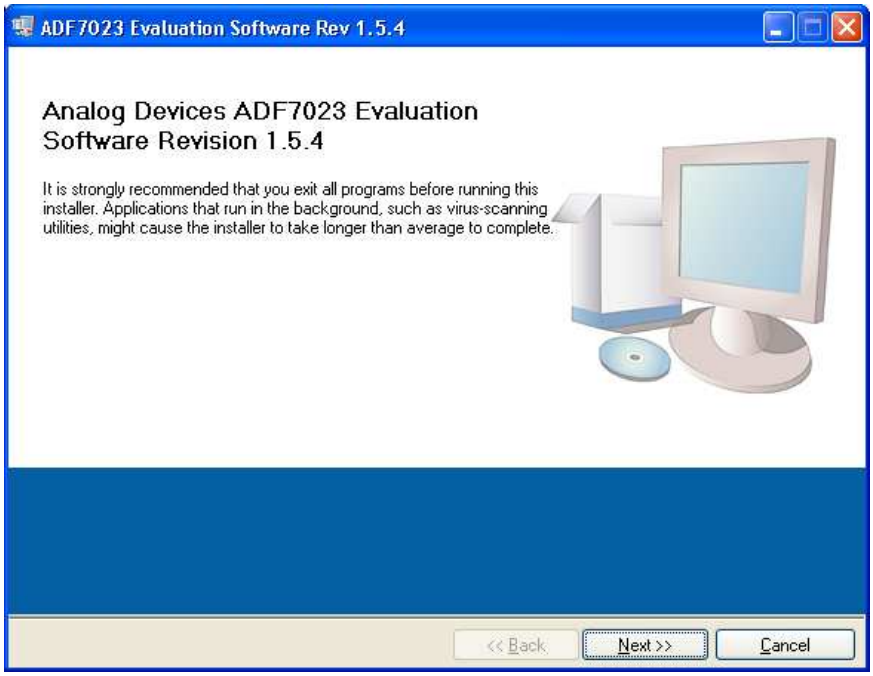



**Figure 3**

5. Click "***Next***" (Figure 4):

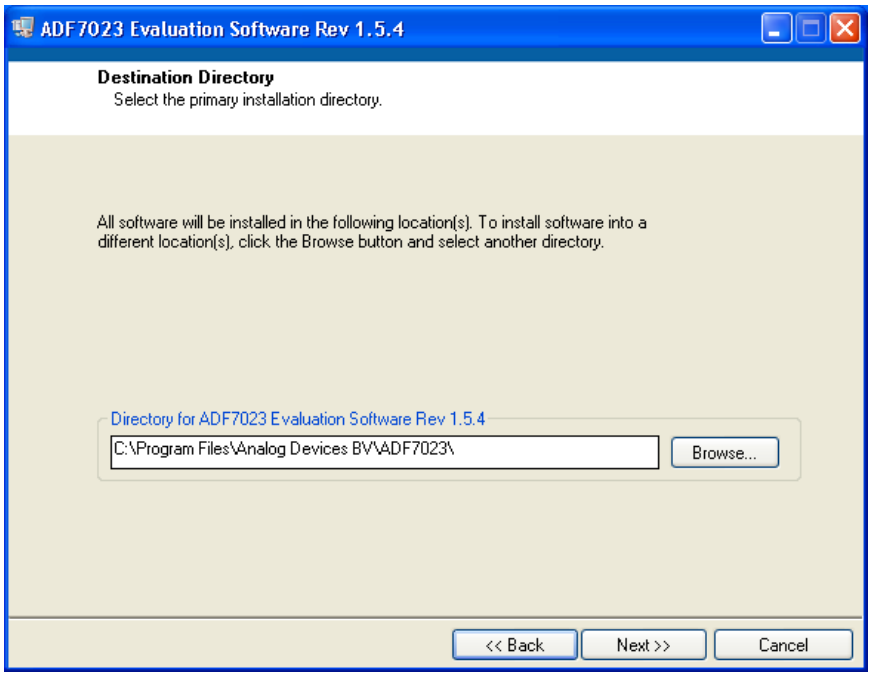



**Figure 4**

6. Click "***I accept this license Agreement***"

   Then Click "***Next***" (Figure 5):

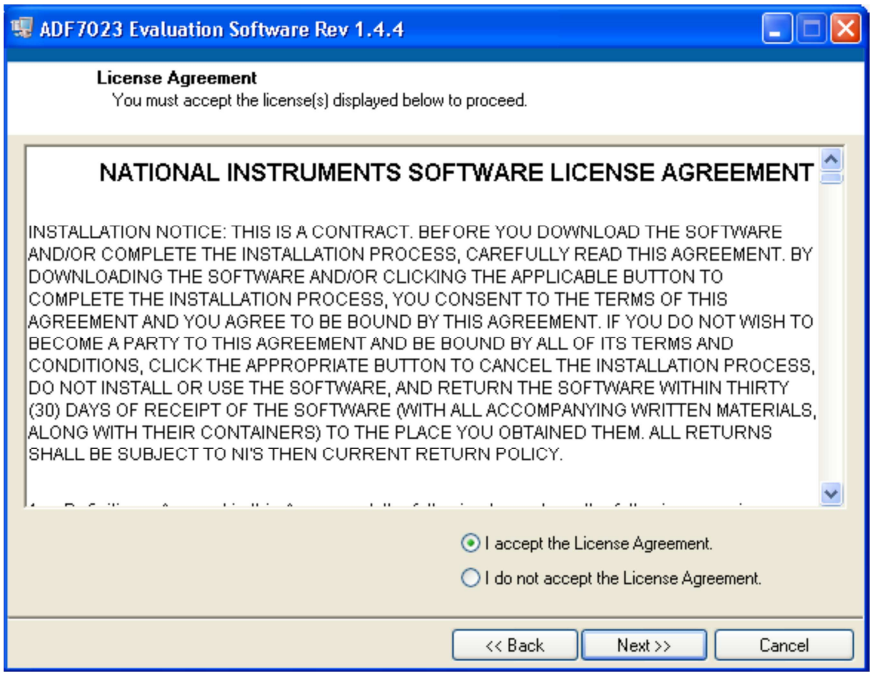



**Figure 5**

7. Click "***Next***" (Figure 6):

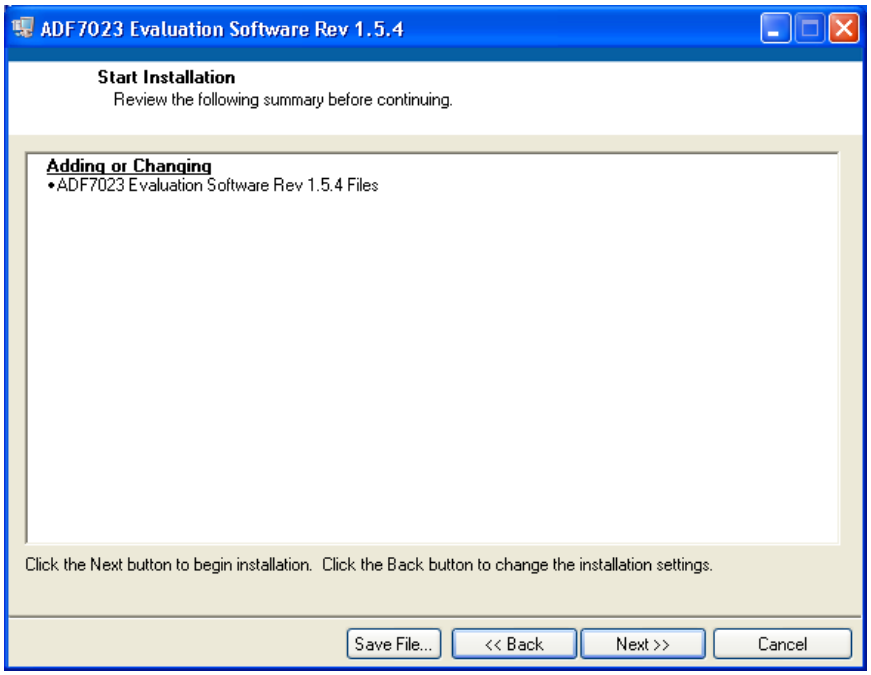



**Figure 6**

8. Click "*Next*" (Figure 7):

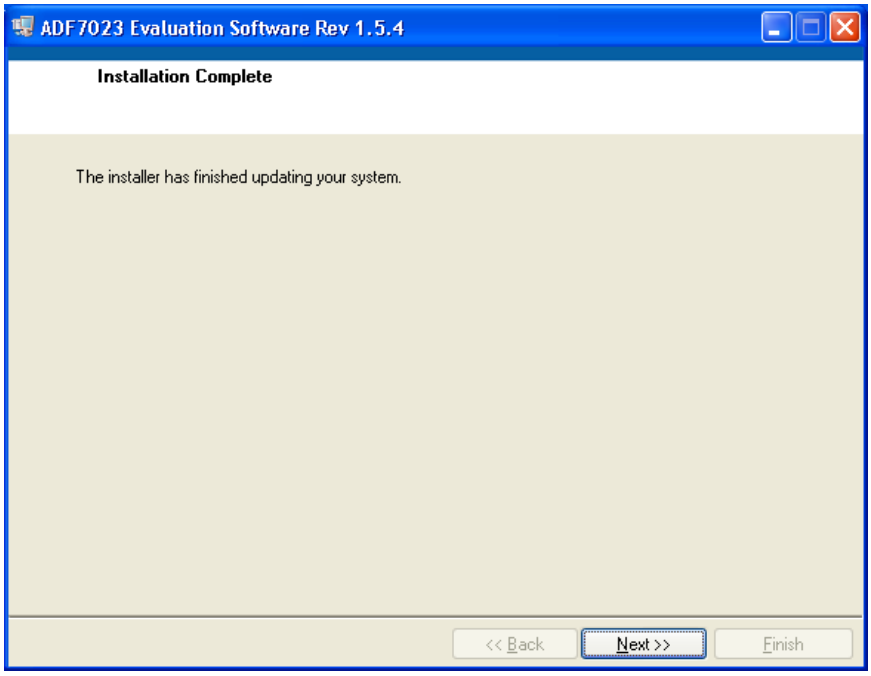



**Figure 7**

9. Click "*Next*" (Figure 8):

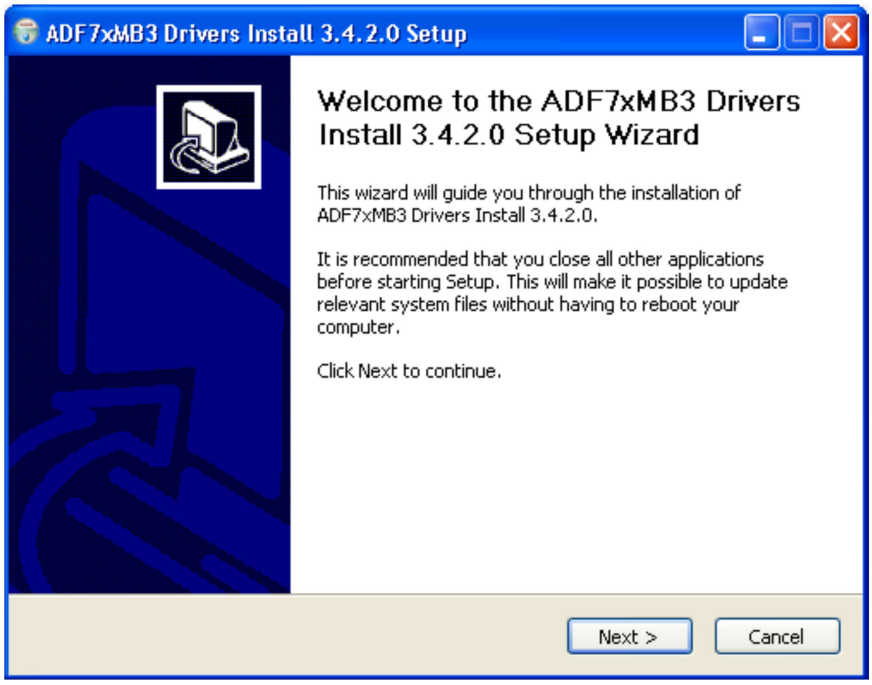



**Figure 8**

10. Click "*Next*" (Figure 9):

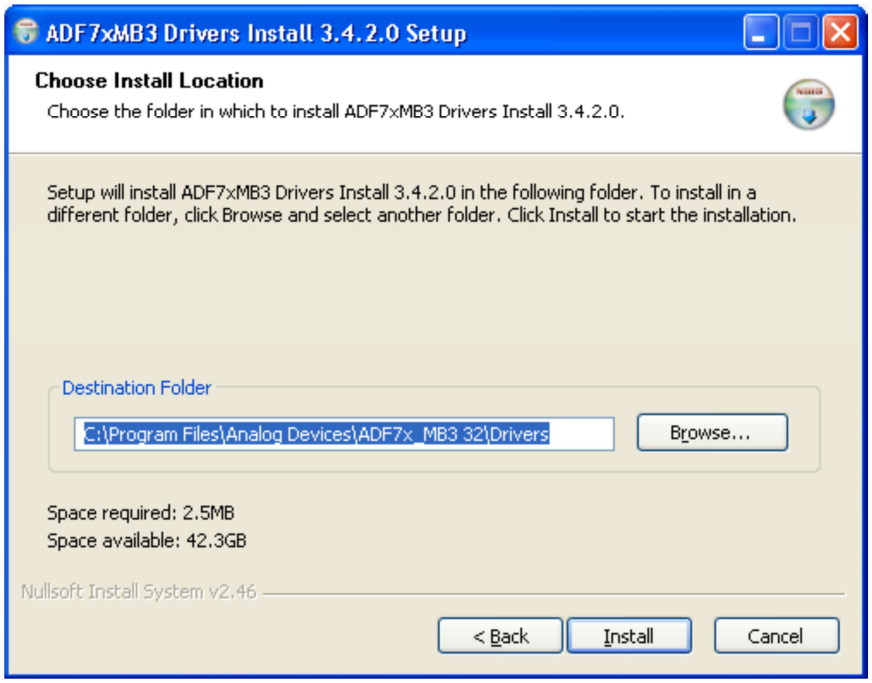



**Figure 9**

11. Click "*Next*" (Figure 10):

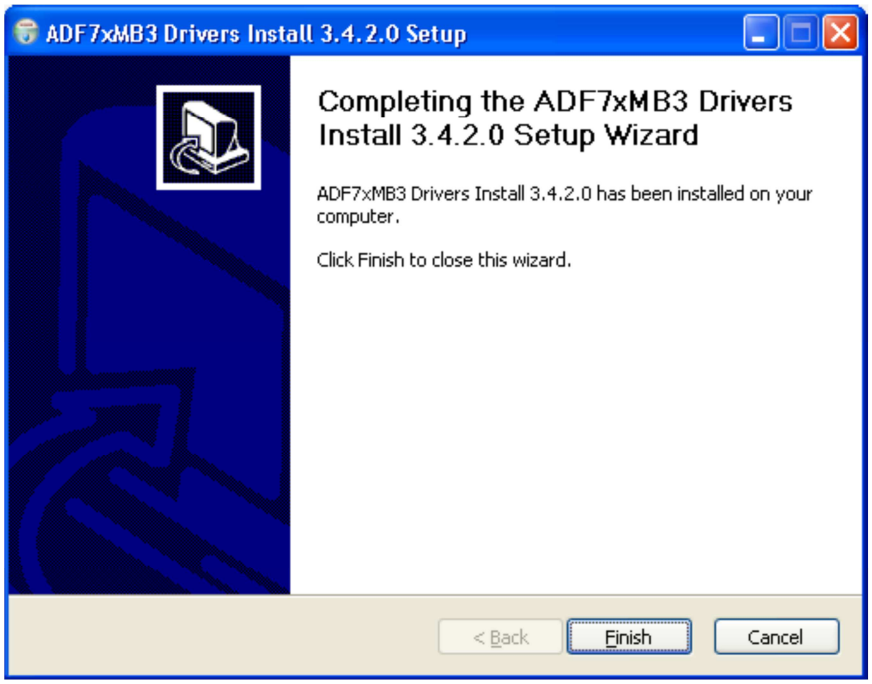



**Figure 10**

12. At this point the ADF7xxxMB3Z Motherboard can be plugged into a free USB port.

13. The following screen will appear:
Ensure the ***"Install the software automatically"*** option is checked as in Figure 11.
Then click "***Next***" :

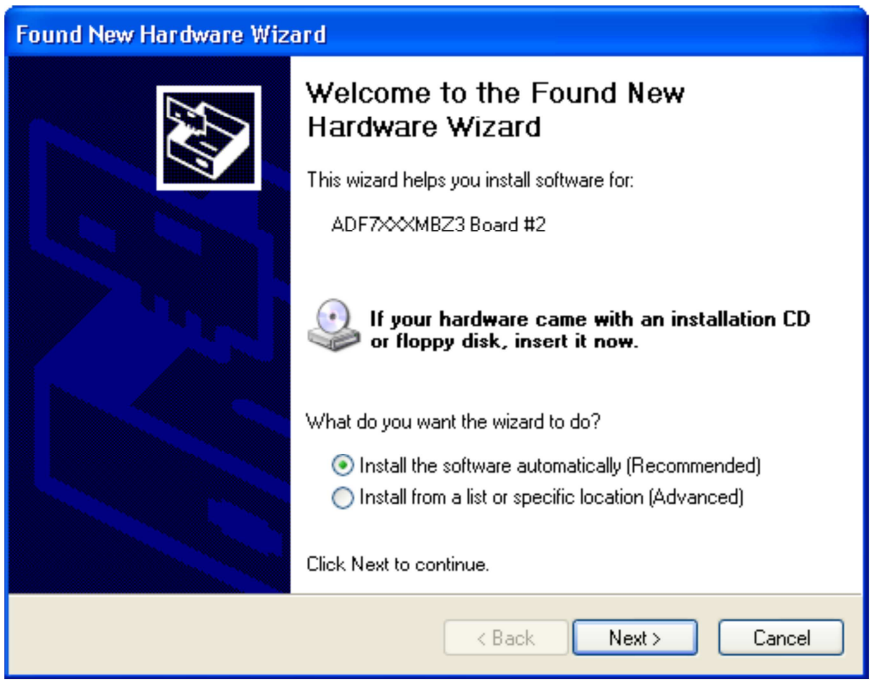



**Figure 11**

14. Click ***"Continue Anyway"*** ( Figure 12):

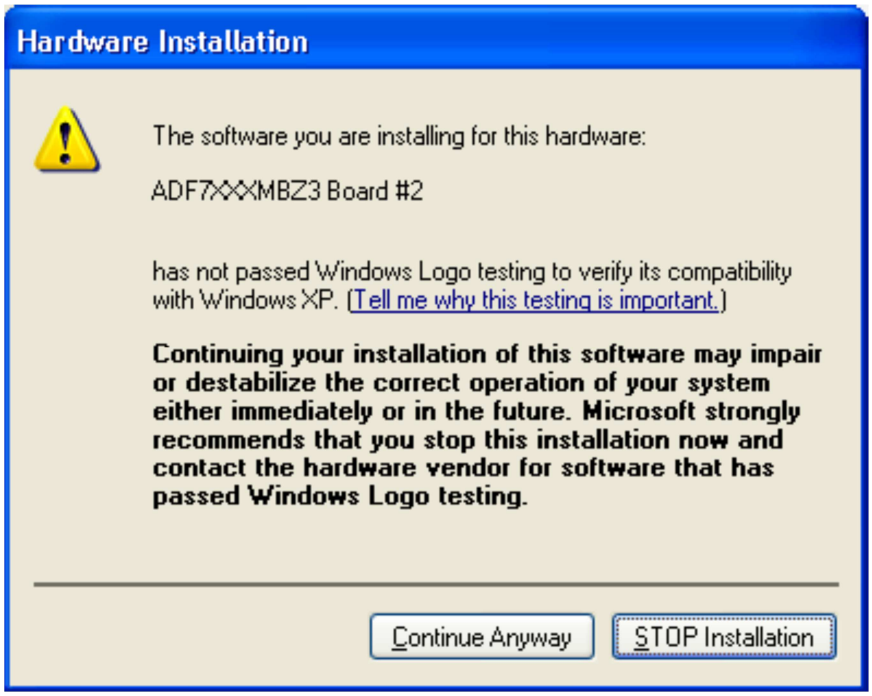



**Figure 12**

15. Click ***"Finish"*** ( Figure 13):

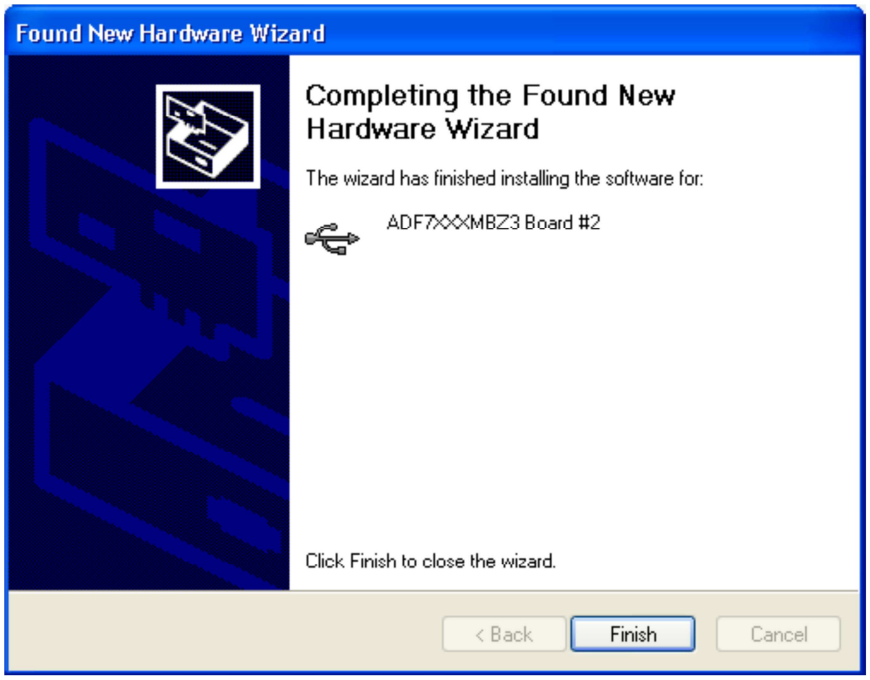



**Figure 13**

## Connecting the Evaluation Boards

This software can allow **TWO** evaluation boards to be connected to a single PC. The EVAL board and the software must be setup accordingly.

Ensure that **Switch 4** is in the correct position before connecting to the PC as shown in Figure 14.

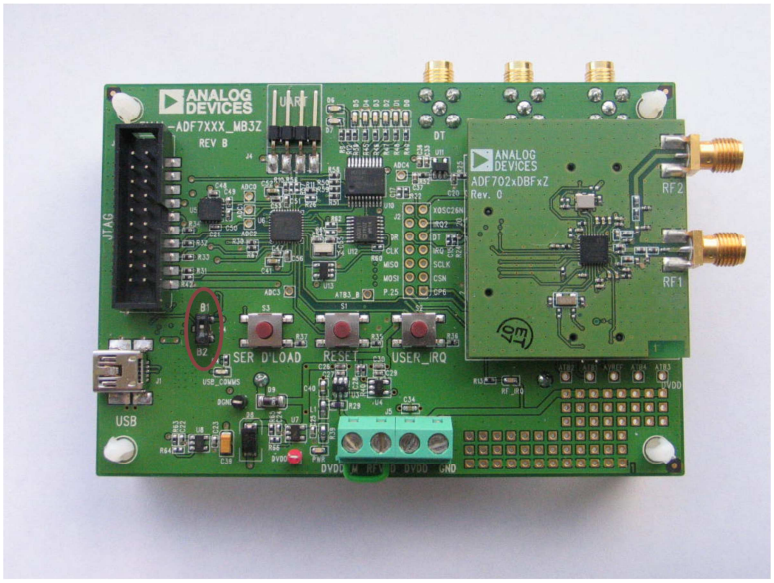



**Figure 14**

- To set the first board as "**BOARD 1**" (Figure 15) on the Software set the switch shown in Figure 14 to "**B1**"
- To set the second board as "**BOARD 2**" (Figure 15) on the Software set the switch shown in Figure 14 to "**B2**"

Ensure the evaluation mother board with the desired daughter card is connected to the PC via USB cable before running the software.

Run the ADF7023 software from Start-> Programs->Analog Devices->ADF7xxx->ADF7023.

Once the software is running press Connect USB (Figure 16).

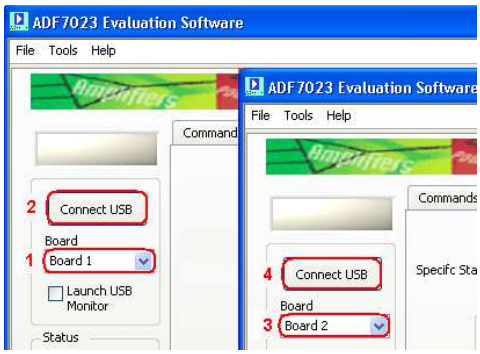



**Figure 15**

## Using the Evaluation Software

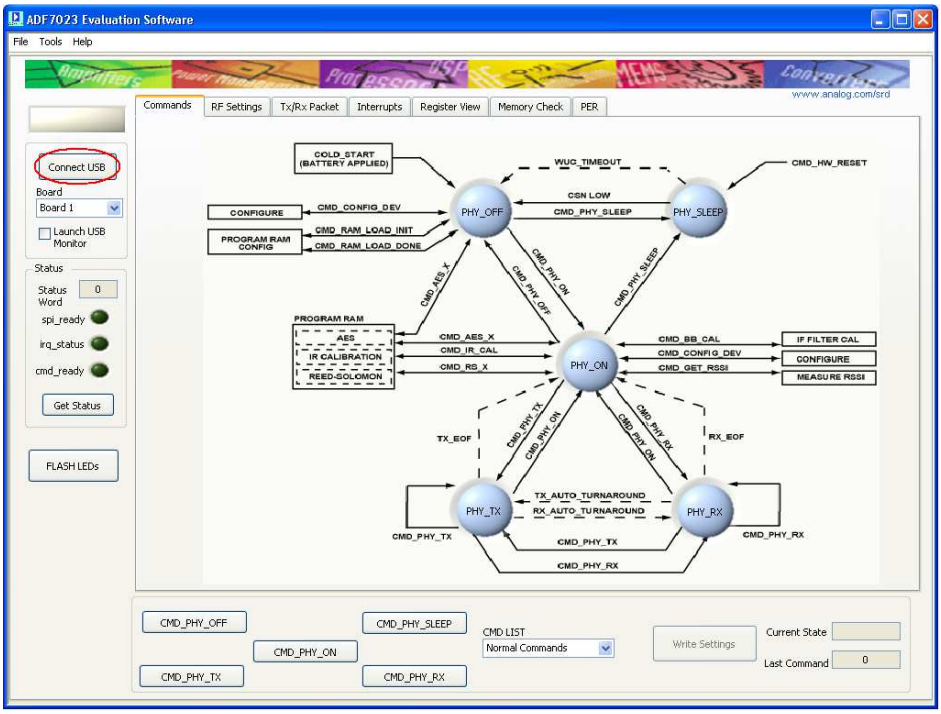



**Figure 16**

Wait until the BUSY signal above the Connect USB button is turned off before pressing any further buttons on the software interface.

The Firmware for the motherboard is automatically checked each time the software is loaded to ensure the revisions are kept up to date.

If the firmware is out of date the following message will pop up (Figure 17):

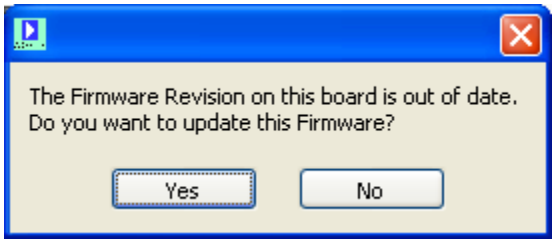



**Figure 17**

To go through the update procedure, refer to the ***Mother Board Firmware Update*** section.

Next enter state PHY_ON by pressing the command CMD_PHY_ON.

This can be done by pressing Button A or Button B (Figure 18).

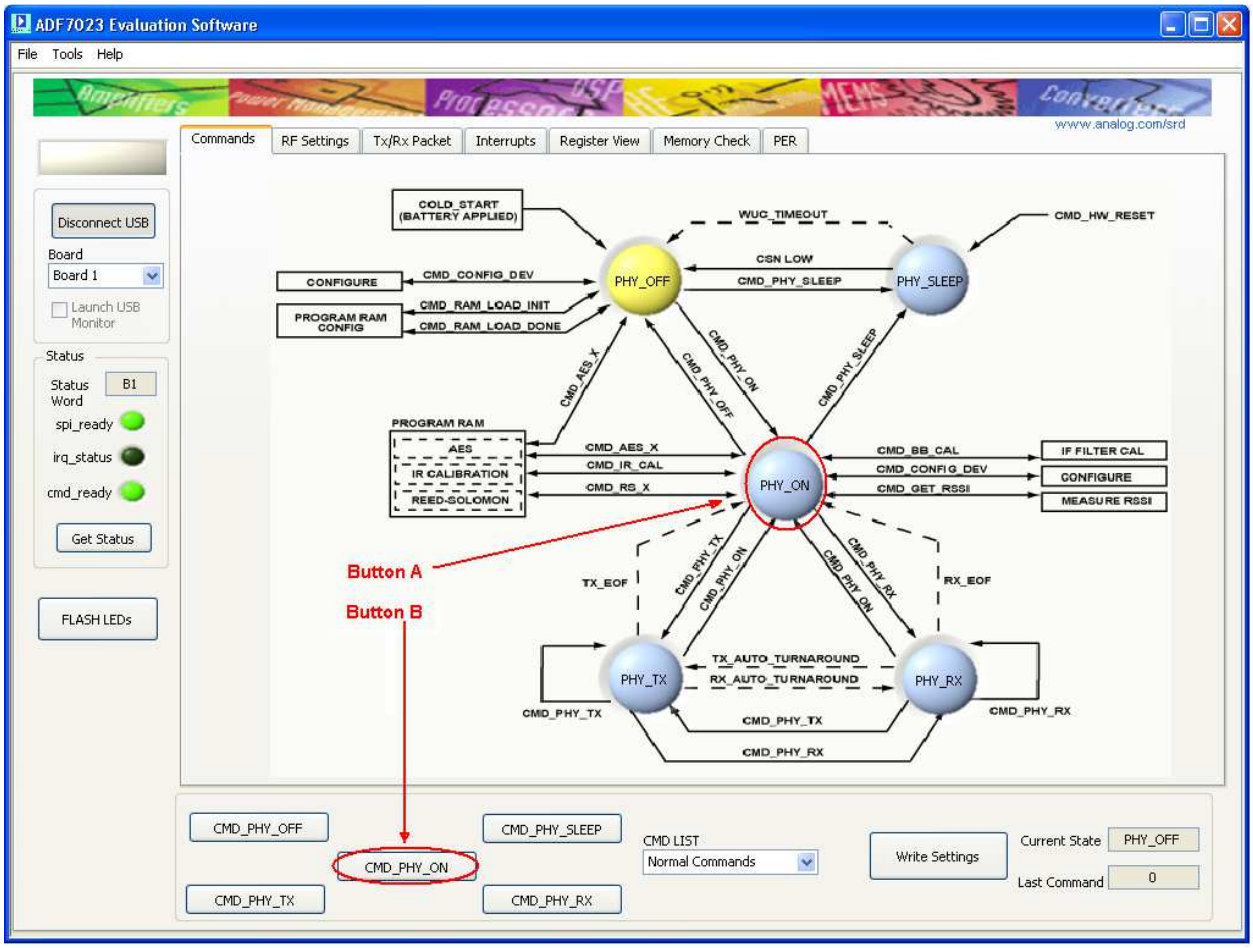



**Figure 18**

The current status of the ADF7023 will be reflected by the color of the buttons on the **"Commands"** tab.

Note: If at any time it is desired to unplug the USB cable, click "***Disconnect USB***" first (Figure 19).

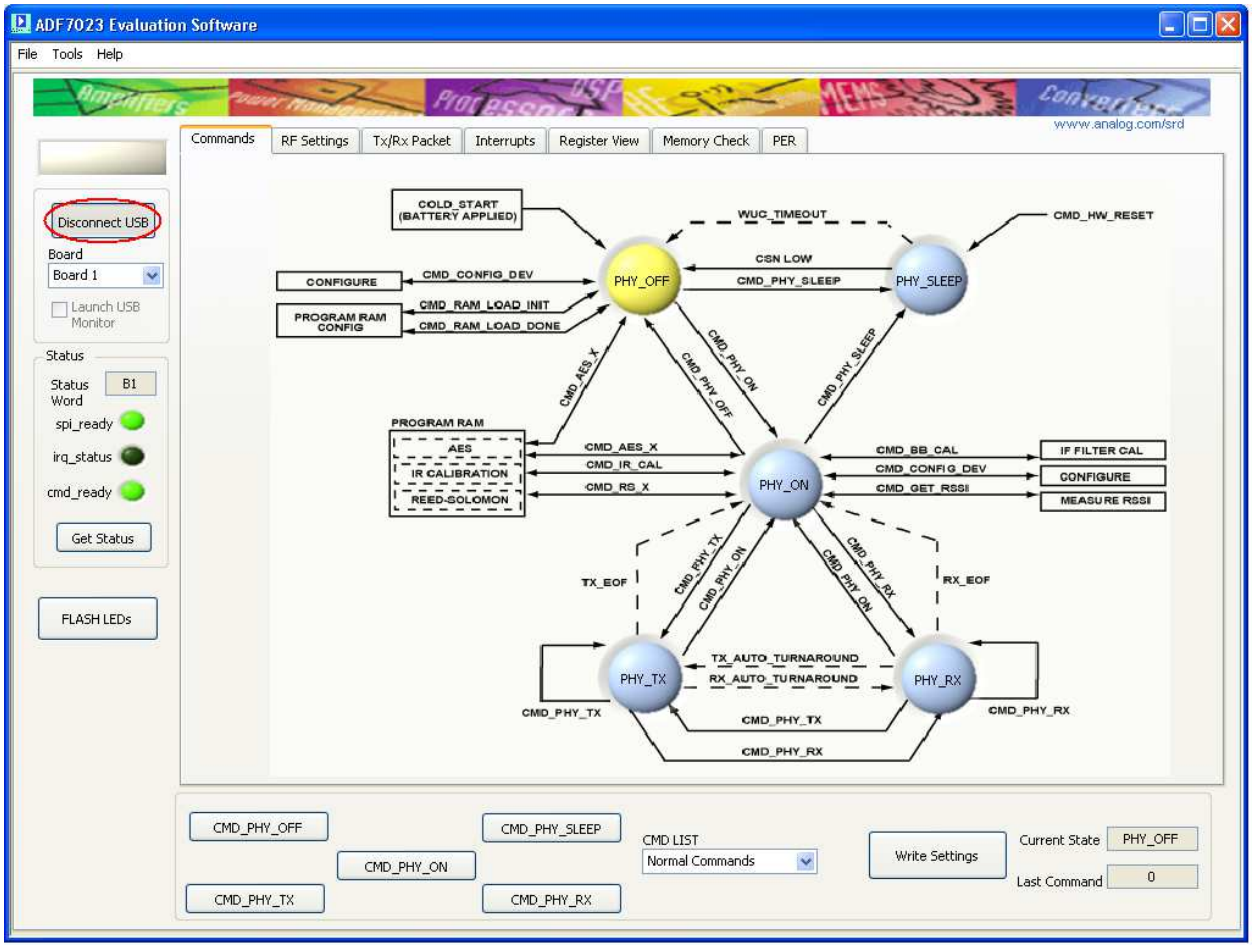



**Figure 19**

## *Mother Board Firmware Version*

The Motherboard firmware revision check is done automatically when "Connect USB" is clicked. If the firmware revision is not correct a popup screen will appear asking the user to update the Firmware (Figure 20).

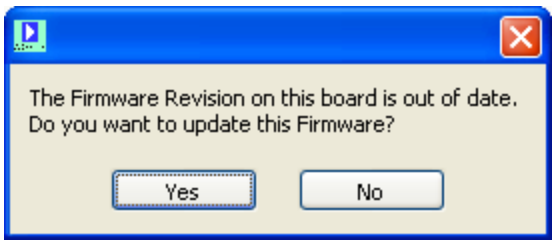



**Figure 20**

To manually check the firmware after connecting the USB select ***Help*** -> ***Check Firmware Revision*** as shown in Figure 21**Error! Reference source not found.**.
If this value is less than 02.00.02.05 then the firmware version will need to be updated.

Firmware update procedure can be found in the ***Mother Board Firmware Update*** section.

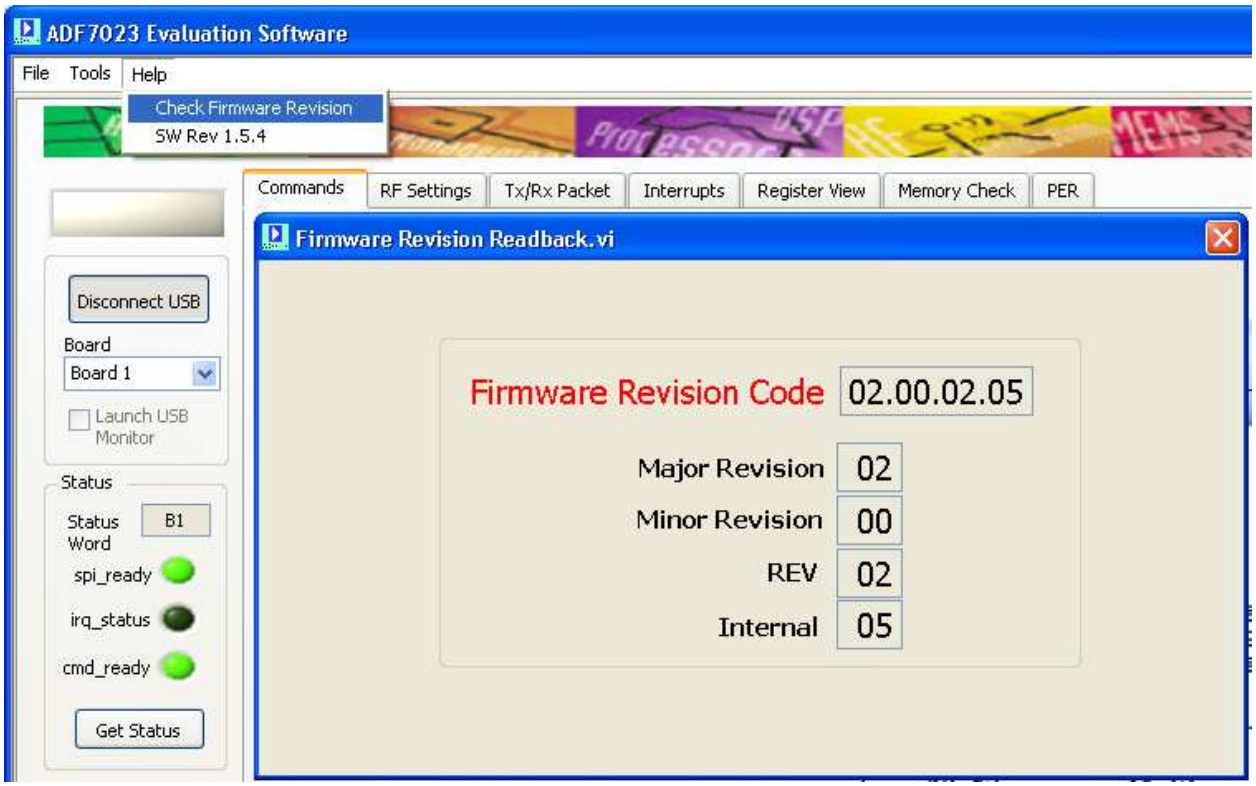



**Figure 21**

## *Mother Board Firmware Update*

1. Before beginning this procedure ensure ONLY the board you wish to update the firmware on is connected to the PC.

2. To update the firmware select "***Tools***" -> "***Motherboard Firmware Download***" (Figure 22).

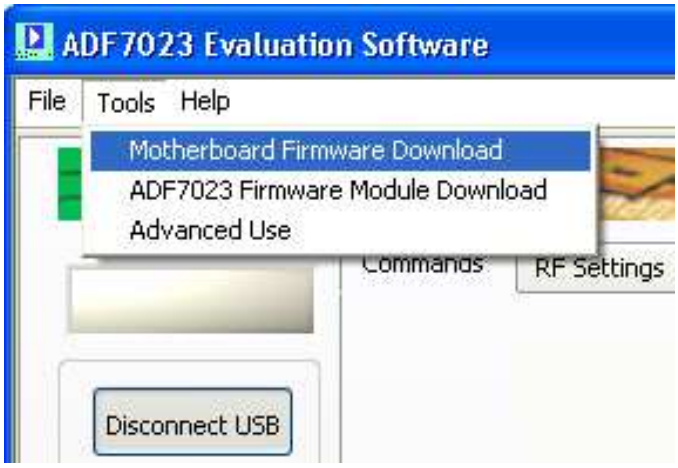



**Figure 22**

3. Select the desired firmware version "***EVAL_ADF7XXXMB3Z_Rev_2.0.2.5.hex***" from the default directory (Figure 23).

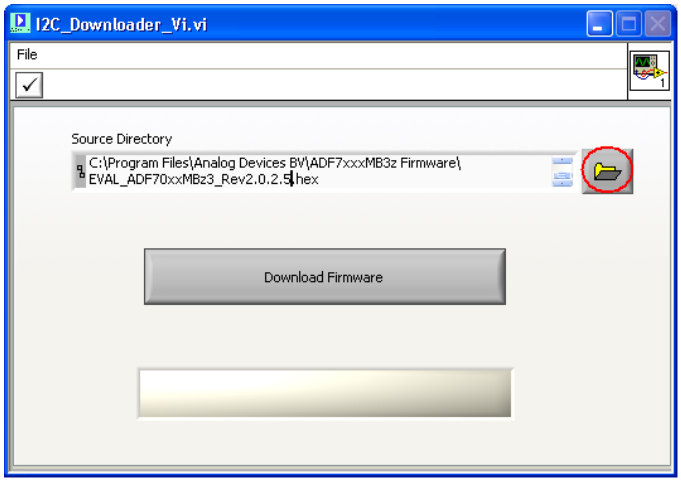



**Figure 23**

4. Click "***Download Firmware***" and follow the onscreen instructions ( Figure 24).

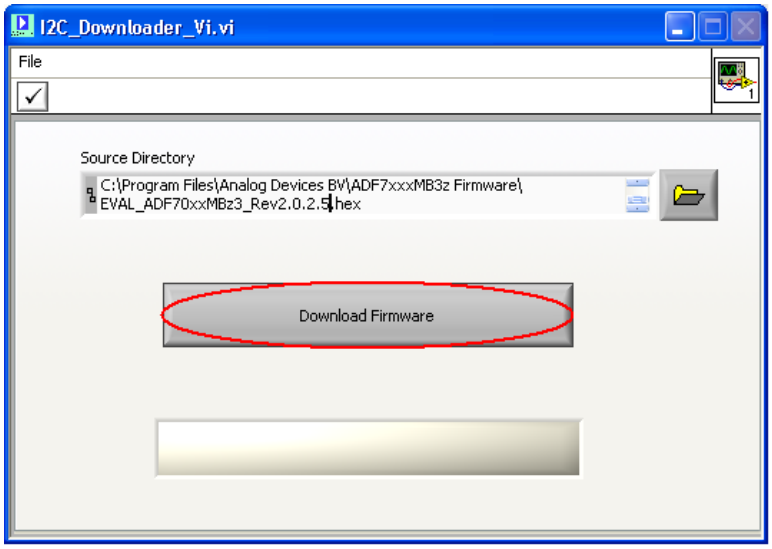



**Figure 24**

5. "***SER DLOAD*** and "***RESET***" buttons will be referenced and can be found as shown in Figure 25.

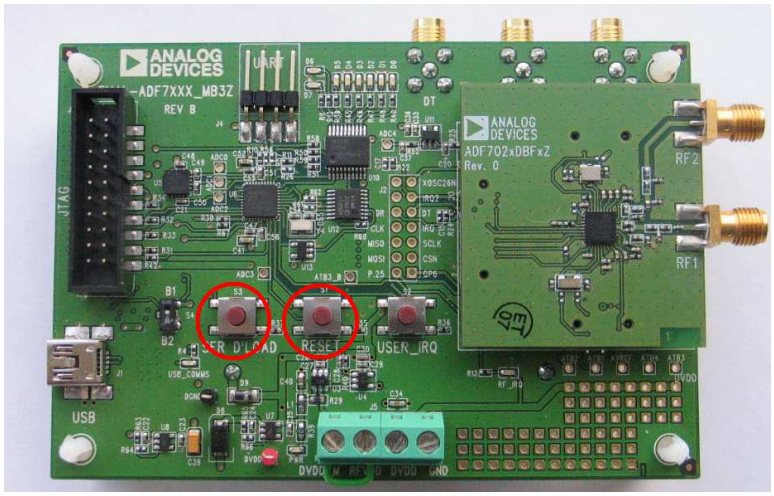



**Figure 25**

6. Disconnect and then reconnect the USB cable from the evaluation platform.
7. The mother board firmware is now updated.

## *Basic RF testing in SPORT Mode*

1. Select the "***RF Settings***" Tab and set the RF parameters as required. (*Figure 26 point*(1))
2. If not already in ***PHY_ON*** enter this state by pressing ***CMD_PHY_ON***. (*Figure 26 point* (5))
3. Select the ***SPORT Mode*** (*Figure 26 point* (2))
4. Press ***Update Needed***. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV. (*Figure 26 point* (3))
5. Press ***CMD_PHY_RX***. The part now enters PHY_RX. (*Figure 26 point* (4))
6. To exit ***PHY_RX*** press ***CMD_PHY_ON*** (*Figure 26 point* (5))

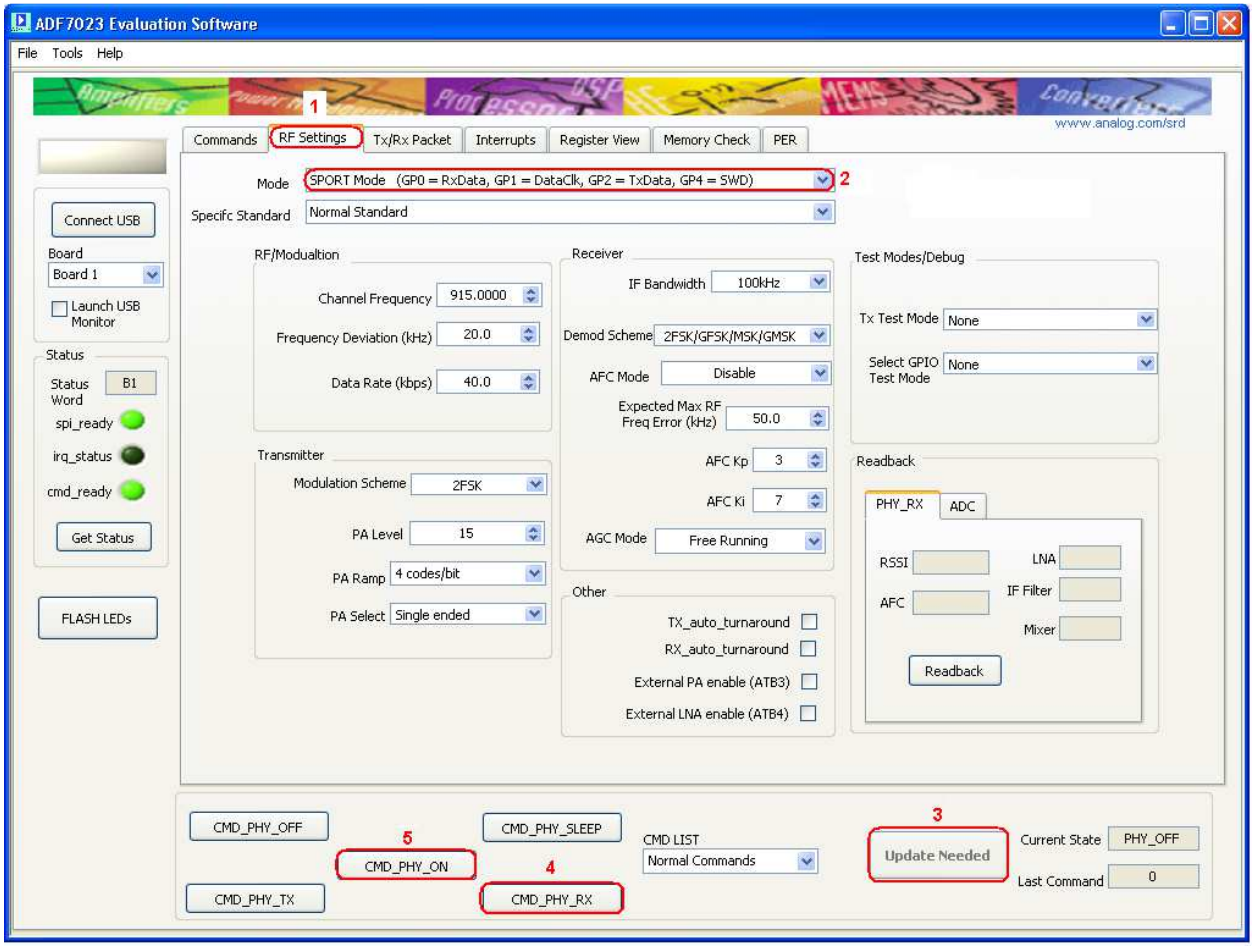



**Figure 26**

- While in ***PHY_RX*** with SPORT mode enabled, the received data demodulated by the ADF7023 will appear at the **DR** SMA connector on the mother board as shown in *Figure 27*

- A clock synchronized with the demodulated data will appear at the **CLK** SMA connector as shown in *Figure 27*.

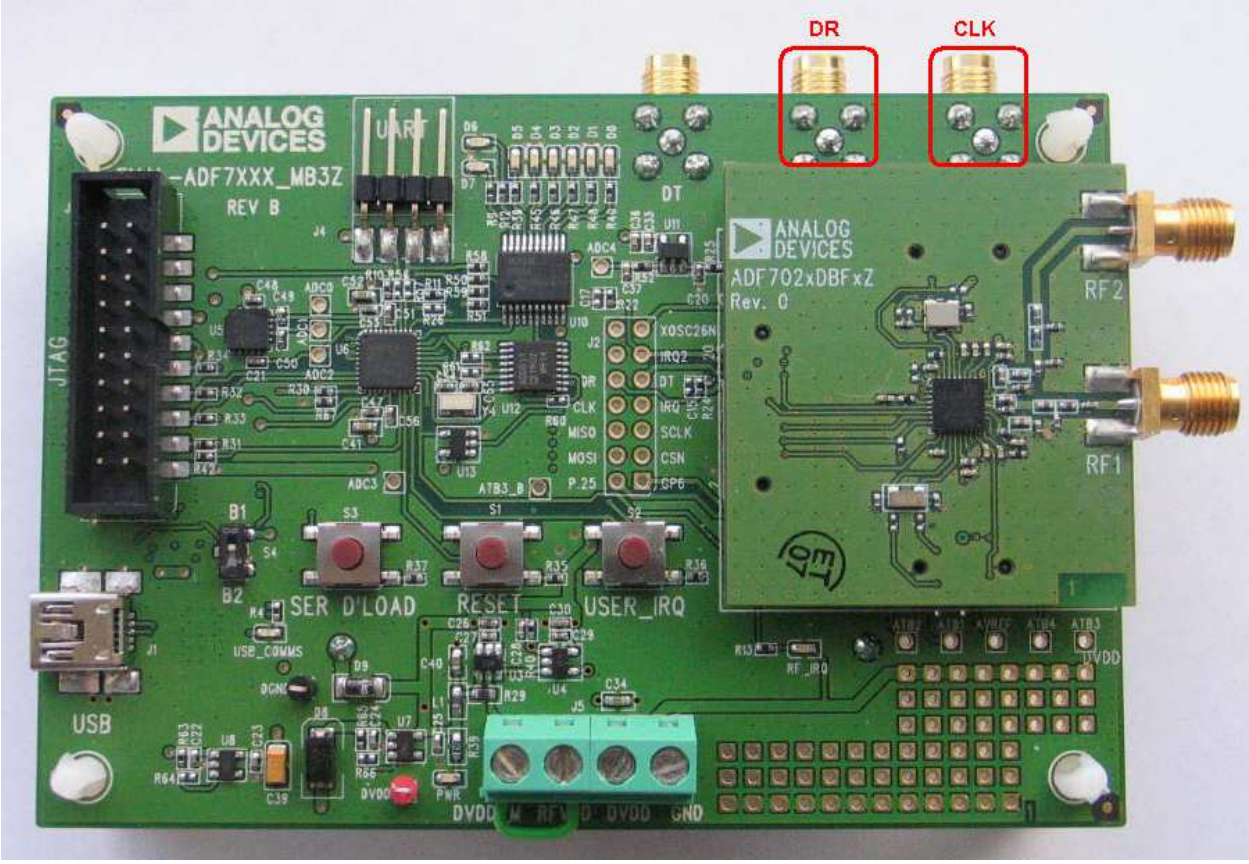



**Figure 27**

## *Entering PHY_TX for basic RF Carrier testing*

1. Select the "***RF Settings***" Tab and set the RF parameters as required. (*Figure 28point* (1)
2. Select "***Packet Mode***" (*Figure 28point* (2))
3. Set Tx Test Mode to "***Transmit Carrier***" (*Figure 28point* (3))
4. Ensure part is in ***PHY_ON*** (*Figure 28point* (4))
5. Press ***Update Needed***. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV (*Figure 28point* (5))
6. Press "***CMD_PHY_TX***" to enter transmit mode (continuous carrier transmission) (*Figure 28point* (6))
7. To exit ***PHY_TX*** press ***CMD_PHY_ON*** (*Figure 28point* (4))

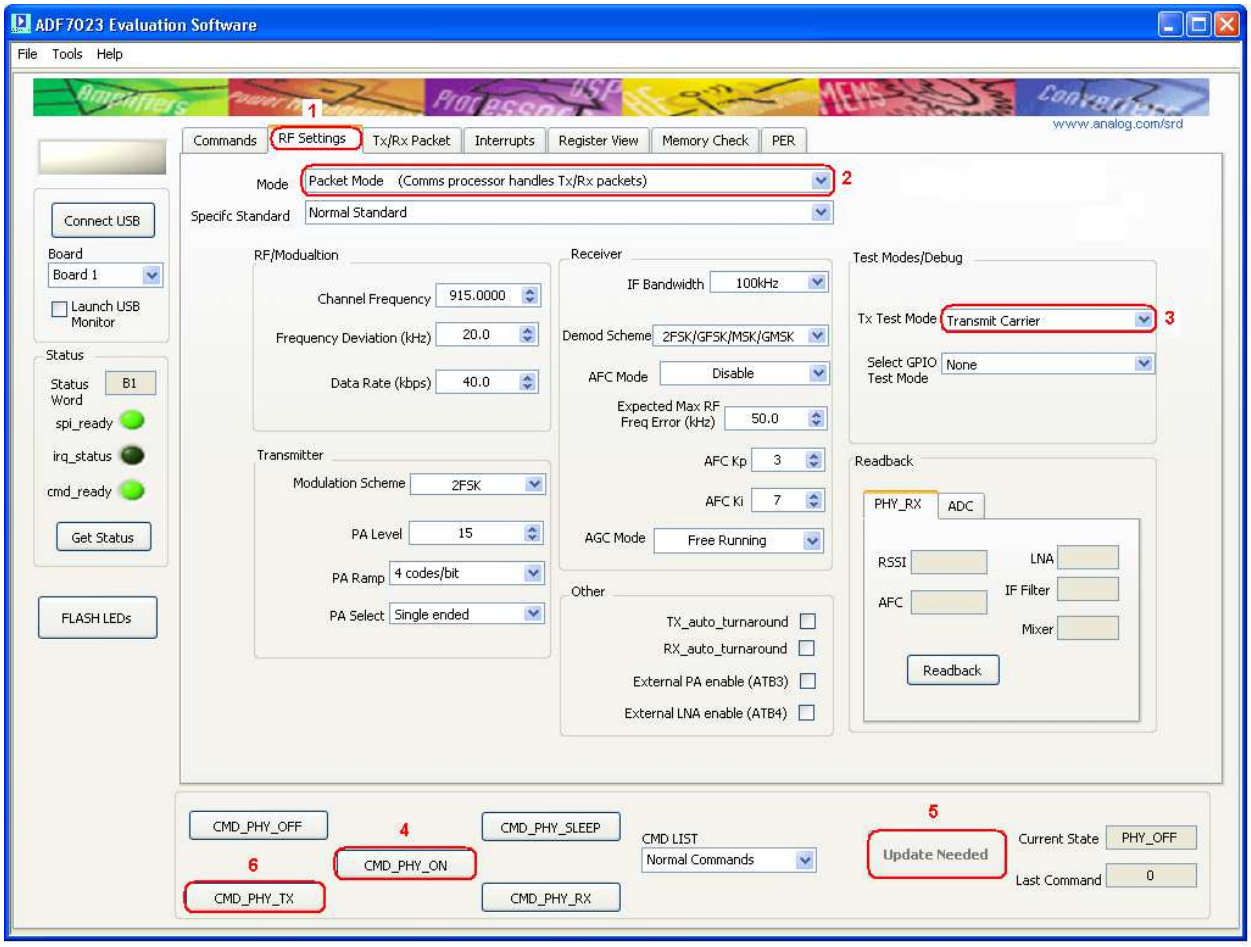



**Figure 28**

## *Entering PHY_TX for basic RF Data testing*

1. Select the "***RF Settings***" Tab and set the RF parameters as required. (*Figure 29 point* (1))
2. Select the ***SPORT Mode*** . (*Figure 29 point* (2))
3. Ensure part is in ***PHY_ON*** (*Figure 29 point* (4))
4. Press ***Update Needed***. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV. (*Figure 29 point* (3))
5. Press "***CMD_PHY_TX***" to enter transmit mode (continuous carrier transmission) (*Figure 29 point* (5))
6. To exit ***PHY_TX*** press ***CMD_PHY_ON*** (*Figure 29 point* (4))

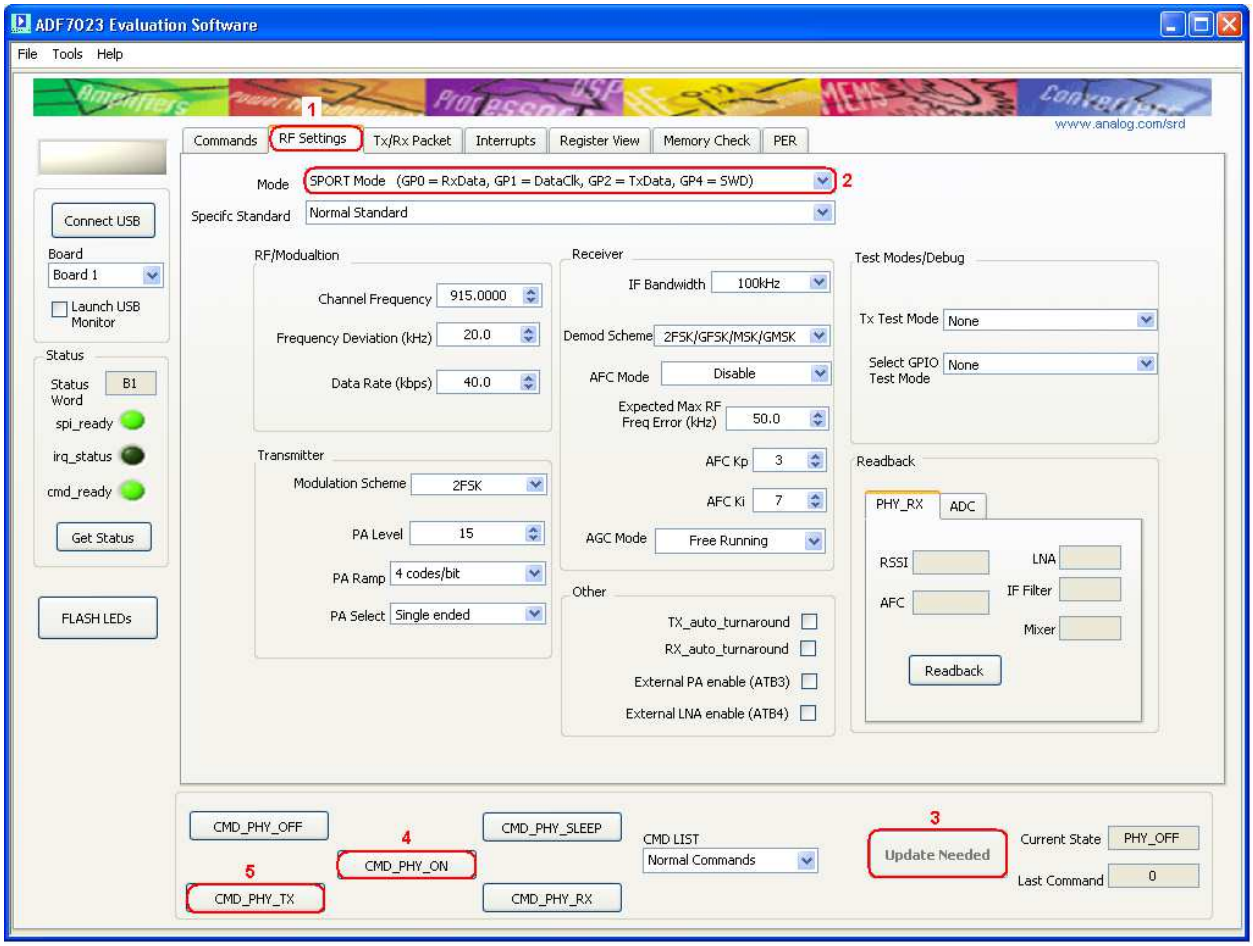



**Figure 29**

- While in ***PHY_Tx*** with SPORT mode enabled, the transmitted data must synchronized with the output clock seen on the **CLK** SMA connector on the mother board as shown in (*Figure 30*)

- The Tx data line, from the users Tx device, should be connected to the **DT** SMA connector as shown in (*Figure 30*).

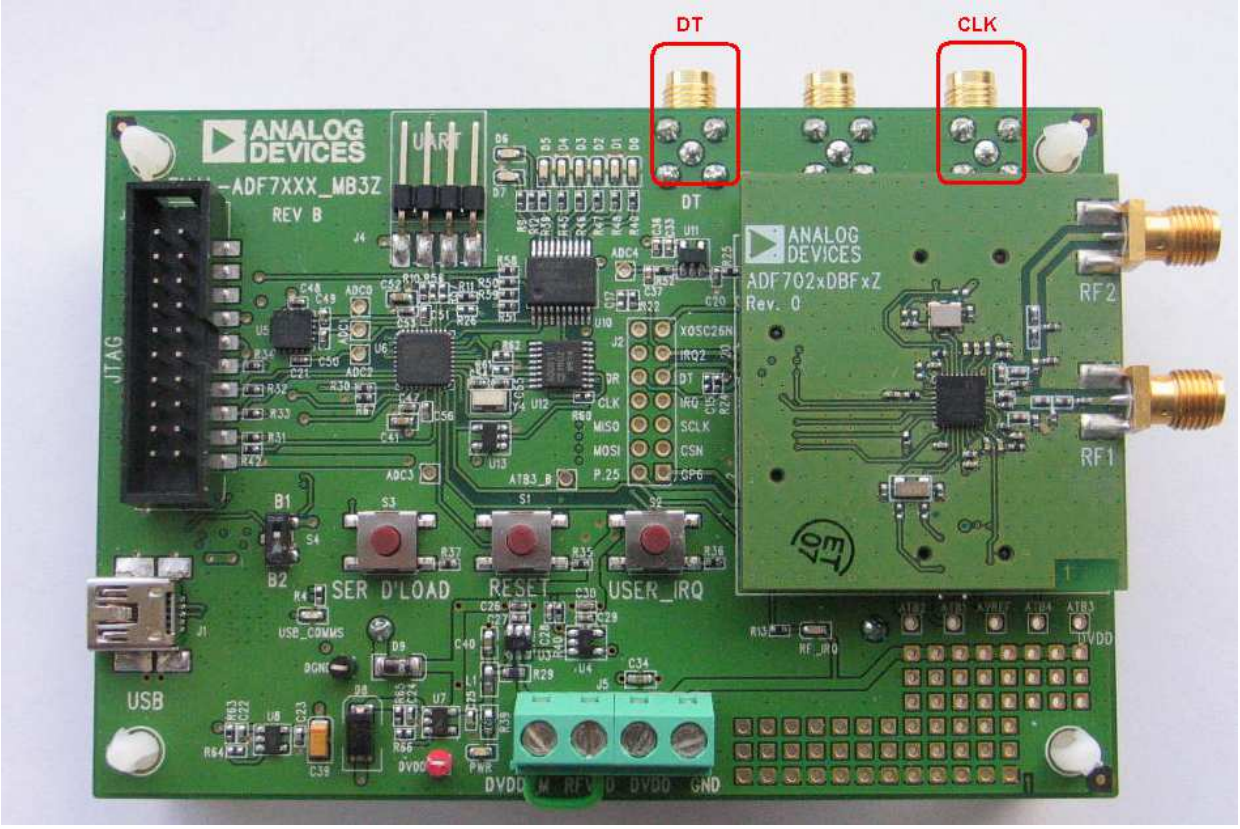



**Figure 30**

# *Simple Rx / Tx Test in Packet Mode*

This section gives a brief introduction on how to Transmit and Receive a packet using the ADF7023 Platform.

## *Rx Setup in Packet Mode*

The settings which follow are for use with EVAL-ADF7023DB1z daughter boards. If you are using a different Daughter board, ensure that the frequency is set within the correct range of the board you are using. Please refer to *Table 1 Evaluation Boards* if you are unsure what the frequency range of you board is designed for.

### *Receiver Board RF Settings*

1. Ensure the **First** ADF7023 Daughter board is correctly plugged into the **First** Mother board and that the "**Current_State**" is "***PHY_ON***" on the **First** instance of the ADF7023 Software.
   Refer to **Connecting the Evaluation Boards** for setup procedures.

2. Select the "***RF Settings***" Tab (Figure 31 point (*1*))

3. Ensure "***Packet mode***" is selected. (Figure 31 point (*2*))

4. Set the "***RF/Modulation"*** parameters as required. (Figure 31 point (*3*))

5. Set the "***Receiver"*** parameters as required. (Figure 31 point (*4*))
   If using AFC ensure the AFC pull in range is set to the desired value.
   (A value of half the IF bandwidth is recommended.)

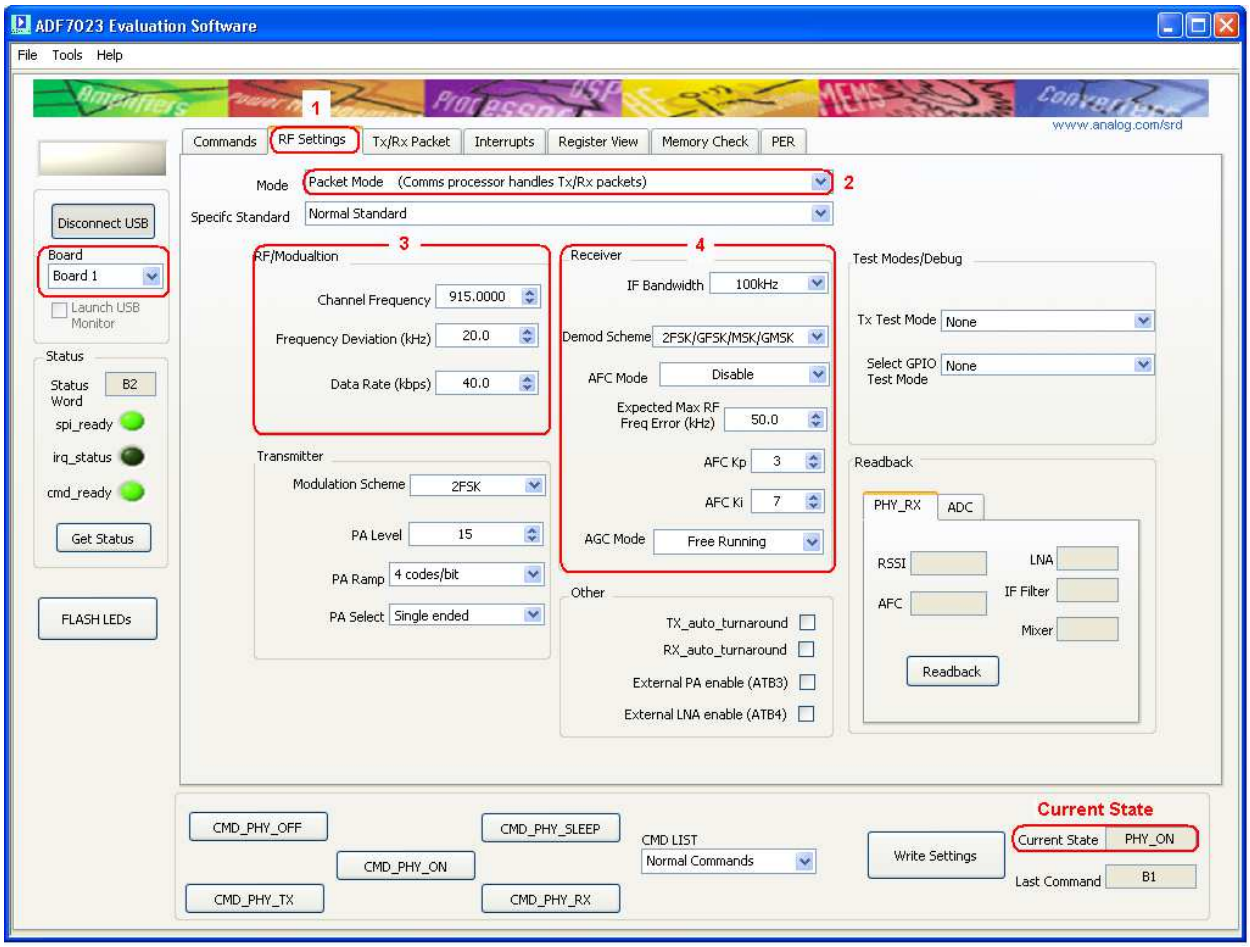



**Figure 31**

### *Receiver Board Rx Packet Settings*

Using the Tx/Rx packet tab you can set up the packet format and configure the packet handler. (Figure 32point (*1*))

1. The transmitted preamble length sync word and CRC can be defined by the user. (Figure 32point (*2*))
   (Note: Ensure CRC is enabled for this test. You have the choice to use the default CRC or enable a programmable CRC whose polynomial may be set in registers 0x11E and 0x11F.)

2. Ensure you are using a fixed packet length and that, "***Packet Length Max***" is set equal the payload length. (Figure 32point (*3*))

3. Set up the Rx base address. (Figure 32point (*4*))
   (Note : This is the start address of the received packet in Packet Ram Memory.)

4. Write the settings to the device using the "***Update Needed***" button. (Figure 32point (*5*))

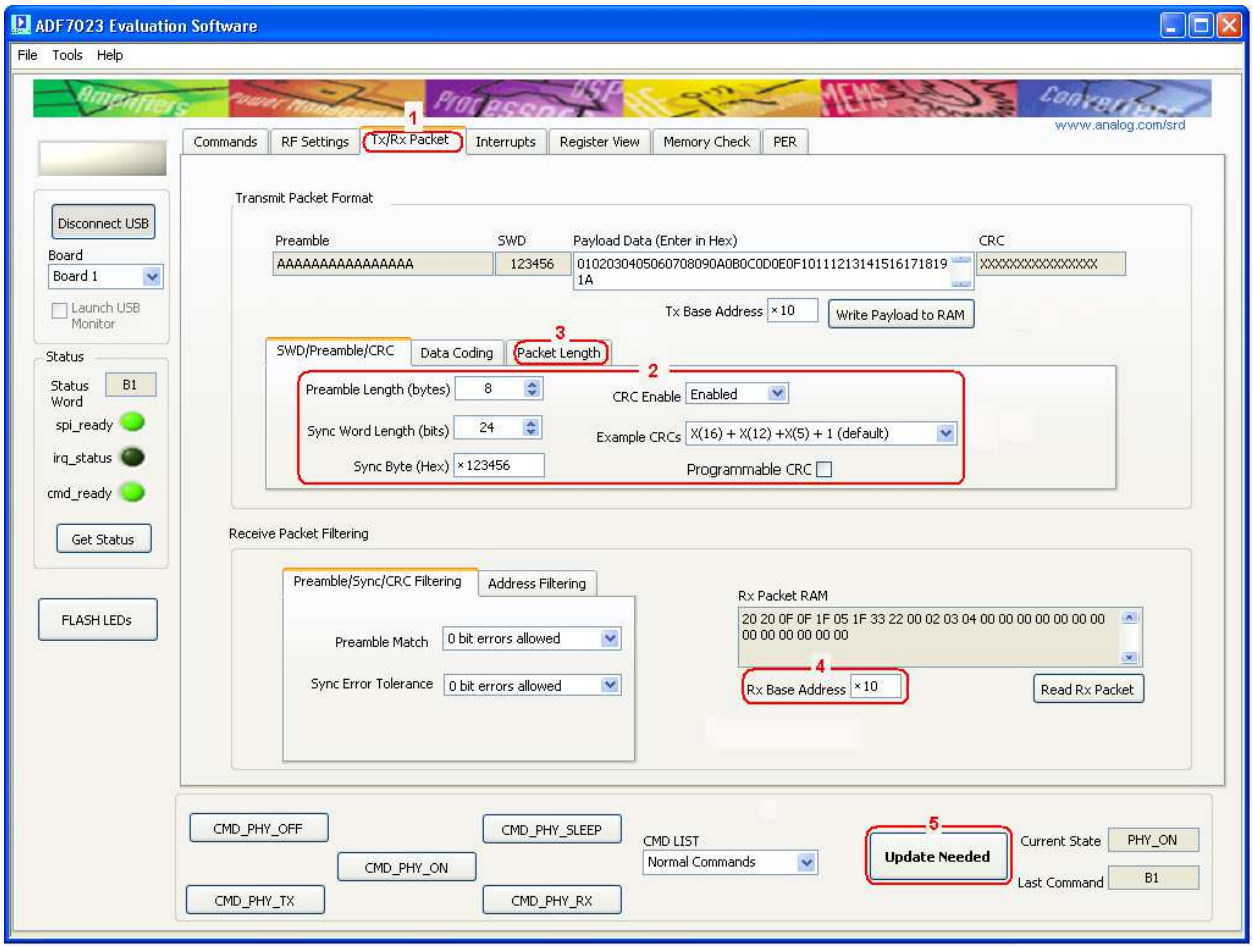



**Figure 32**

### *Receiver Board Interrupts*

Interrupts may be configured for various conditions in the "***Interrupts"*** tab. (Figure 33 point (***1***))

1. Set the "***crc_correct***" interrupt. (Figure 33 point (***2***))
   This will give an interrupt signal upon reception of a packet with a valid CRC.

2. Write the settings to the device using the "***Update Needed***" button. (Figure 33 point (***3***))

3. Put the part into Receive by pressing "***CMD_PHY_RX***" (Figure 33 point (***4***))
   (Note: Ensure that the current state of the part is in "***PHY_ON***" before pressing "***CMD_PHY_RX***".)

"***Board 1***" is now in Receive and waits for a transmitted signal. It will remain in Rx until a valid packet with a valid CRC is received.

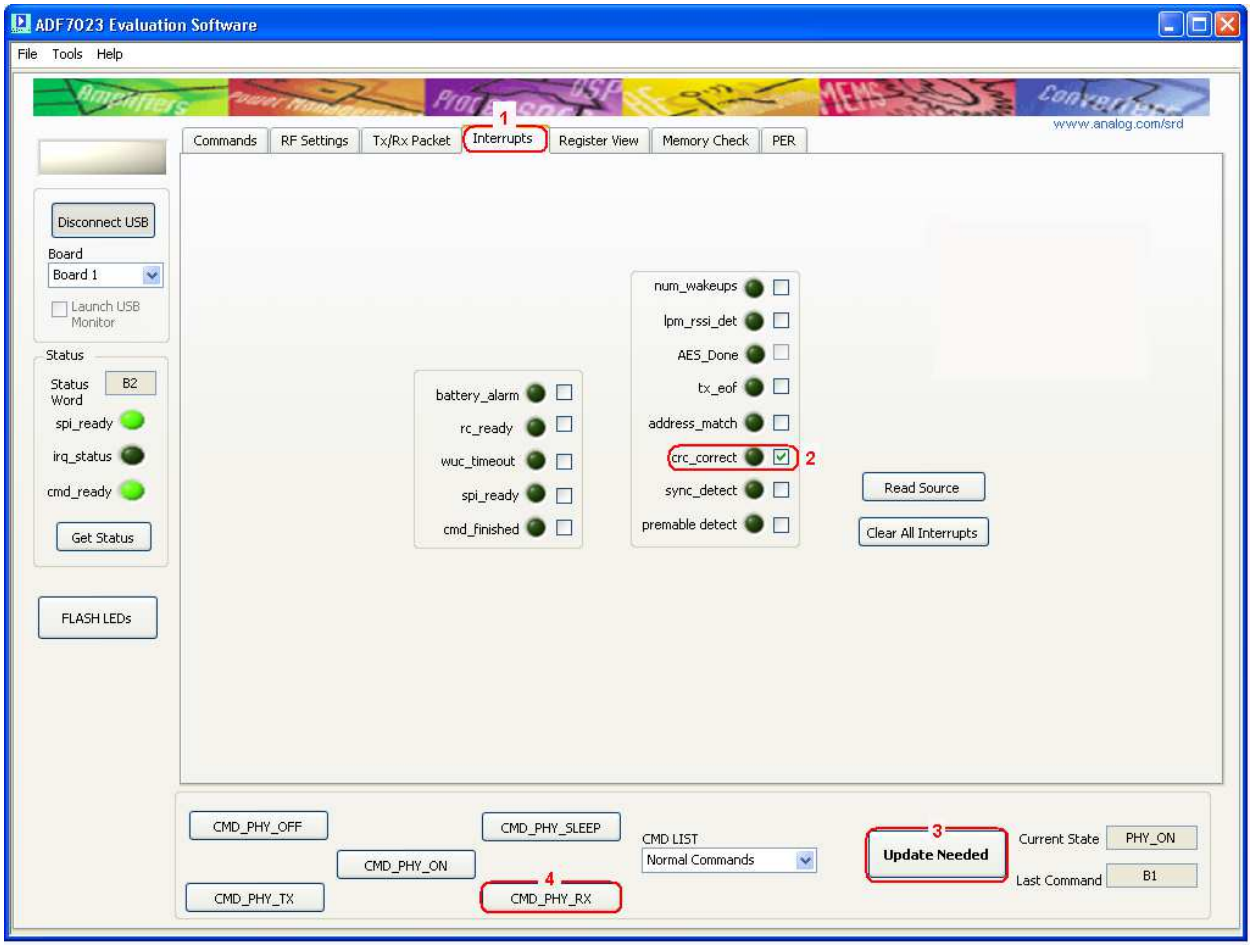



**Figure 33**

## *Tx Setup in Packet Mode*

The settings which follow are for use with EVAL-ADF7023DB1z daughter boards. If you are using a different Daughter board, ensure that the frequency is set within the correct range of the board you are using. Please refer to table x if you are unsure what the frequency range of you board is designed for.

### *Transmitter Board RF Settings*

1. Ensure the **Second** ADF7023 Daughter board is correctly plugged into the **Second** Mother board and that the "**Current_State**" is "***PHY_ON***" on the **Second** instance of the ADF7023 Software.
   Refer to **Connecting the Evaluation Boards** section for setup procedures.

2. Select the "***RF Settings***" Tab (Figure 34 point (***1***))

3. Ensure "***Packet mode***" is selected. (Figure 34 point (***2***))

4. Set the "***RF/Modulation"*** parameters as required. (Figure 34 point (***3***))
   (Note : Ensure the **Transmitter *RF/Modulation*** parameters are the same as the **Receiver *RF/Modulation*** parameters previously setup).

5. Set the "***Transmitter"*** parameters as required. (Figure 34 point (***4***))

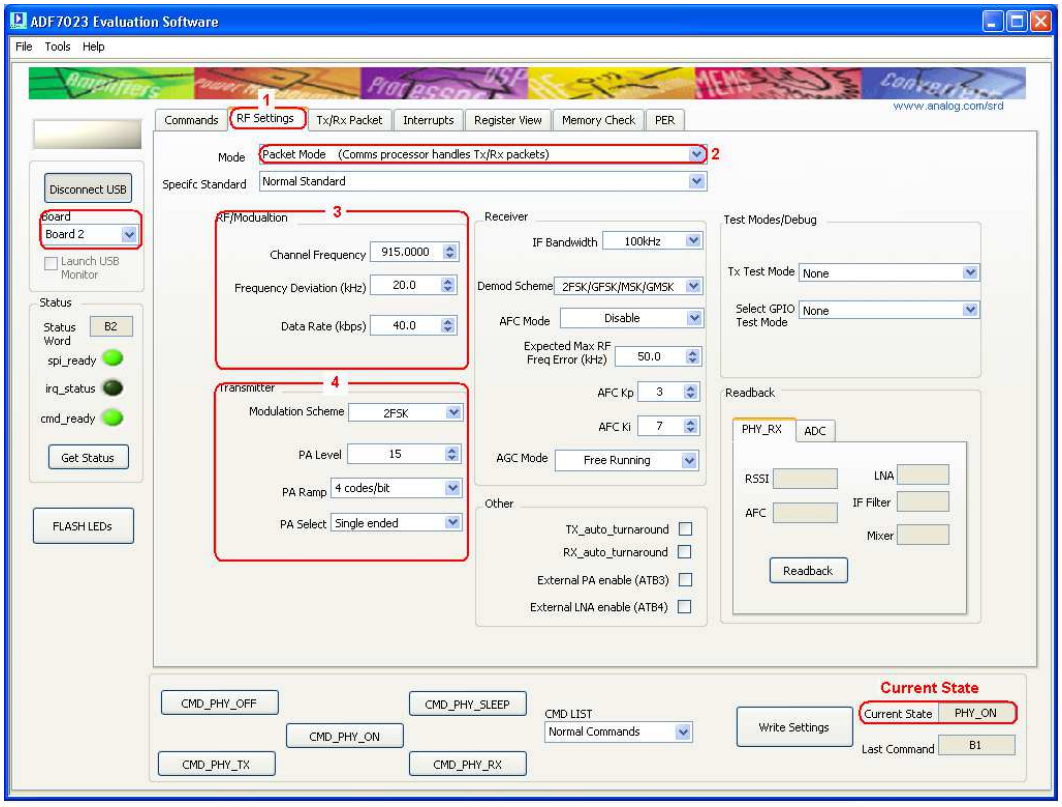



Figure 34

### *Transmitter Board Tx Packet Settings*

Using the Tx/Rx packet tab you can set up the packet format and configure the packet handler. Ensure these settings are the same as the Receiver settings previously set. (Figure 35 point (*1*))

1. The transmitted preamble length sync word and CRC can be defined by the user. (Figure 35 point (*2*))
   (Note: Ensure CRC is enabled for this test. You have the choice to use the default CRC or enable a programmable CRC whose polynomial may be set in registers 0x11E and 0x11F.)

2. Ensure you are using a fixed packet length and that, "***Packet Length Max***" is set equal the payload length. (Figure 35 point (*3*))

3. Set up the Tx base address. (Figure 35 point (*4*))
   (Note : This is the start address of the Transmitted packet in Packet Ram Memory.)

4. Insert Hex data in the ***Payload Data*** field (Figure 35 point (*5*))
   then click "***Write Payload to RAM***" (Figure 35 point (*6*))

5. Write the settings to the device using the "***Update Needed***" button. (Figure 35 point (*7*))

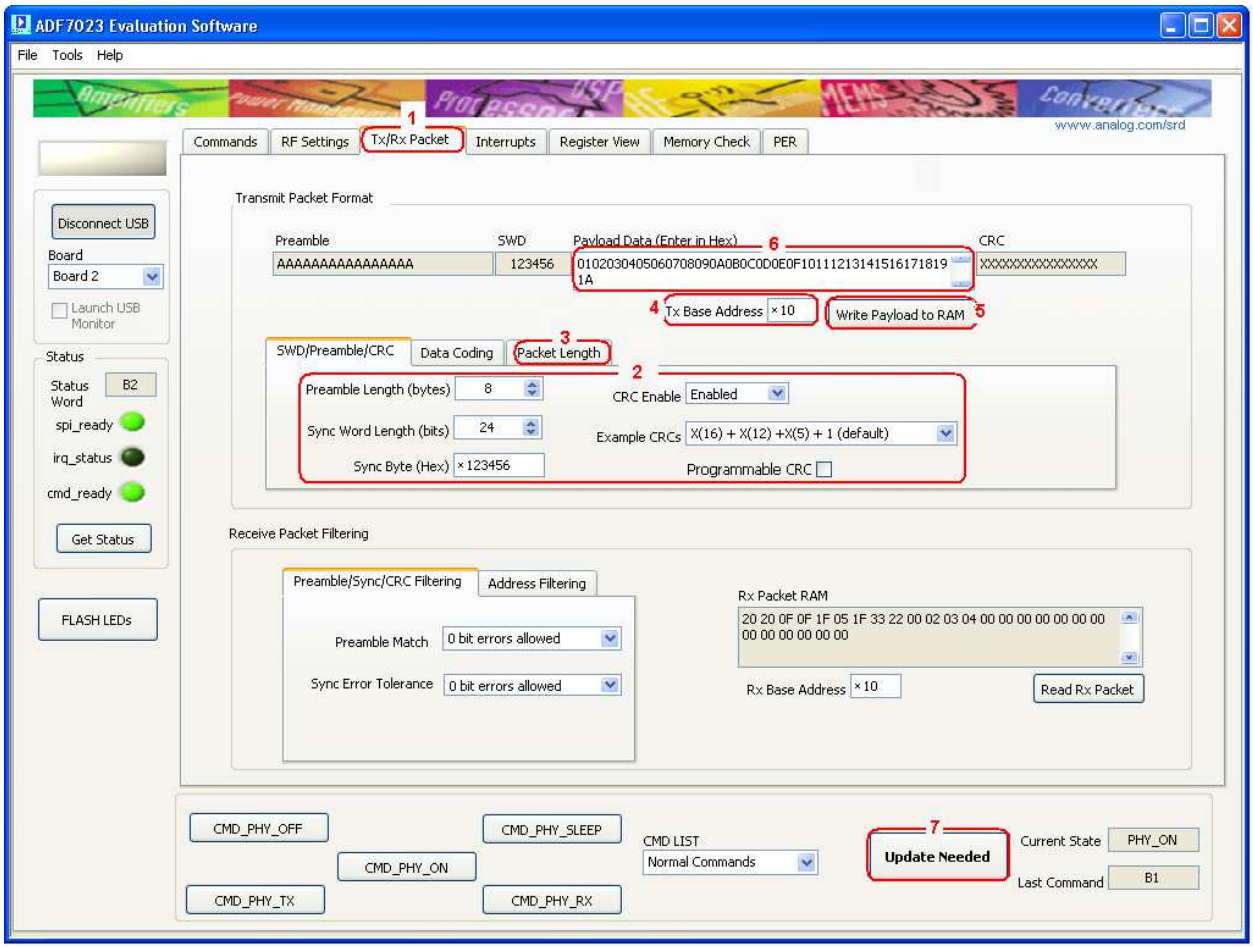



**Figure 35**

### *Transmitter Board Interrupts*

Interrupts may be configured for various conditions in the "***Interrupts"*** tab. (Figure 36point (***1***))

1. Set the "***tx_eof***" interrupt. (Figure 36point (***2***))
   This will give an interrupt signal after a packet has been fully transmitted.

2. Write the settings to the device using the "***Update Needed***" button. (Figure 36point (***3***))

3. Transmit a packet by clicking "***CMD_PHY_TX***" (Figure 36point (***4***))
   (Note: Ensure that the current state of the part is in "***PHY_ON***" before pressing "***CMD_PHY_TX***".)

"***Board 2***" is now in Transmit and once a packet is transmitted the part returns to the ***PHY_ON*** state.

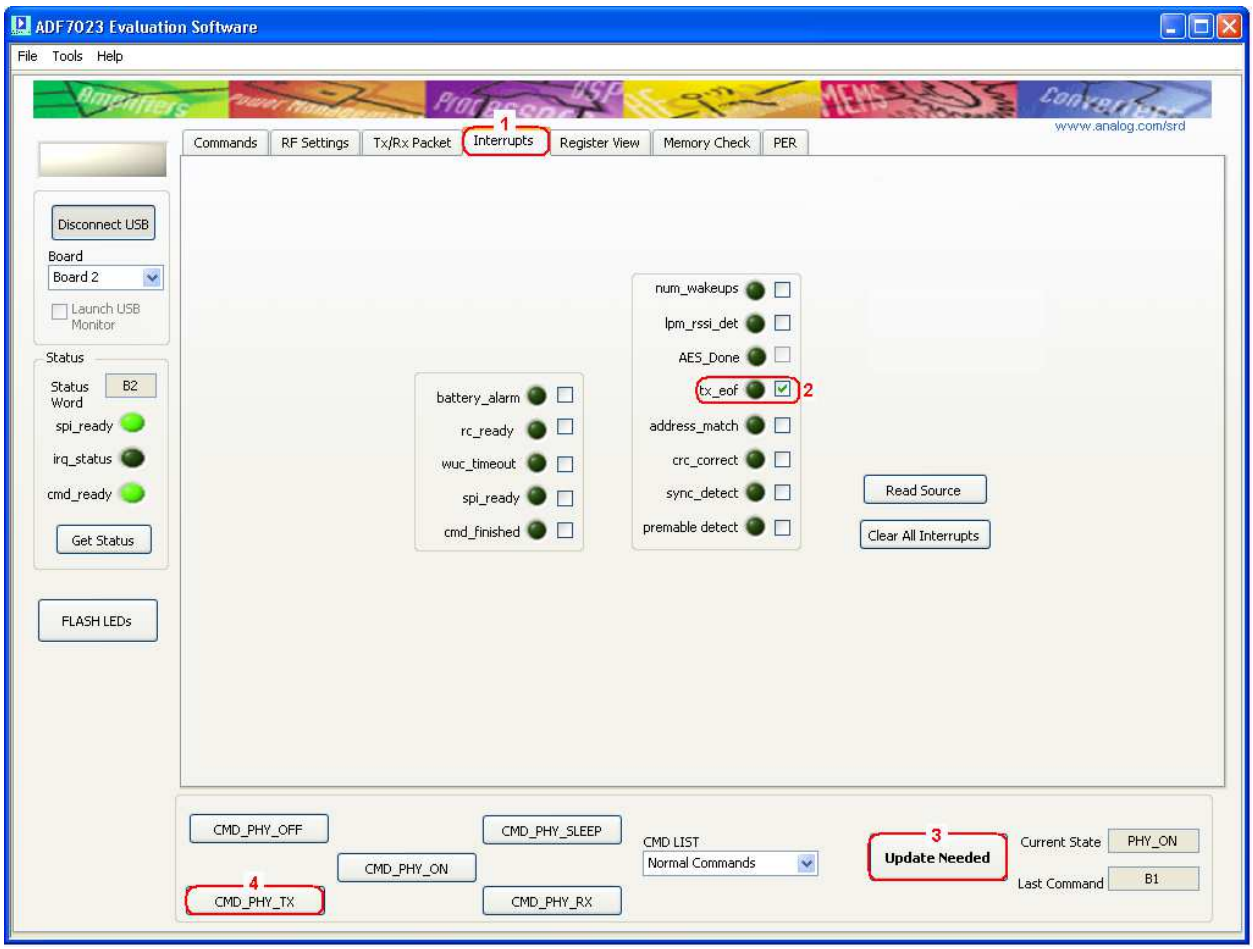



**Figure 36**

## *Reading Interrupt Source on Transmitter board*

Once the Transmitter has transmitted a packet you should now see "Interrupt Detected!" on both instances of the software. (Figure 37 point (***1***))

On the Transmitter board the interrupt signifies that a packet has been successfully transmitted. To check the source of the interrupt, click "***Read Source***" (Figure 37 point (***2***)

To Clear the interrupt status click "***Clear All Interrupts***" (Figure 37 point (***3***))

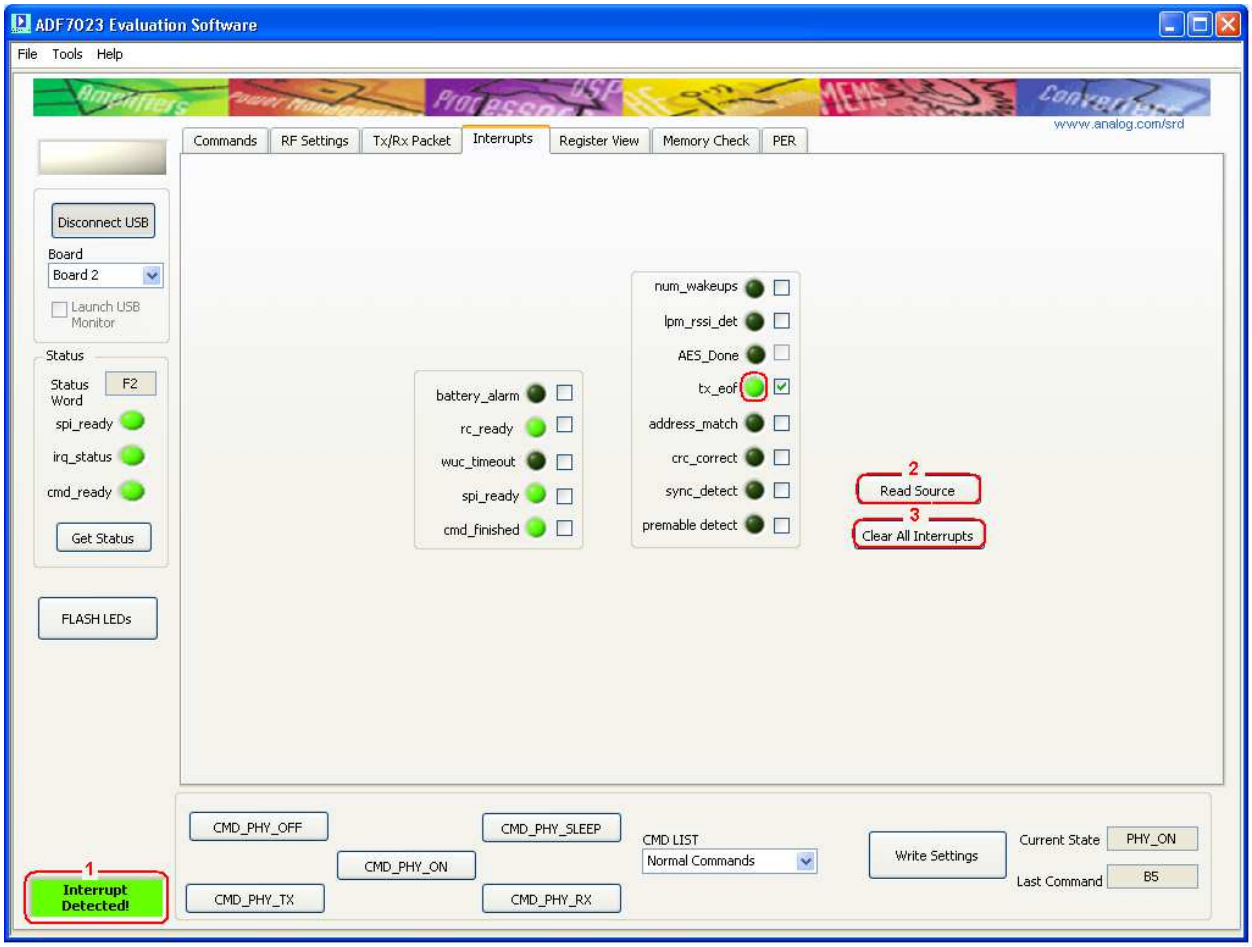



**Figure 37**

## *Reading Interrupt Source on Receiver board*

Once the Transmitter has transmitted a packet you should now see "Interrupt Detected!" on the Receiver software instance. (Figure 38 point (***1***))

On the Receiver board the interrupt signifies that a packet has been successfully Received with a valid CRC.
To check the source of the interrupt, click "***Read Source***" (Figure 38 point (***2***))

To Clear the interrupt status click "***Clear All Interrupts***" (Figure 38 point (***3***))

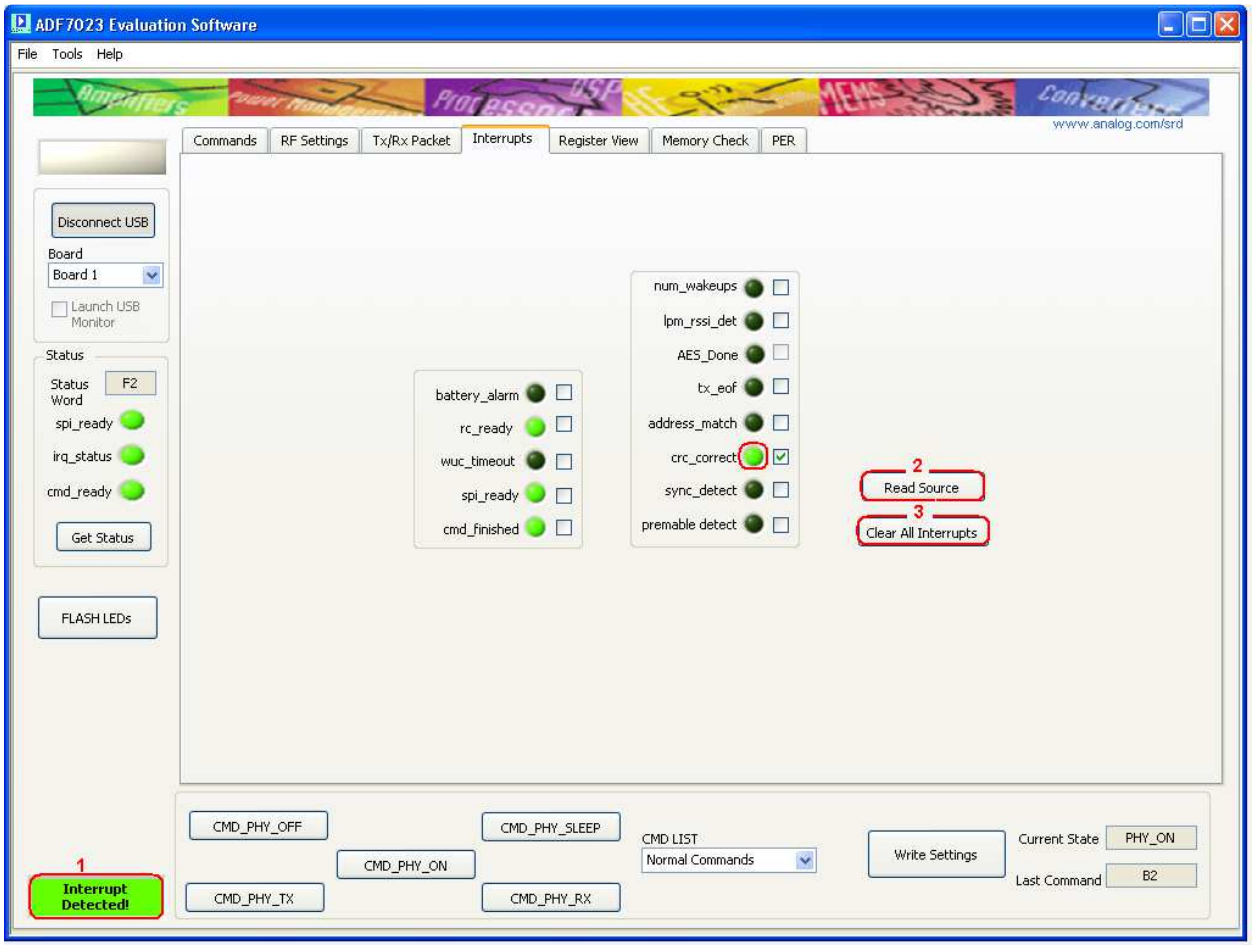



**Figure 38**

## *Running a Packet Error Rate Test*

To run a packet error rate test the previous section, Simple Rx / Tx Test in Packet Mode, must first be followed. Once interrupts are observed, on both the Rx and Tx software instances, the Packet Error Rate (PER) test may be used.

### *Configuring the Receiver board for the PER test*

1. Once all of the Receiver and packet parameters are setup correctly (as in ***Rx Setup in Packet Mode*** section) then select the "***PER***" Tab. (Figure 39 point (***1***))

2. Select the "***Rx Board Setup***" Tab (Figure 39 point (***2***))

3. Set the number of packets to be received, "***No. of Packets to Rx***" (Figure 39 point (***3***))

4. Write these settings to the uC by clicking "***Write Rx Settings***" (Figure 39 point (***4***))

5. To begin the test and put the receiver into Rx click "***Begin PER Rx***" (Figure 39 point (***5***))
   (Note: The receiver will remain in Rx waiting for a packet to be transmitted from a valid transmitter.)

6. If at any time you wish to terminate the test manually press "***Stop Test***". (Figure 39 point (***6***))
   (Note: The test will stop automatically once it receives the final transmitted packet.)

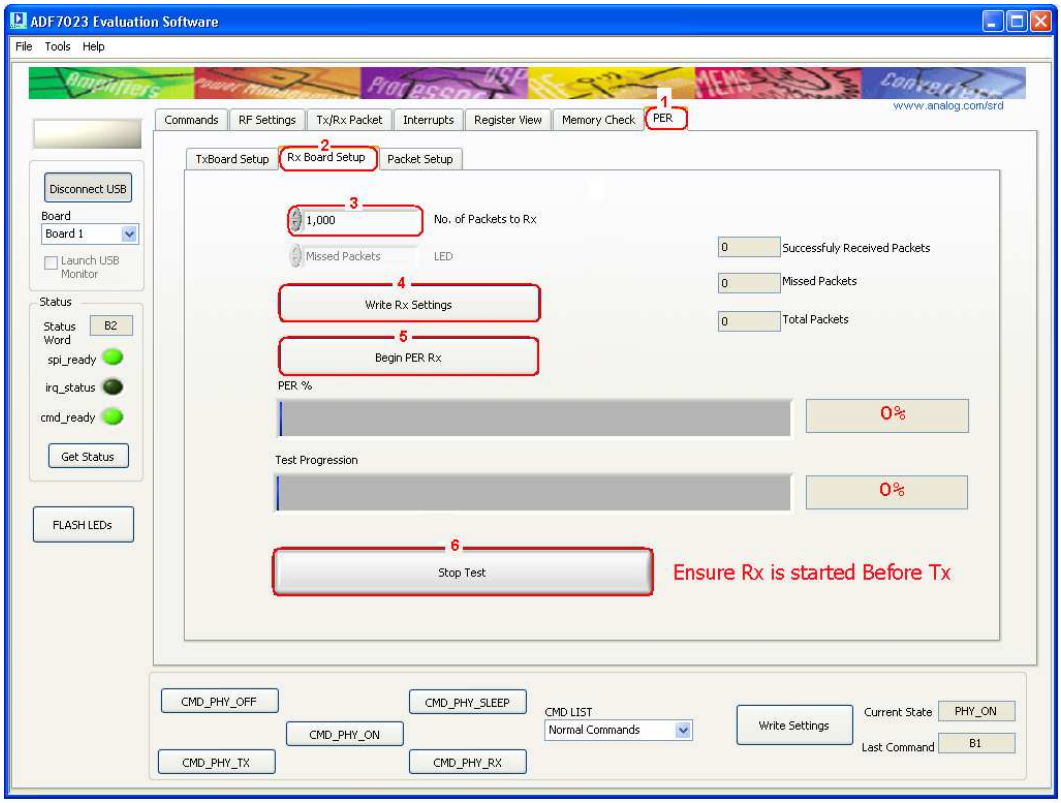



**Figure 39**

### *Configuring the Transmitter board for the PER test*

1. Once all of the Transmitter and packet parameters are setup correctly (as in *Tx Setup in Packet Mode* section) then select the "***PER***" Tab. (Figure 40 point (***1***))

2. Select the "***Tx Board Setup***" Tab (Figure 40 point (***2***))

3. Set the number of packets to be received, "***No. of Packets to Tx***" (Figure 40 point (***3***))
   (Note: Ensure the number of packets on the Receive and Transmit side are set the same.)

4. Set the delay between each transmitted packet from the "***Delay Between Packets***" dropdown menu. (Figure 40 point (***4***))

5. Write these settings to the uC by clicking "***Write Tx Settings***" (Figure 40 point (***5***))

6. To begin the test and put the receiver into Tx click "***Begin PER Tx***" (Figure 40 point (***5***))
   (Note: The transmitter will continuously transmit packets until "***No. of Packets to Tx***" value is reached.)

7. If at any time you wish to terminate the test manually press ***"Stop Test***". (Figure 40 point ***(6***))
   (Note: The test will stop automatically once the transmitter has transmitted the final packet.)

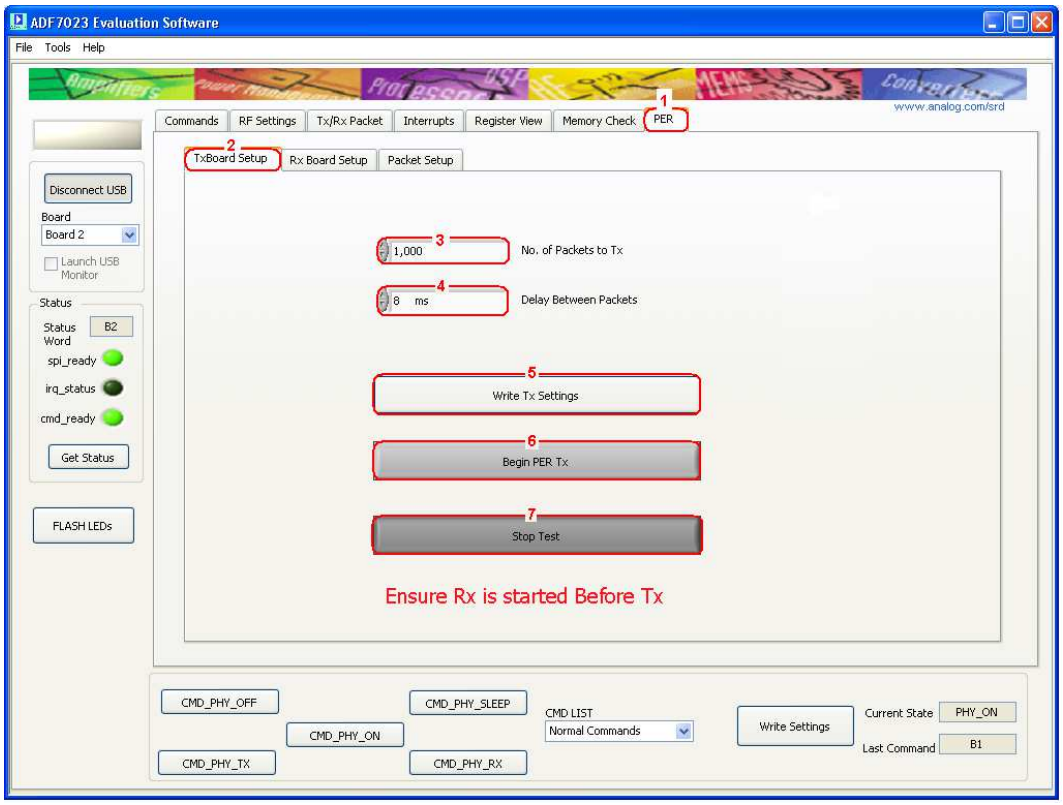



**Figure 40**

## *Running a Script*

1. Select "***Run Script***" from the "***CMD LIST***" drop down menu as shown in *Figure 41*Figure 41.

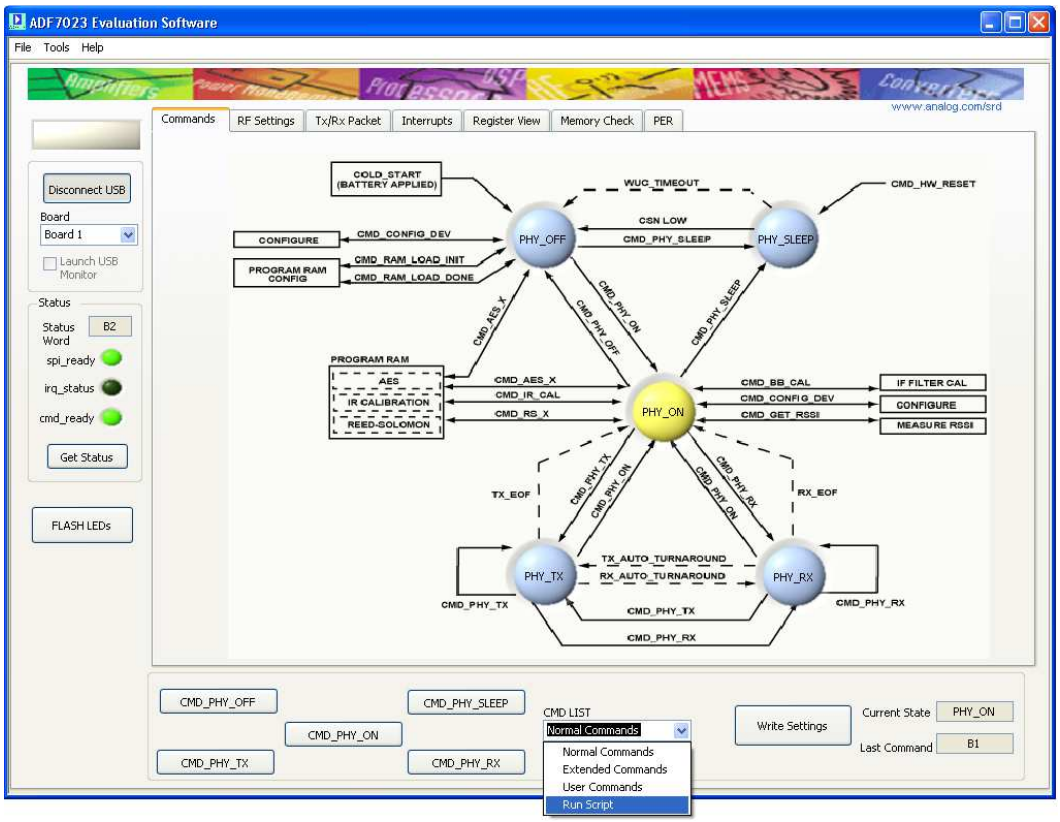



**Figure 41**

2. Select the path where the script file is stored. (Figure 42Figure 40 point (***1***))

3. Click "***Execute Script***" to run the selected script. (Figure 42Figure 40 point (***2***)

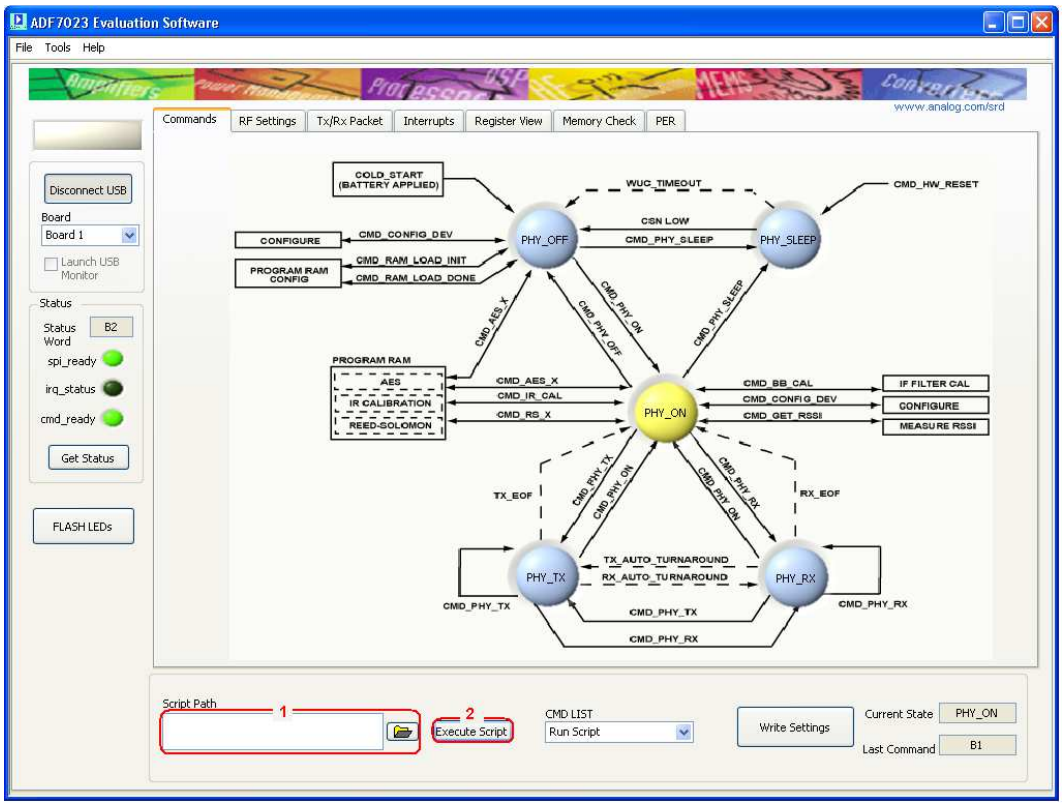



**Figure 42**

***Using Scripts***

Scripts can be written in Notepad and saved with a file extension of .txt

The following are examples can be used:

- To write to a PACKET_RAM register enter the line “18xxyy” where “xx” represents the last eight bits of the address to be written to and “yy” represents the value to be stores at this address.
    - For Example if you need to write 0xAB to PACKET_RAM location 0x010, then the script code would be : 1810AB

- To write to a BBRAM register enter the line “19xxyy” where “xx” represents the last eight bits of the address to be written to and “yy” represents the value to be stores at this address.
    - For Example if you need to write 0xCD to BBRAM location 0x123, then the script code would be : 1923CD

- To write to a MCR register enter the line “1Bxxyy” where “xx” represents the last eight bits of the address to be written to and “yy” represents the value to be stores at this address.
    - For Example if you need to write 0xEF to MCR location 0x345, then the script code would be : 1B45EF

- To introduce a delay before the next script command enter the line “Sxxxx”. Where “xxxx” represents an integer multiple of 1ms.
    - For example to enter a delay of 120ms before the next command is to be issued then the script code would be: “S120”

- To issue a COMMAND enter the desired command.
    - For Example to enter “***PHY_OFF***”, then the script code would be : B1
    - For Example to enter “***PHY_ON***”, then the script code would be : B2
    - For Example to enter “***PHY_TX***”, then the script code would be : B5

- To introduce comments in the file use “//” before the comment.

**Scripting Example**

The following script would be used for the previous examples:

```
//Start of script
1810AB          //Set Packet_Ram address 0x010 to AB
1923CD          //Set BBRam address 0x123 to CD
1B45EF          //Set MCR address 0x345 to EF
S120            //Delay for 120ms
B1              //Enter PHY_OFF
B2              //Enter PHY_ON
B5              //Enter PHY_Tx
//End of script
```

# ADF7023 Evaluation Board Schematics and BOMs

**Table 2 Components Common to All Daughter Boards**

| Qty | Name | Value | Tolerance | PCB Decal | Manufacturing Part No. |
|---|---|---|---|---|---|
| 1 | C1 | 1.5nF | ±5% | 0402 | GRM155R71H152KA01D |
| 9 | C14, C16, C24, C28, C30, C33, C37, C62, C65 | 220nF | ±10% | 0402 | GRM155R61A224KE19D |
| 2 | C15, C27 | 100pF | ±5% | 0402 | GRM1555C1H101JZ01D |
| 3 | C23, C34, C35 | 18pF | ±5% | 0402 | GRM1555C1H180JZ01D |
| 1 | C25 | 150nF | ±5% | 0402 | GRM155R61A154KE19D |
| 2 | C26, C42 | 10uF | ±20% | 0603 | 6R3R14X106MV4T |
| 2 | C39, C40 | 5.6pF | ±5% | 0402 | GRM1555C1H5R6DZ01D |
| 4 | R3, R4, R8, R9 | DNI | | | Not inserted |
| 1 | R12 | 36k | ±1% | 0402 | MCR01MZPF3602 |
| 1 | R15 | 100k | ±1% | 0402 | MCR01MZPF1003 |
| 1 | R16 | 1.1k | ±1% | 0402 | MCR01MZPF1101 |
| 1 | Y1 | 26MHz | | | NX3225SA-26.000000MHZ-G2 |
| 1 | Y2 | 32.768kHz | | | ABS07-32.768KHZ-7-T |
| 1 | U1 | | | LFCSP-32 | ADF7023 |

**Table 3 Eval-ADF7023DB1Z Components (868/915MHz Separate Matches)**

| **Qty** | **Name** | **Value** | **Tolerance** | **PCB Decal** | **Manufacturing Part No.** |
|---|---|---|---|---|---|
| 1 | C2 | 1pF | ±0.25pF | 0402 | GRM1555C1H1R0CA01D |
| 2 | C3, C5 | 2.2pF | ±0.25pF | 0402 | GRM1555C1H2R2CZ01D |
| 1 | C18 | 56pF | ±5% | 0402 | GRM1555C1H470JZ01D |
| 1 | C19 | 2.7pF | ±0.25pF | 0402 | GRM1555C1H2R7CZ01D |
| 1 | C20 | 1.2pF | ±0.25pF | 0402 | GRM1555C1H1R2CZ01D |
| 1 | C66 | 100pF | ±5% | 0402 | GRM1555C1H101JZ01D |

| | | | | | |
|---|---|---|---|---|---|
| 1 | C67 | 47pF | ±5% | 0402 | GRM1555C1H470JZ01D |
| 1 | L1 | 1.8nH | ±5% | 0402 | Coilcraft 0402CS-1N8XJL |
| 1 | L2 | 24nH | ±5% | 0402 | Coilcraft 0402CS-24NXJL |
| 1 | L3 | 12nH | ±5% | 0402 | Coilcraft 0402CS-12NXJL |
| 1 | L4 | 6.2nH | ±5% | 0402 | Coilcraft 0402CS-6N2XJL |
| 1 | L6 | 47nH | ±5% | 0402 | Coilcraft 0402CS-47NXJL |
| 2 | L5, L10 | 12nH | ±5% | 0402 | Coilcraft 0402CS-12NXJL |

**Table 4 Eval-ADF7023DB2Z Components (868/915MHz Combined Match)**

| Qty | Name | Value | Tolerance | PCB Decal | Manufacturing Part No. |
|---|---|---|---|---|---|
| 1 | C2 | DNI | | | Not Inserted |
| 2 | C3,C22 | 2.2pF | ±0.25pF | 0402 | GRM1555C1H2R2CZ01D |
| 1 | C18 | 56pF | ±5% | 0402 | GRM1555C1H470JZ01D |
| 2 | C19 | 2.7pF | ±0.25pF | 0402 | GRM1555C1H2R7CZ01D |
| 1 | C20 | 1.8pF | ±0.25pF | 0402 | GRM1555C1H1R8CZ01D |
| 1 | C66 | 100pF | ±5% | 0402 | GRM1555C1H101JZ01D |
| 1 | C67 | 47pF | ±5% | 0402 | GRM1555C1H470JZ01D |
| 1 | L1 | 1.8nH | ±5% | 0402 | Coilcraft 0402CS-1N8XJL |
| 3 | L2, L4, L9 | 12nH | ±5% | 0402 | Coilcraft 0402CS-11NXJL |
| 1 | L3 | 11nH | ±5% | 0402 | Coilcraft 0402CS-11NXJL |
| 1 | L6 | 47nH | ±5% | 0402 | Coilcraft 0402CS-47NXJL |
| 1 | L7 | 24nH | ±5% | 0402 | Coilcraft 0402CS-24NXJL |

**Table 5 Eval-ADF7023DB3Z Components (433MHz Separate Matches)**

| Qty | Name | Value | Tolerance | PCB Decal | Manufacturing Part No. |
|---|---|---|---|---|---|
| 1 | C2 | 1.2pF | ±0.25pF | 0402 | GRM1555C1H1R2CZ01D |
| 2 | C3, C5 | 3.9pF | ±0.25pF | 0402 | GRM1555C1H3R9CZ01D |
| 3 | C19, C20 | 5.6pF | ±0.25pF | 0402 | GRM1555C1H5R6DZ01D |

| | | | | | |
|---|---|---|---|---|---|
| 2 | C18, C67 | 270pF | ±5% | 0402 | GRM1555C1H271JA01D |
| 1 | C66 | 100pF | ±5% | 0402 | GRM1555C1H101JZ01D |
| 1 | L1 | 15nH | ±5% | 0402 | Coilcraft 0402CS-15NXJL |
| 1 | L2 | 82nH | ±5% | 0402 | Coilcraft 0402CS-82NXJL |
| 2 | L3, L4 | 27nH | ±5% | 0402 | Coilcraft 0402CS-27NXJL |
| 2 | L5, L10 | 33nH | ±5% | 0402 | Coilcraft 0402CS-11NXJL |
| 1 | L6 | 100nH | ±5% | 0402 | Coilcraft 0402CS-R10XJL |

**Table 6 Eval-ADF7023DB4Z Components (433MHz Combined Match)**

| Qty | Name | Value | Tolerance | PCB Decal | Manufacturing Part No. |
|---|---|---|---|---|---|
| 1 | C2 | DNI | | | Not Inserted |
| 1 | C3, C22 | 3.9pF | ±0.25pF | 0402 | GRM1555C1H3R9CZ01D |
| 2 | C18, C67 | 270pF | ±5% | 0402 | GRM1555C1H271JA01D |
| 1 | C19 | 4.7pF | ±0.1pF | 0402 | GRM1555C1H4R7BA01D |
| 1 | C20 | 2.7pF | ±0.1pF | 0402 | GRM1555C1H2R7BA01D |
| 1 | C66 | 100pF | ±5% | 0402 | GRM1555C1H101JZ01D |
| 1 | L1 | 13nH | ±5% | 0402 | Coilcraft 0402CS-13NXJL |
| 1 | L2, L9 | 33nH | ±5% | 0402 | Coilcraft 0402CS-33NXJL |
| 1 | L3 | 30nH | ±5% | 0402 | Coilcraft 0402CS-30NXJL |
| 1 | L4 | 41nH | ±5% | 0402 | Coilcraft 0402CS-41NXJL |
| 1 | L6 | 100nH | ±5% | 0402 | Coilcraft 0402CS-R10XJL |
| 1 | L7 | 82nH | ±5% | 0402 | Coilcraft 0402CS-82NXJL |

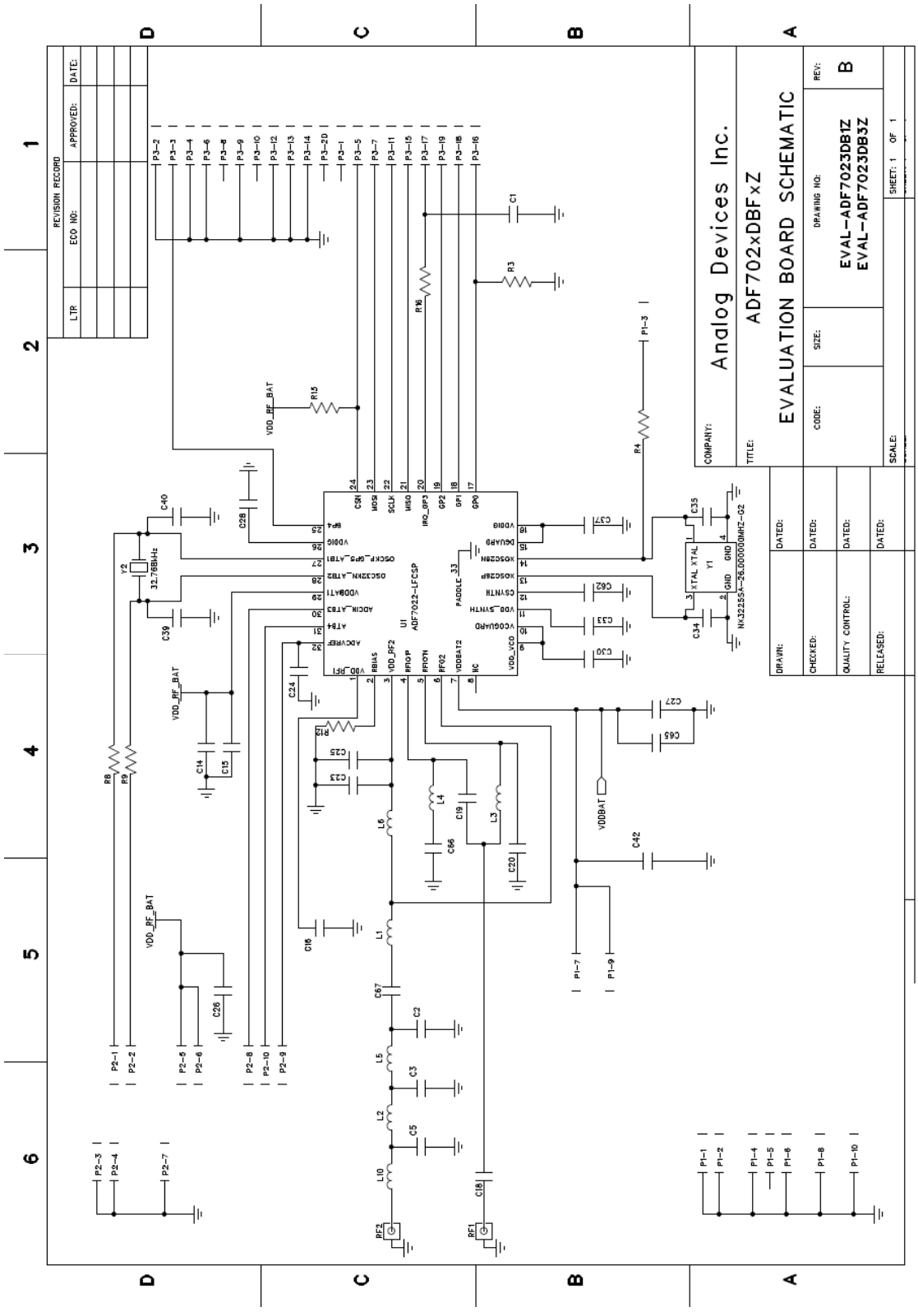



**Figure 43 Separate PA and LNA Matches Board Schematic (DB1Z, DB3Z)**

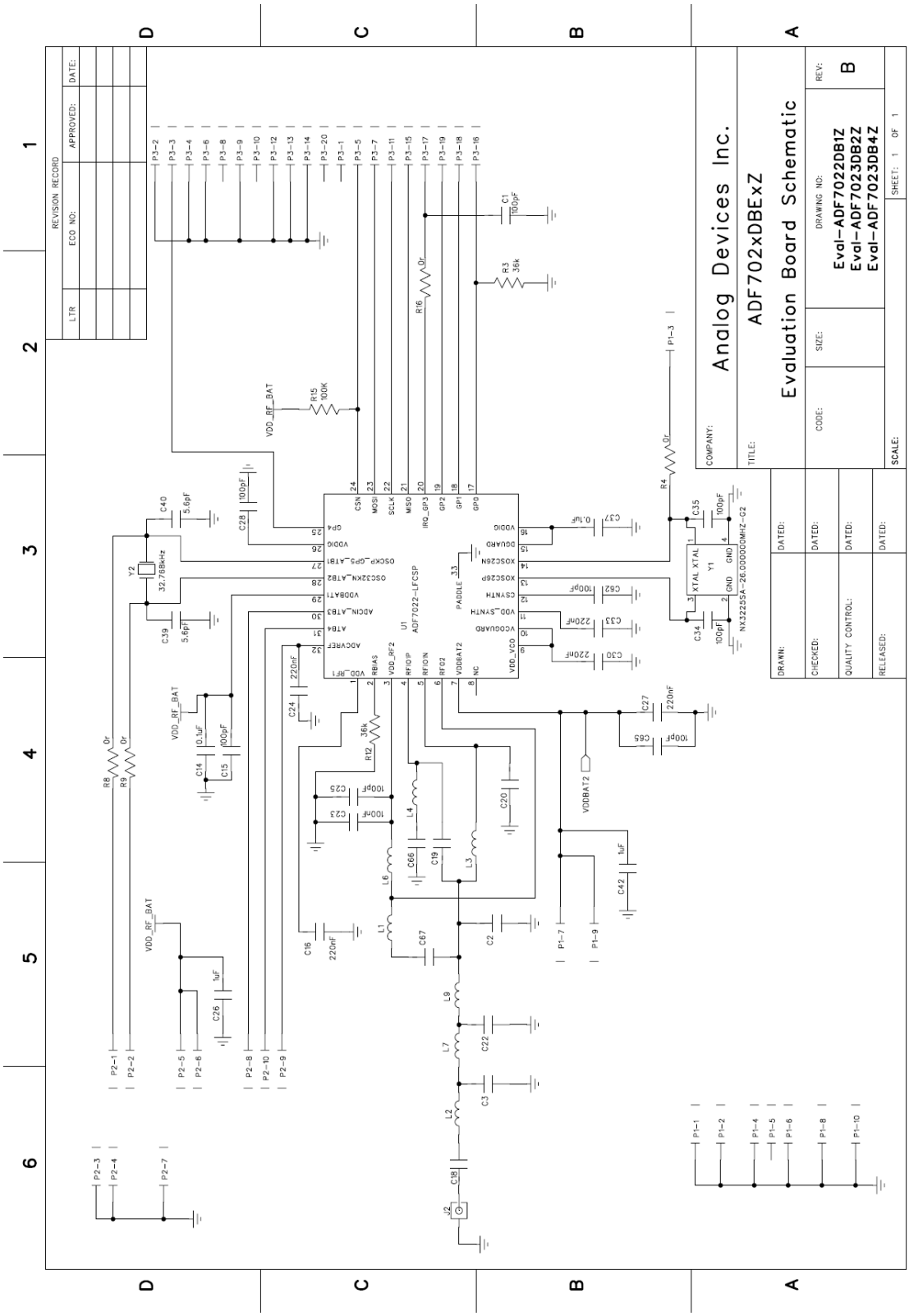



**Figure 44 Combined PA and LNA Match Board Schematic (DB2Z, DB4Z)**

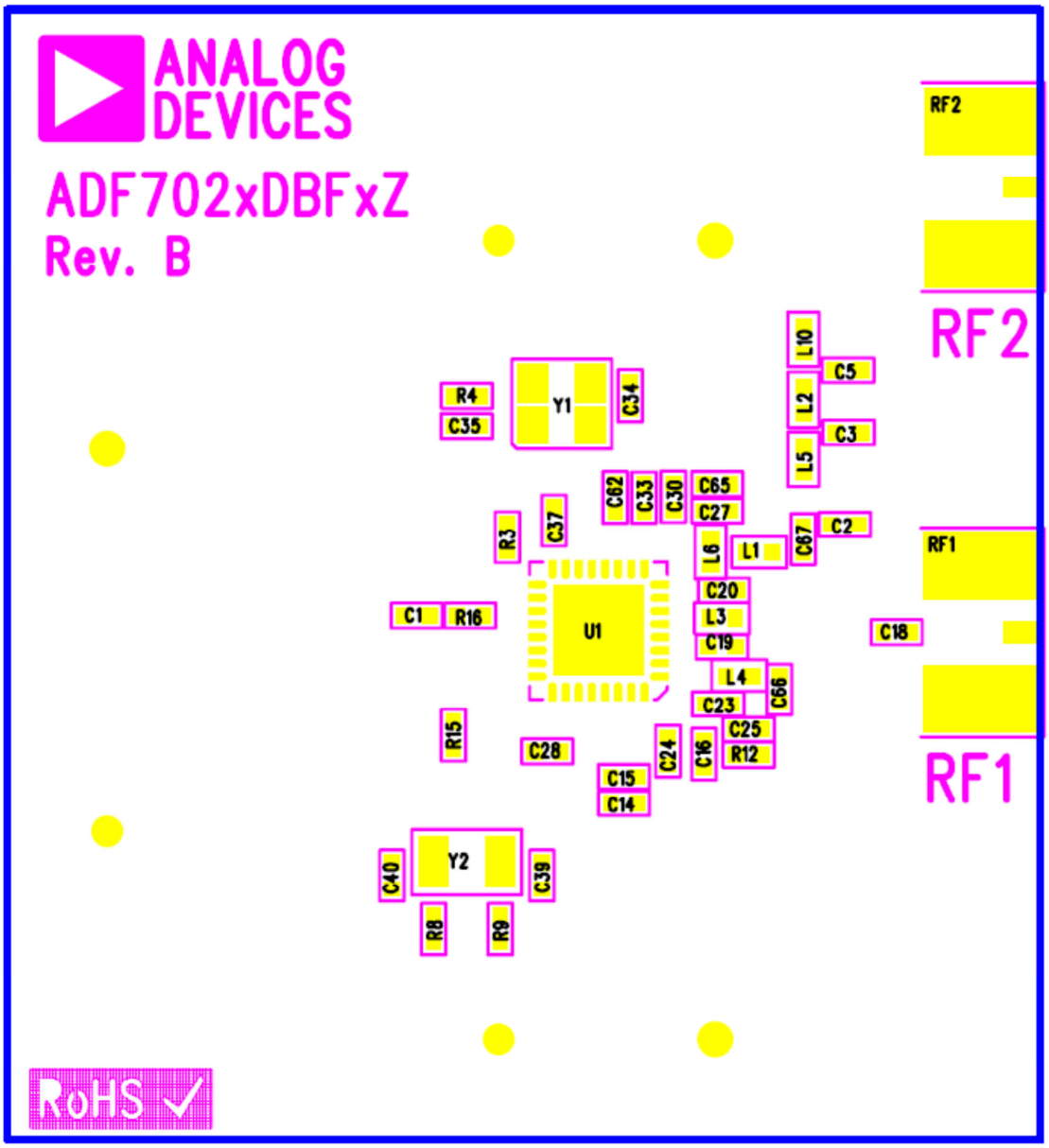



**Figure 45 Separate PA and LNA Matches Board Silkscreen (DB1Z, DB3Z)**

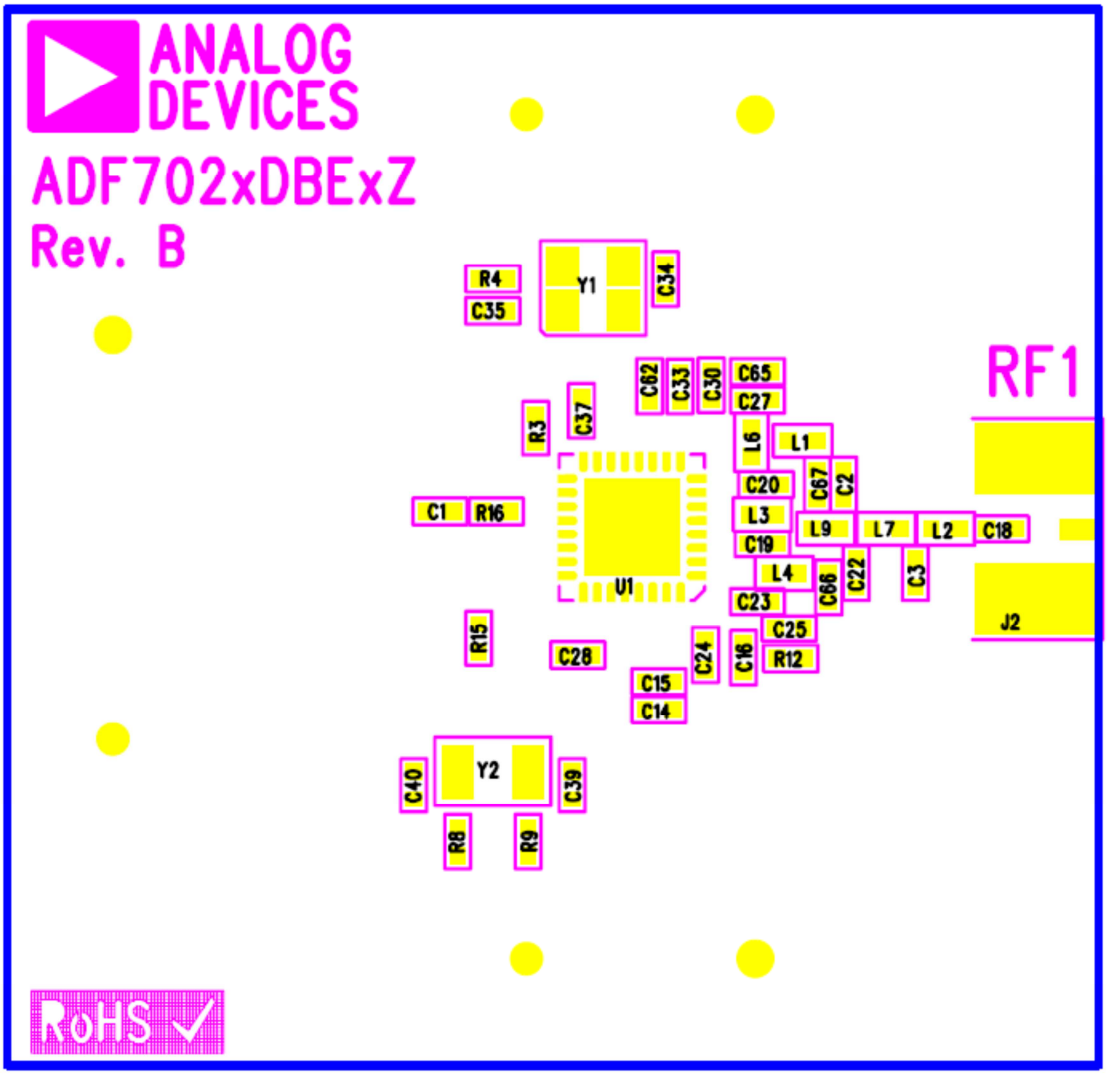



**Figure 46 Combined PA and LNA Match Board Silkscreen (DB2Z, DB4Z)**

# Eval-ADF7XXXMB3Z Mother Board Schematics and Silk Screen

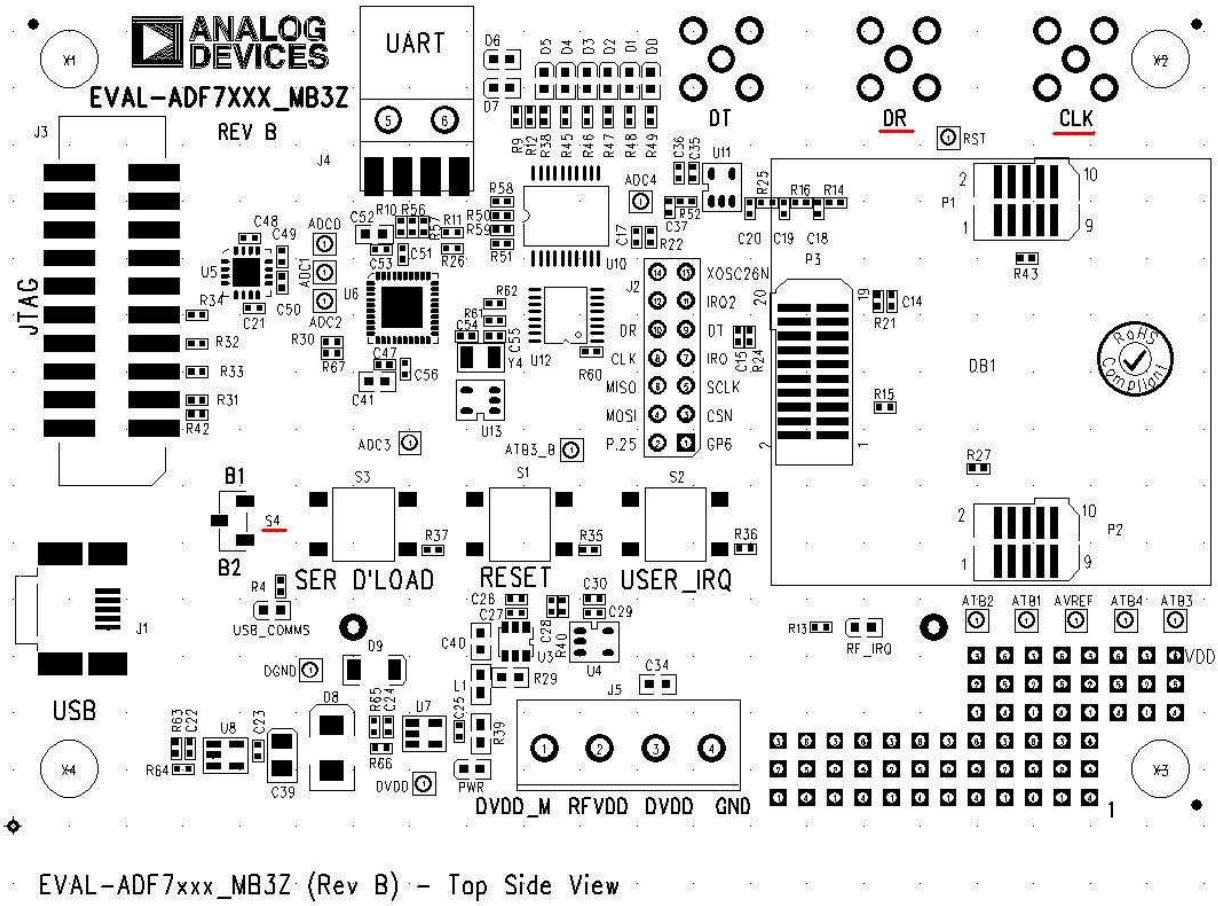



**Figure 47 Mother Board Silkscreen**

ADF7xxxMB3Z RevB.sch-3 - Thu Sep 30 14:09:50 2010