C2M0040120D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	1200 V
I_D @ 25˚C	55 A
$R_{DS(on)}$	40 mΩ

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

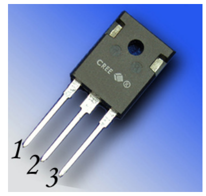
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

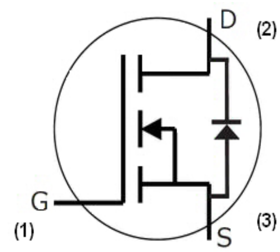
Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drives
- Pulsed Power Applications

Package



TO-247-3



Part Number	Package	Marking
C2M0040120D	TO-247-3	C2M0040120

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	55	A	V_{GS} = 20 V, T_C = 25˚C	Fig. 19
		36		V_{GS} = 20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	278	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.2	4	V	V_{DS} = V_{GS} , I_D = 10mA	Fig. 11
			2.4		V	V_{DS} = V_{GS}, I_D = 10mA,T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		44	52	mΩ	V_{GS} = 20 V, I_D = 40 A	Fig. 4,5,6
			82			V_{GS} = 20 V, I_D = 40 A, T_J = 150 °C	
g_{fs}	Transconductance		18.2		S	V_{DS}= 20 V, I_{DS}= 40 A	Fig. 7
			17.2			V_{DS}= 20 V, I_{DS}= 40 A, T_J = 150 °C	
C_{iss}	Input Capacitance		2440		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		171				
C_{rss}	Reverse Transfer Capacitance		11				
E_{oss}	C_{oss} Stored Energy		89		μJ		Fig 16
E_{ON}	Turn-On Switching Energy (Body Diode)		1.7		mJ	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 40A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		0.4				
E_{ON}	Turn-On Switching Energy (External SiC Diode)		1.3			V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 40A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH	
E_{OFF}	Turn Off Switching Energy (External SiC Diode)		0.4				
$t_{d(on)}$	Turn-On Delay Time		13		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 40 A $R_{G(ext)}$ = 2.5 Ω, R_L = 20 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		61				
$t_{d(off)}$	Turn-Off Delay Time		25				
t_f	Fall Time		13				
$R_{G(int)}$	Internal Gate Resistance		1.8		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		34		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 40 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		42				
Q_g	Total Gate Charge		120				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.0		V	V_{GS} = - 5 V, I_{SD} = 20 A, T_J = 25 °C	Fig. 8, 9, 10
		3.6		V	V_{GS} = - 5 V, I_{SD} = 20 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		60	A	T_C= 25 °C	Note 1
$I_{S, pulse}$	Diode Pulse Current		160	A	V_{GS} = - 5 V, Pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	54		ns	V_{GS} = - 5 V, I_{SD} = 40 A T_J = 25 °C VR = 800 V dif/dt = 1000 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	283		nC		
I_{rrm}	Peak Reverse Recovery Current	15		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.33	0.45	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

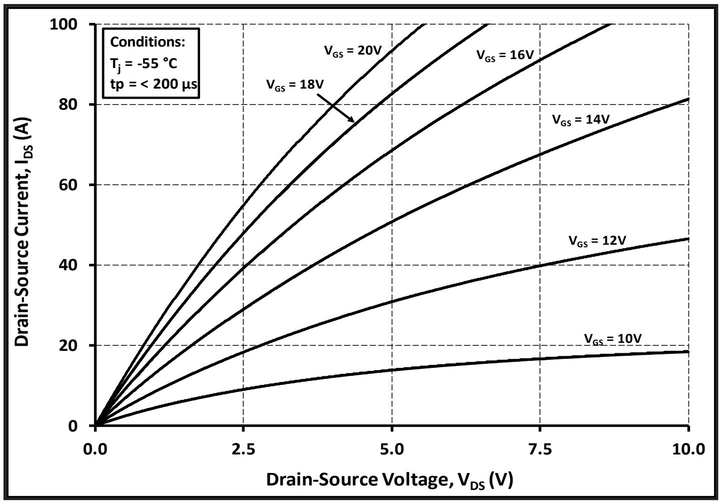


Figure 1. Output Characteristics T_J = -55 °C

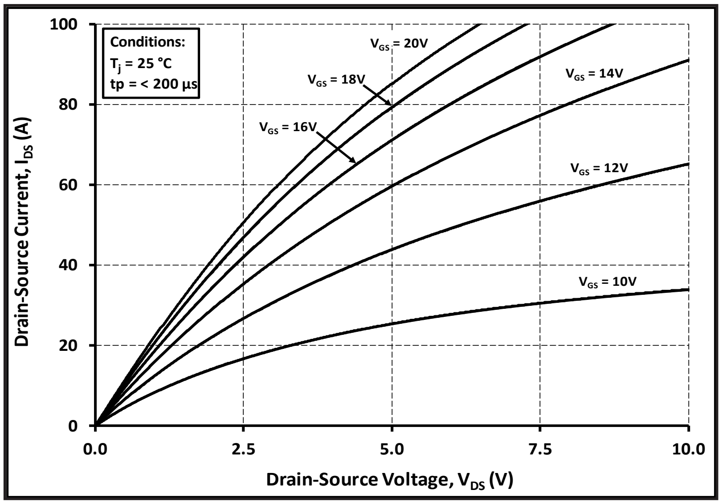


Figure 2. Output Characteristics T_J = 25 °C

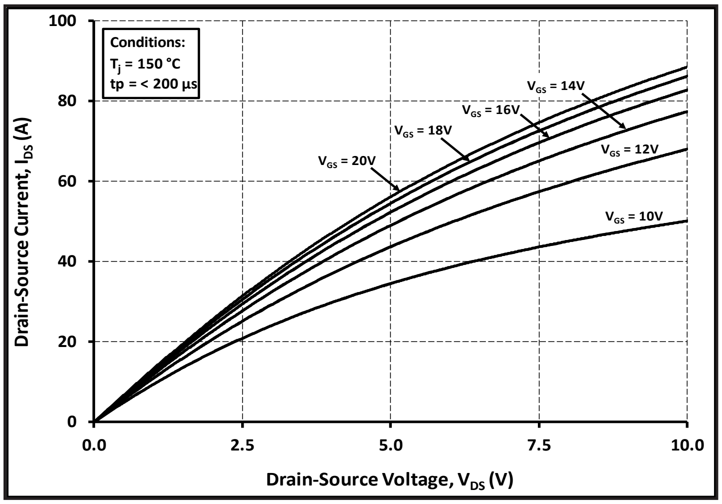


Figure 3. Output Characteristics T_J = 150 °C

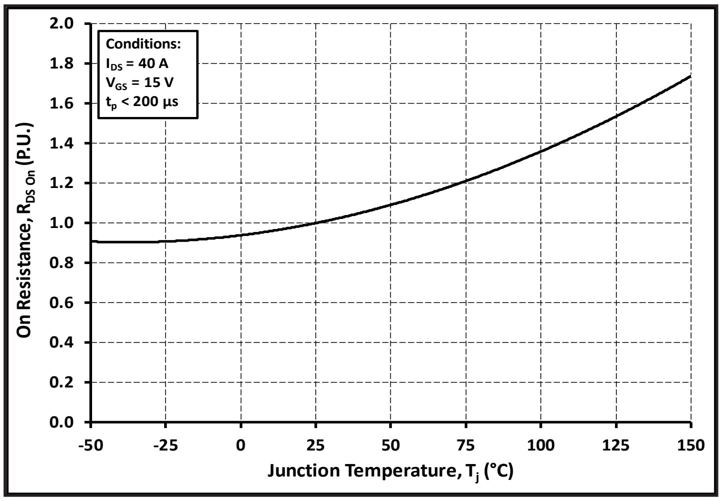


Figure 4. Normalized On-Resistance vs. Temperature

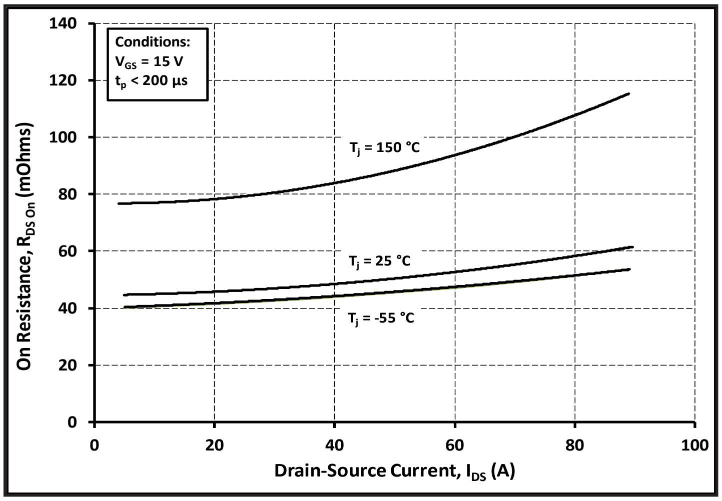


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

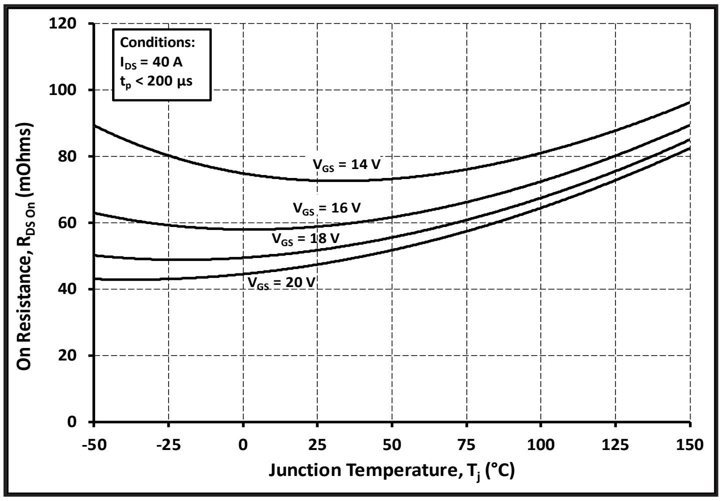


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

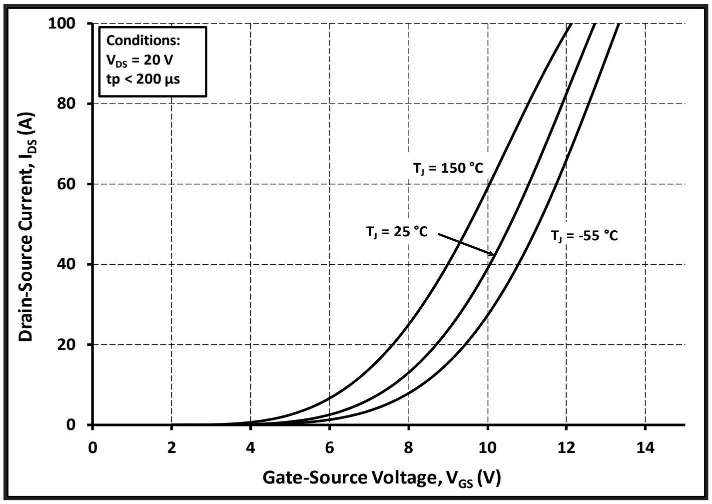


Figure 7. Transfer Characteristic for Various Junction Temperatures

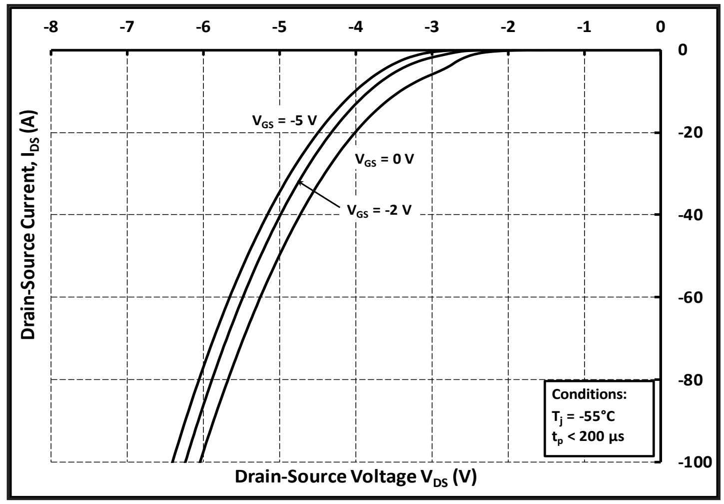


Figure 8. Body Diode Characteristic at -55 °C

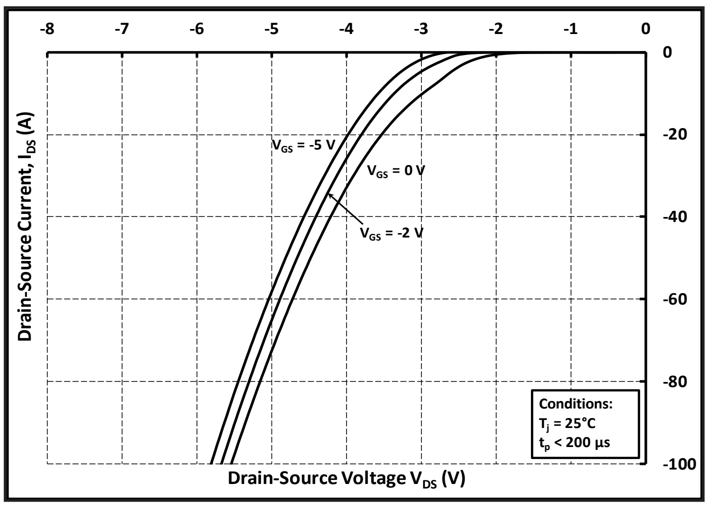


Figure 9. Body Diode Characteristic at 25 °C

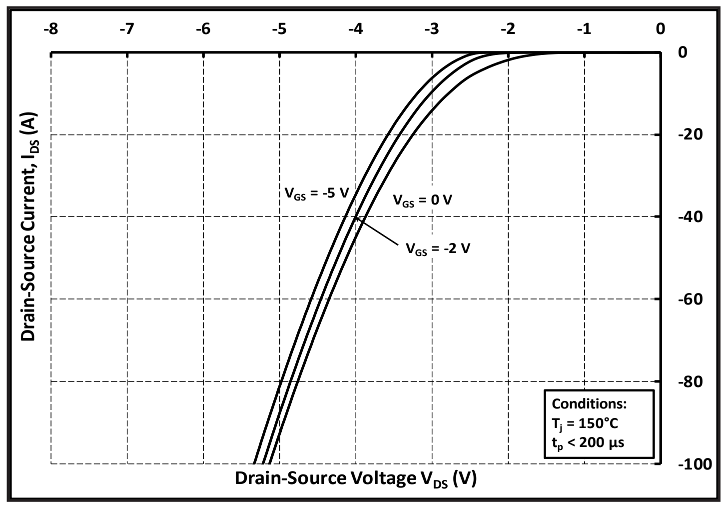


Figure 10. Body Diode Characteristic at 150 °C

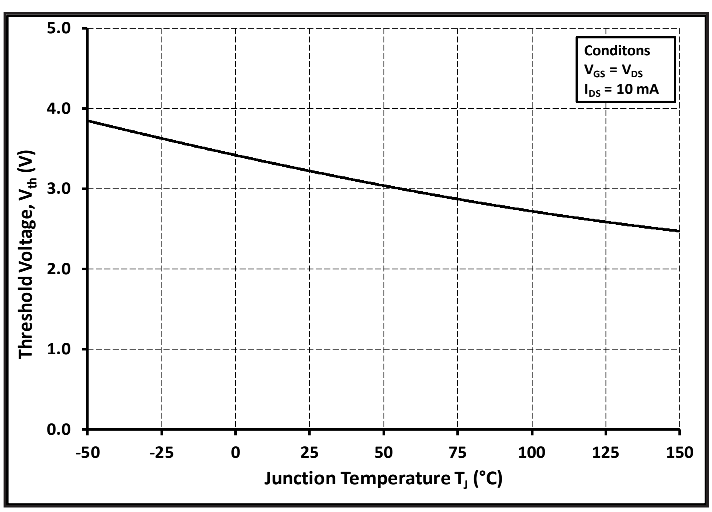


Figure 11. Threshold Voltage vs. Temperature

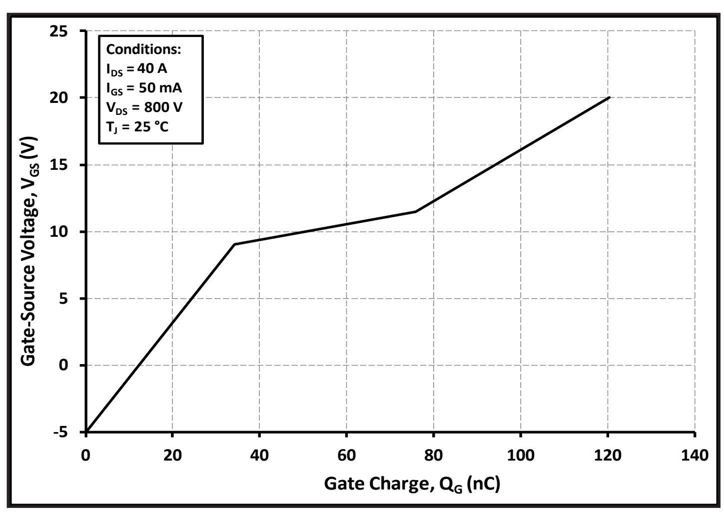


Figure 12. Gate Charge Characteristics

Typical Performance

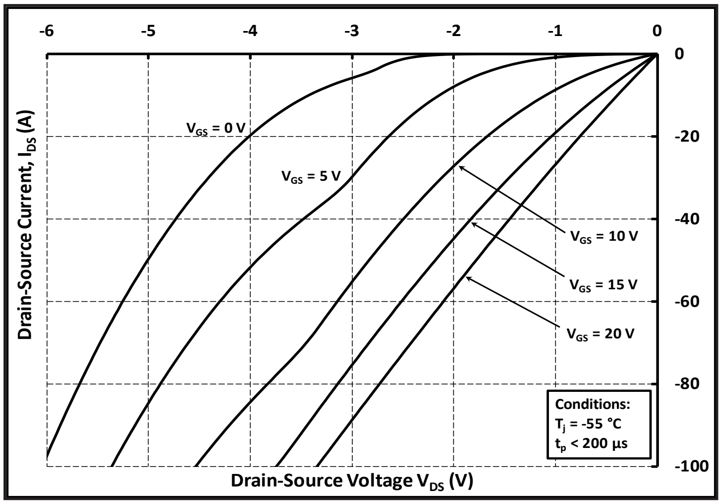


Figure 13. 3rd Quadrant Characteristic at -55 °C

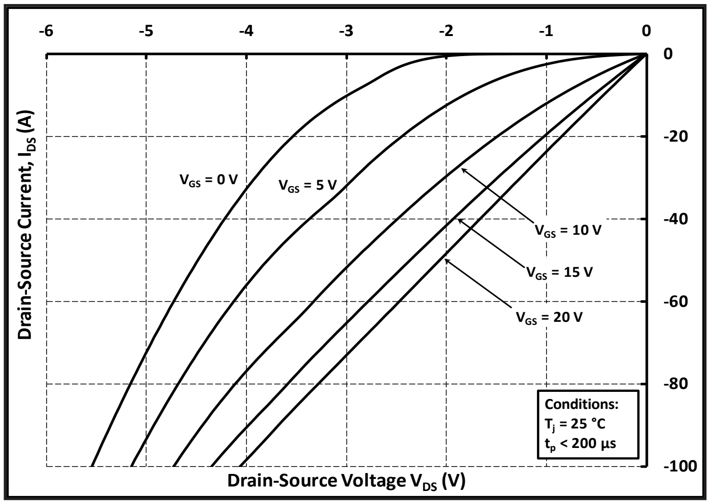


Figure 14. 3rd Quadrant Characteristic at 25 °C

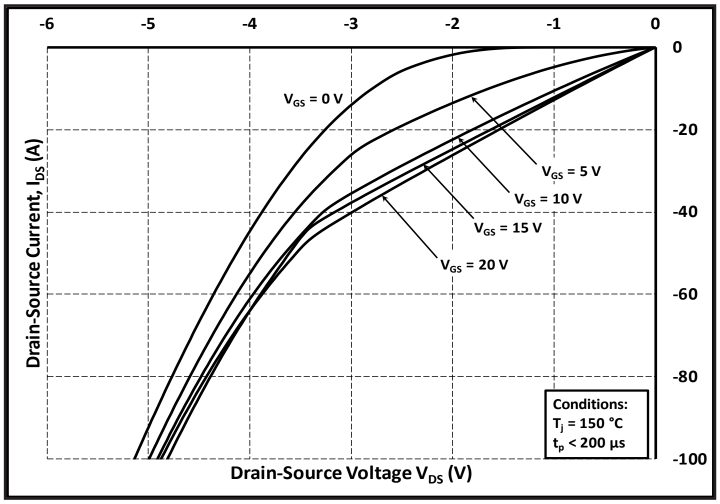


Figure 15. 3rd Quadrant Characteristic at 150 °C

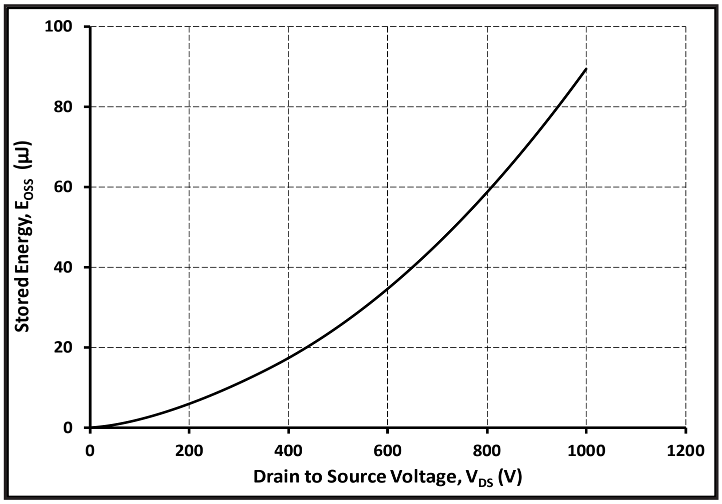


Figure 16. Output Capacitor Stored Energy

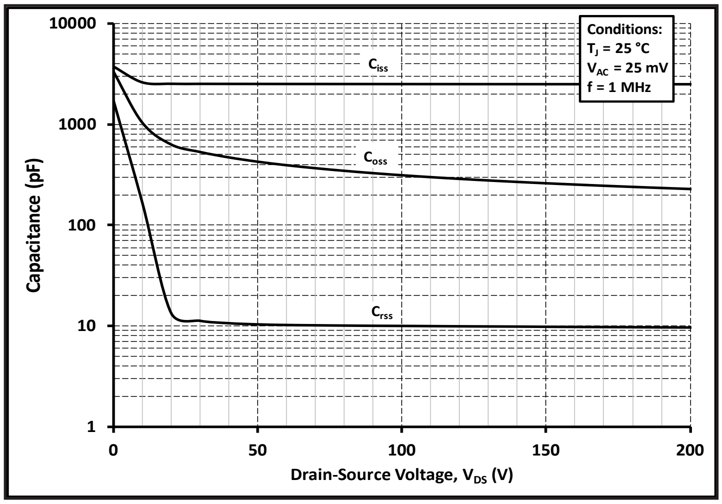


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

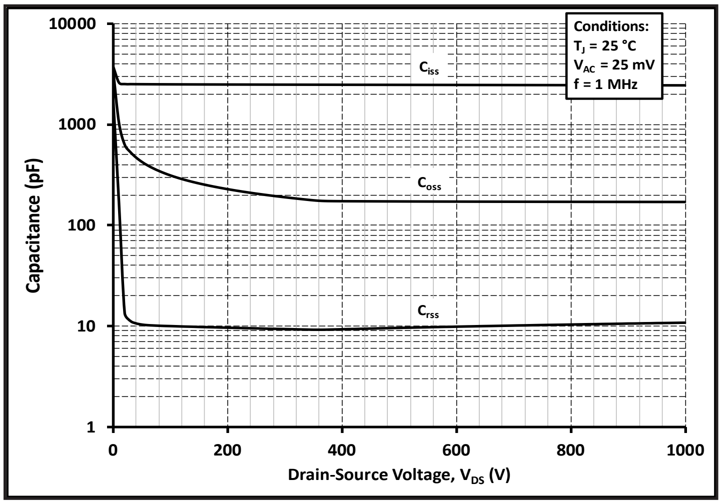


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

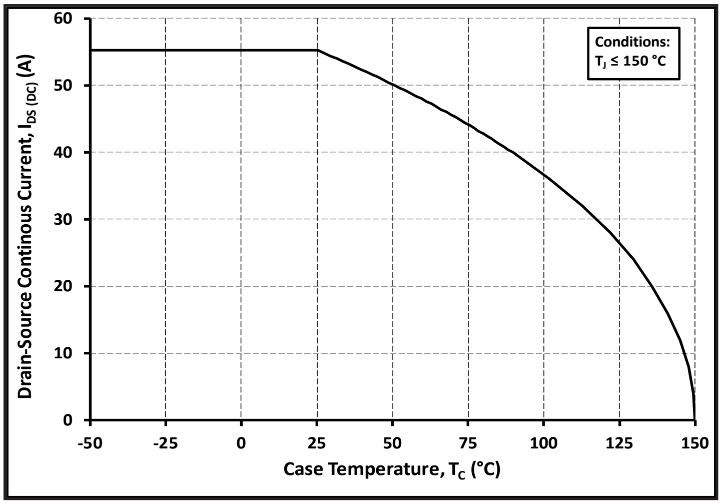


Figure 19. Continuous Drain Current Derating vs. Case Temperature

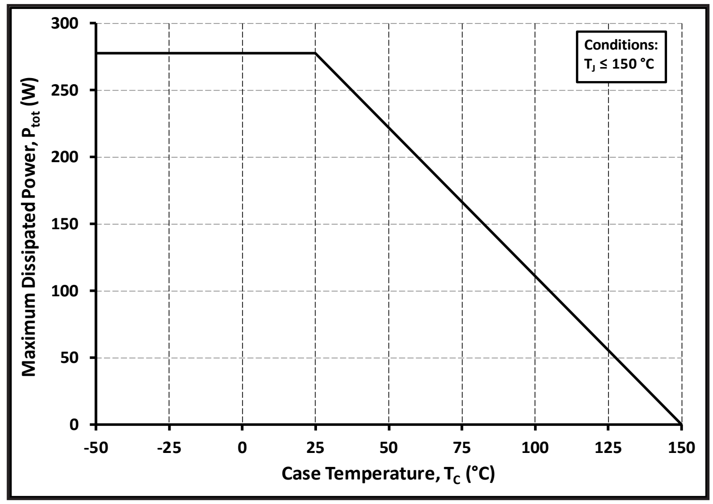


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

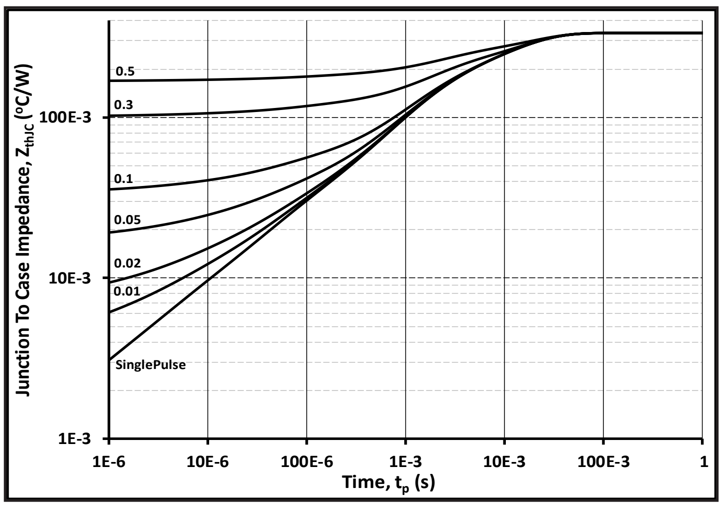


Figure 21. Transient Thermal Impedance (Junction - Case)

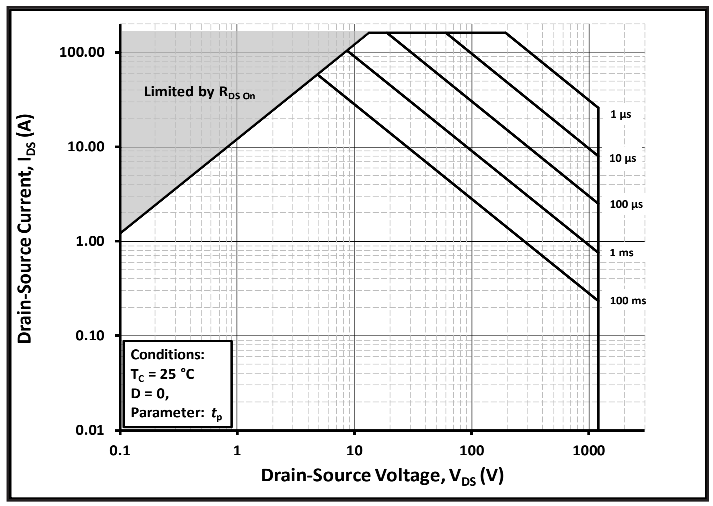


Figure 22. Safe Operating Area

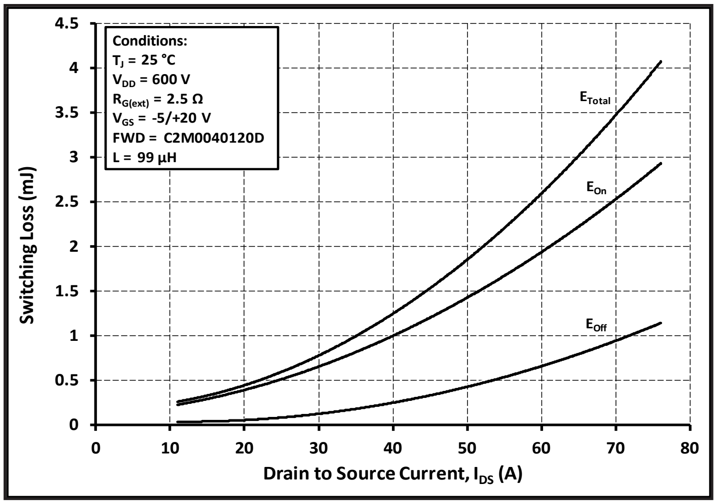


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

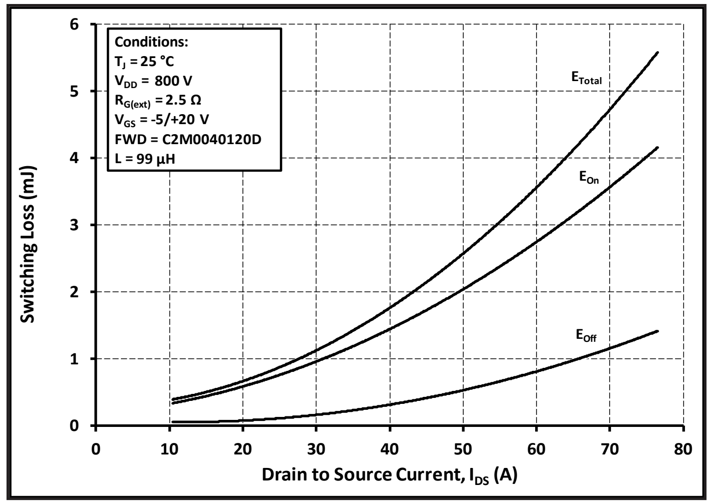


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

Typical Performance

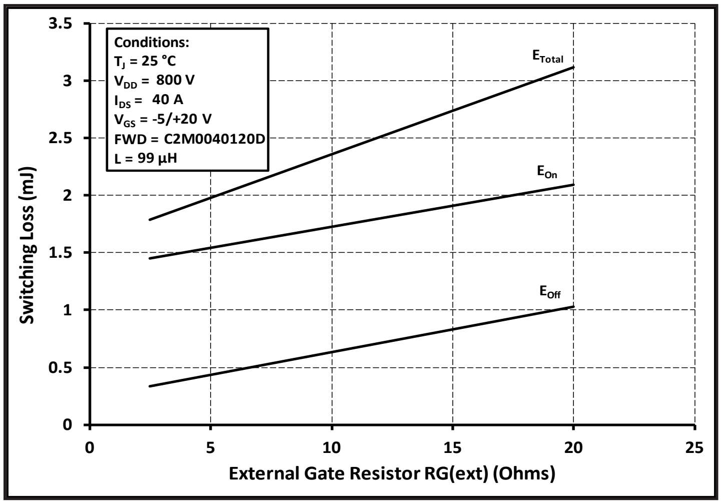


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

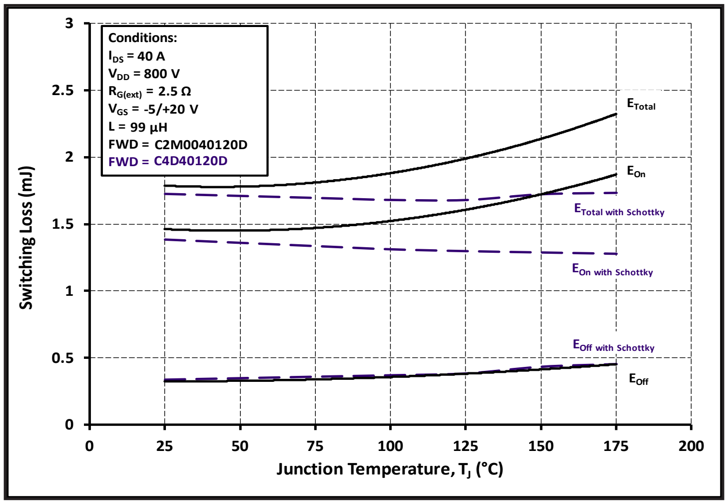


Figure 26. Clamped Inductive Switching Energy vs. Temperature

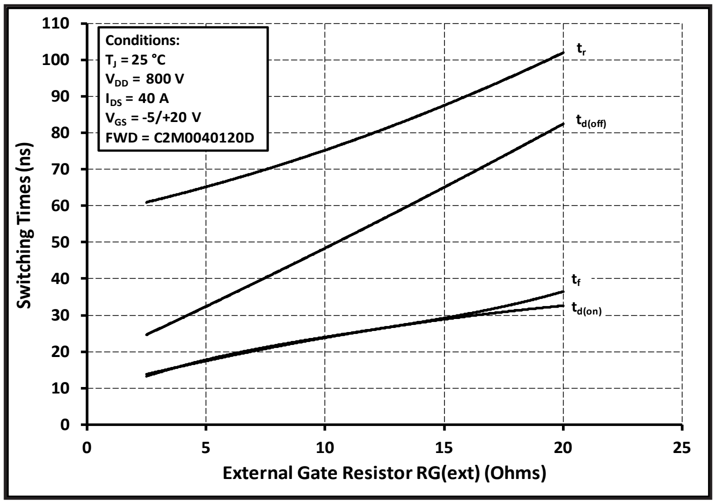


Figure 27. Switching Times vs. $R_{G(ext)}$

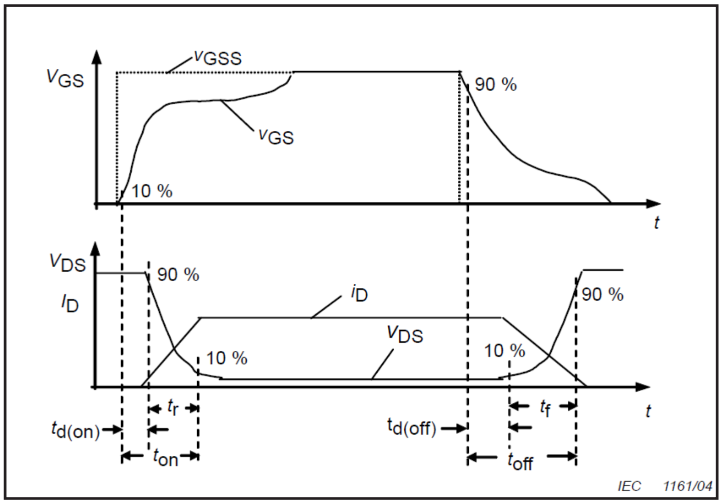


Figure 28. Switching Times Definition

Test Circuit Schematic

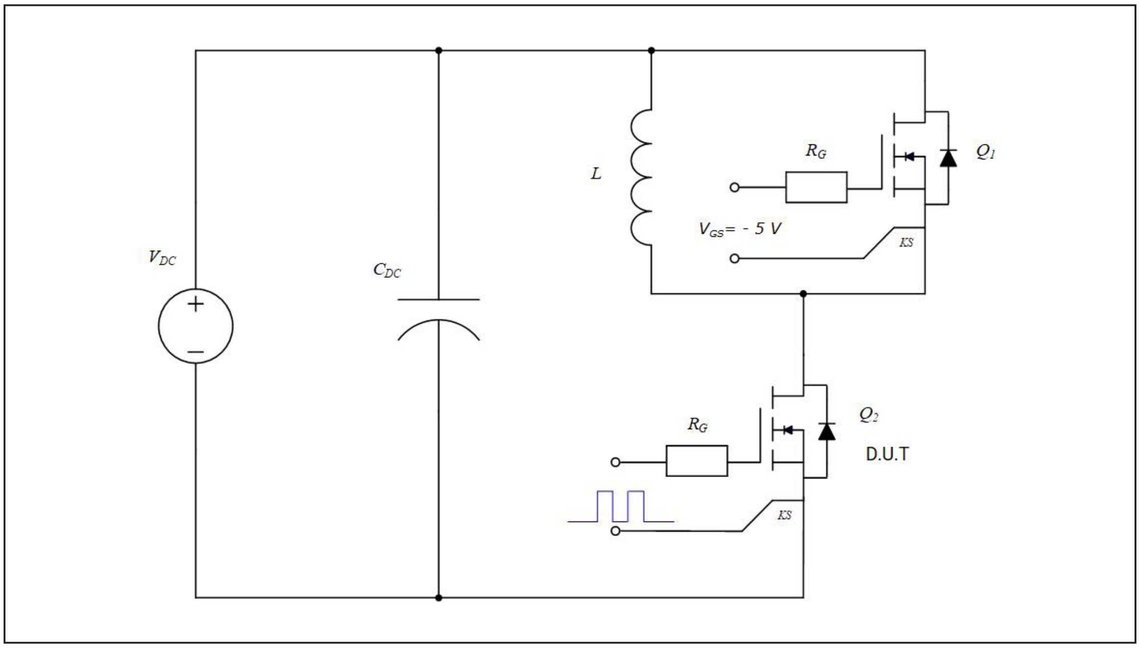


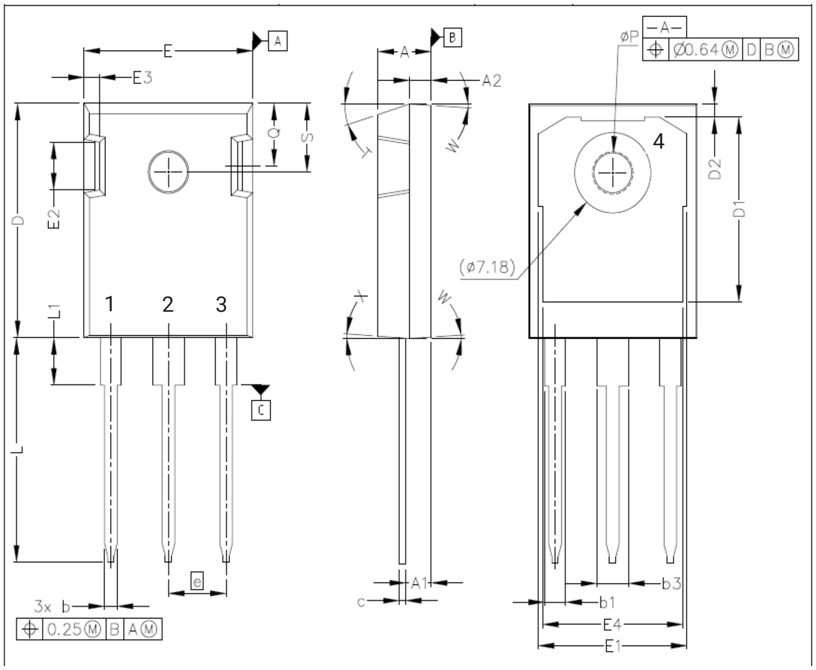
Figure 29. Clamped Inductive Switching
Waveform Test Circuit

ESD Ratings

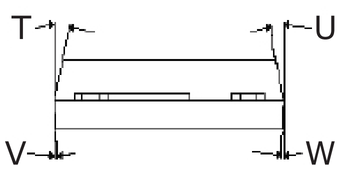
ESD Test	Resulting Classification
ESD-HBM	3A (4000V - 8000V)
ESD-CDM	C3 (>=1000V)

Package Dimensions

Package TO-247-3



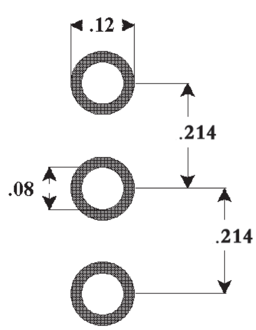
SYM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	.190	.205
A1	2.29	2.54	.090	.100
A2	1.91	2.16	.075	.085
b	1.07	1.33	.042	.052
b1	1.91	2.41	.075	.095
b3	2.87	3.38	.113	.133
c	0.55	0.68	.022	.027
D	20.80	21.10	.819	.831
D1	16.25	17.65	.640	.695
D2	0.95	1.25	.037	.049
E	15.75	16.13	.620	.635
E1	13.10	14.15	.516	.557
E2	3.68	5.10	.145	.201
E3	1.00	1.90	.039	.075
E4	12.38	13.43	.487	.529
e	5.44 BSC		.214 BSC	
N	3		3	
L	19.81	20.32	.780	.800
L1	4.10	4.40	.161	.173
øP	3.51	3.65	.138	.144
Q	5.49	6.00	.216	.236
S	6.04	6.30	.238	.248
T	17.5° REF.			
W	3.5° REF.			
X	4° REF.			



Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

Recommended Solder Pad Layout



TO-247-3

Notes

- **RoHS Compliance**
The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power