CMOS Digital Integrated Circuits Silicon Monolithic

TC7WPB8306L8X,TC7WPB8307L8X

1. Functional Description

- Low-Voltage, Low-Power 2-Bit Dual-Supply Bus Switch

2. General

The TC7WPB8306L8X and TC7WPB8307L8X are CMOS 2-bit dual-supply bus switches that can provide an interface between two nodes at different voltage levels. These devices can be connected to two independent power supplies. V_{CCA} supports 1.8-V, 2.5-V and 3.3-V power supplies, whereas V_{CCB} supports 2.5-V, 3.3-V and 5.0 V power supplies.

Each An terminal has an internal pull-up resistor to V_{CCA}, and each Bn terminal has an internal pull-up resistor to V_{CCB}. And each I/O terminal has a signal level detection circuit which speeds up the low-to-high transition.

The Output Enable ($\overline{OE}$: TC7WPB8307L8X, OE: TC7WPB8306L8X) input is common for all the two-bits of the data lines; thus these device are used as a single two-bits bus switch. For the TC7WPB8306L8X, Output Enable (OE) is active-High: When OE is High, the switch is on; when Low, the switch is off. For the TC7WPB8307L8X, Output Enable ($\overline{OE}$) is active-Low: When $\overline{OE}$ is Low, the switch is on; when High, the switch is off. All inputs and outputs of the TC7WPB8306L8X and TC7WPB8307L8X can tolerate overvoltage conditions up to 5.5 V. The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.

3. Features

(1) Operating voltage: 1.8 V to 2.5 V / 1.8 V to 3.3 V / 1.8 V to 5.0 V / 2.5 V to 3.3 V / 2.5 V to 5.0 V / 3.3 V to 5.0 V bidirectional interface

(2) Operating voltage: V_{CCA} = 1.65 to 5.0 V, V_{CCB} = 2.3 to 5.5 V

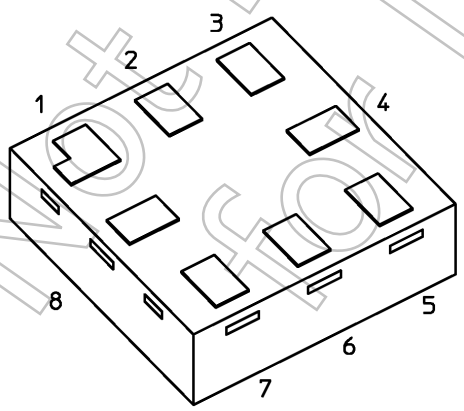
(3) R_{ON} = 6.5 Ω (typ.)
(ON-resistance test condition: V_{IS} = 0 V, I_{IS} = 10 mA, V_{CCA} = 3.0 V, V_{CCB} = 4.5 V)

(4) ESD performance: Machine mode ≥ ±200 V, Human body model ≥ ±2000 V

(5) 5.5-V tolerant function and power-down protection provided on all inputs and outputs.

(6) Packages: MP8

4. Packaging

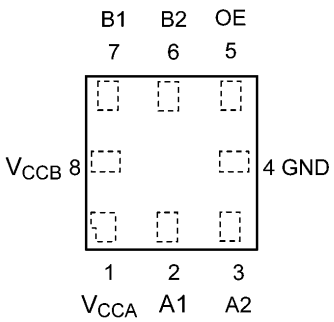


BOTTOM VIEW

MP8

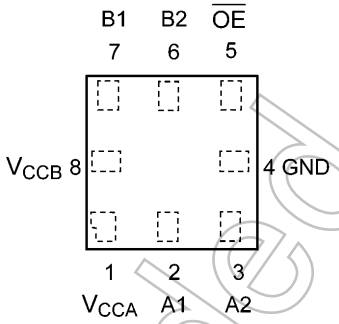
5. Pin Assignment

TC7WPB8306L8X



(Top view)

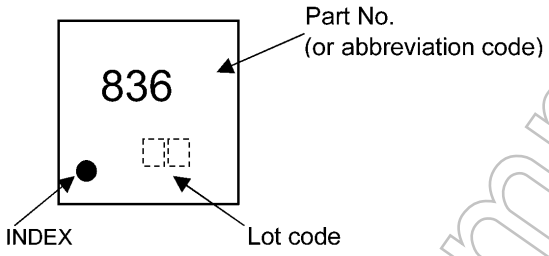
TC7WPB8307L8X



(Top view)

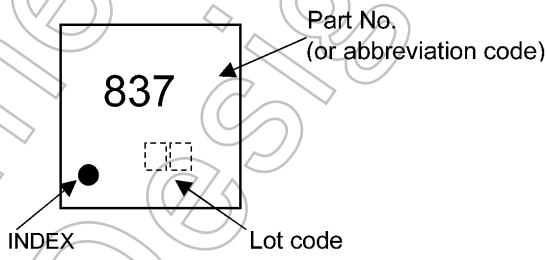
6. Marking

TC7WPB8306L8X



(Top view)

TC7WPB8307L8X

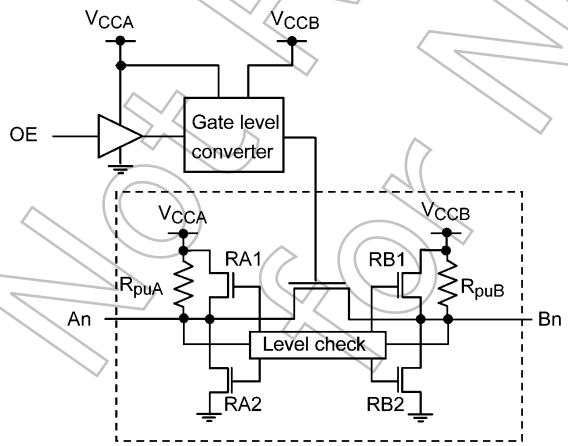


(Top view)

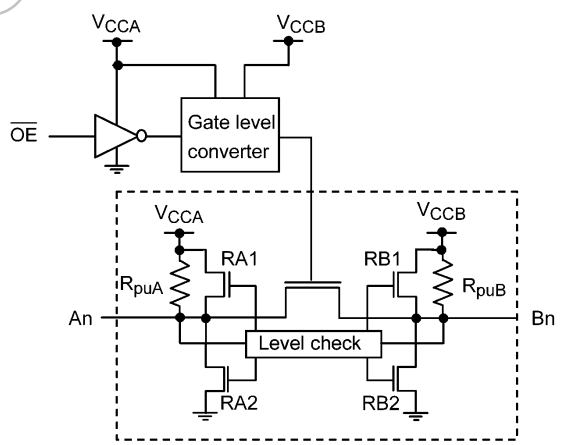
7. Block Diagram

One-shot driver circuits (RA1, RB1, RA2 and RB2) of the TC7WPB8306L8X and TC7WPB8307L8X detect either a rising or falling edge on the A or B port. During the rise time, the RA1 and RB1 transistors are turned on for a certain period to speed up a transition from Low to High. Likewise, during the fall time, the RA2 and RB2 transistors are turned on to speed up a transition from High to Low.

TC7WPB8306L8X



TC7WPB8307L8X



8. Principle of Operation

8.1. Truth Table

Inputs OE (TC7WPB8306L8X)	Inputs $\overline{OE}$ (TC7WPB8307L8X)	Function
H	L	A port = B port
L	H	Disconnect

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}		-0.5 to 7.0	V
	V_{CCB}		-0.5 to 7.0	
Input voltage ($\overline{OE}$, OE)	V_{IN}		-0.5 to 7.0	
Switch I/O voltage	V_S		-0.5 to 7.0	
Clamp diode current	I_{IK}		-50	mA
Switch I/O current	I_S		64	
V_{CC}/ground current per supply pin	I_{CCA}		±25	
	I_{CCB}		±25	
Power dissipation	P_D		300	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

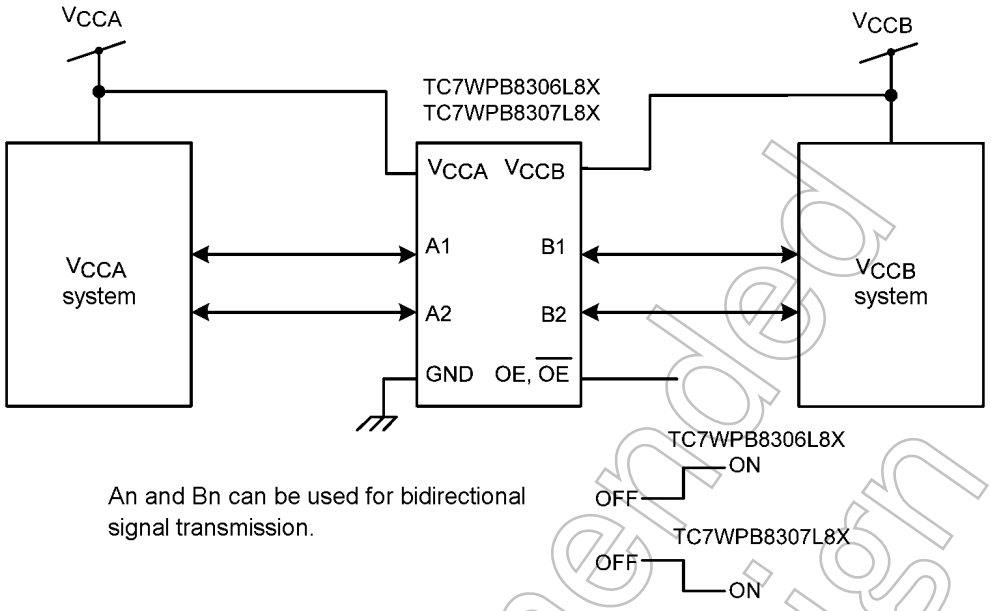
10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}	(Note 1)	1.65 to 5.0	V
	V_{CCB}		2.3 to 5.5	
Input voltage ($\overline{OE}$, OE)	V_{IN}		0 to 5.5	
Switch I/O voltage	V_S		0 to 5.5	
Operating temperature	T_{opr}		-40 to 85	°C
Input rise time ($\overline{OE}$, OE)	dt/dv		0 to 10	ns/V
Input fall time ($\overline{OE}$, OE)	dt/dv		0 to 10	

Note : The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

Note 1: The V_{CCA} voltage must be lower than the V_{CCB} voltage.

11. Application Circuit (Note)



Note: V_{CCA} < V_{CCB} voltage must be lower than the V_{CCB} voltage.

Note: Level-shifting functionality is enabled by adding pull-up resistors from An to V_{CCA} or V_{CCB} and from Bn to V_{CCB} or V_{CCA}, respectively.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Note	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IH}		—	1.65 ≤ V_{CCA} < 2.3	V_{CCA} to 5.5	0.8 × V_{CC}	—	V
				2.3 ≤ V_{CCA} < 5.0	V_{CCA} to 5.5	0.7 × V_{CCA}	—	
Low-level input voltage	V_{IL}		—	1.65 ≤ V_{CCA} < 2.3	V_{CCA} to 5.5	—	0.2 × V_{CCA}	V
				2.3 ≤ V_{CCA} < 5.0	V_{CCA} to 5.5	—	0.3 × V_{CCA}	
ON-resistance	R_{ON}	(Note 1)	V_{IS} = 0 V, I_{IS} = 10 mA See Fig. 13.1.	1.65	2.3	—	24	Ω
				2.3	3.0	—	14	
				3.0	4.5	—	12	
Pull-up resistance	R_{pu}		R_{puA} V_{IS} = V_{CCA} - 0.2 V	1.65	V_{CCA} to 5.5	—	40	kΩ
				2.3	V_{CCA} to 5.5	—	30	
				3.0	V_{CCA} to 5.5	—	20	
			R_{puB} V_{IS} = V_{CCB} - 0.2 V	1.65	V_{CCA} to 5.5	—	40	
				2.3	V_{CCA} to 5.5	—	30	
				3.0	V_{CCA} to 5.5	—	20	
One-shot driver ON-resistance	$R_{ON(OS)}$		RA1 = ON V_{IS} = V_{CCA} - 0.2 V	1.65	V_{CCA} to 5.5	—	80	Ω
				2.3	V_{CCA} to 5.5	—	60	
				3.0	V_{CCA} to 5.5	—	40	
			RA2 = ON V_{IS} = GND + 0.2 V	1.65 to 1.9	2.3	—	40	
				1.65 to 2.7	3.0	—	30	
				1.65 to 3.6	4.5	—	20	
			RB1 = ON V_{IS} = V_{CCB} - 0.2 V	1.65 to 1.9	2.3	—	40	
				1.65 to 2.7	3.0	—	30	
				1.65 to 3.6	4.5	—	20	
			RB2 = ON V_{IS} = GND + 0.2 V	1.65 to 1.9	2.3	—	40	
				1.65 to 2.7	3.0	—	30	
				1.65 to 3.6	4.5	—	20	
Power-OFF leakage current	I_{OFF}		An, Bn = 0 to 5.5 V, Per circuit	0	0	—	±1.0	μA
Switch OFF-state leakage current	I_{SZ}		An, Bn = 0 to 5.5 V, $\overline{OE}$ = V_{CCA}, OE = GND	1.65 to 5.0	V_{CCA} to 5.5	—	±1.0	
Input leakage current	I_{IN}		$\overline{OE}$, OE = 0 to 5.5 V	1.65 to 5.0	V_{CCA} to 5.5	—	±1.0	
Quiescent supply current	I_{CCA}		$\overline{OE}$, OE = V_{CCA} or GND, I_S = 0 A	1.65 to 5.0	V_{CCA}	—	1.0	μA
	I_{CCB}			1.65 to 5.0	V_{CCA}	—	1.0	
	I_{CCA}		V_{CCA} ≤ $\overline{OE}$, ≤ 5.5 V, I_S = 0 A	1.65 to 5.0	V_{CCA}	—	±1.0	
	I_{CCB}			1.65 to 5.0	V_{CCA}	—	±1.0	

Note 1: Measured by the voltage drop between A and B pins at the indicated current through the switch.

12.2. AC Characteristics

12.2.1. V_{CCA} = 1.8 ± 0.15 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (bus → bus)	t_{PLH}/t_{PHL}	(Note 1)	See Fig. 14.1, 14.3.	2.5 ± 0.2	—	25	ns
				2.5 ± 0.2	—	10	
3-state output enable time	t_{PZL}/t_{PZH}		See Fig. 14.2, 14.4.	2.5 ± 0.2	—	21	
3-state output disable time	t_{PLZ}/t_{PHZ}		See Fig. 14.2, 14.4.	2.5 ± 0.2	—	23	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 15 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

12.2.2. V_{CCA} = 2.5 ± 0.2 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (bus → bus)	t_{PLH}/t_{PHL}	(Note 1)	See Fig. 14.1, 14.3.	3.3 ± 0.3	—	18	ns
				3.3 ± 0.3	—	7	
3-state output enable time	t_{PZL}/t_{PZH}		See Fig. 14.2, 14.4.	3.3 ± 0.3	—	17	
3-state output disable time	t_{PLZ}/t_{PHZ}		See Fig. 14.2, 14.4.	3.3 ± 0.3	—	19	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 15 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

12.2.3. V_{CCA} = 2.5 ± 0.2 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (bus → bus)	t_{PLH}/t_{PHL}	(Note 1)	See Fig. 14.1, 14.3.	5.0 ± 0.5	—	15	ns
				5.0 ± 0.5	—	9	
3-state output enable time	t_{PZL}/t_{PZH}		See Fig. 14.2, 14.4.	5.0 ± 0.5	—	13	
3-state output disable time	t_{PLZ}/t_{PHZ}		See Fig. 14.2, 14.4.	5.0 ± 0.5	—	5	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 15 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

12.2.4. V_{CCA} = 3.3 ± 0.3 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns, f = 10 kHz)

Characteristics	Symbol	Note	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (bus → bus)	t_{PLH}/t_{PHL}	(Note 1)	See Fig. 14.1, 14.3.	5.0 ± 0.5	—	10	ns
				5.0 ± 0.5	—	6	
3-state output enable time	t_{PZL}/t_{PZH}		See Fig. 14.2, 14.4.	5.0 ± 0.5	—	9	
3-state output disable time	t_{PLZ}/t_{PHZ}		See Fig. 14.2, 14.4.	5.0 ± 0.5	—	11	

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 15 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

12.3. Timing Requirements

12.3.1. V_{CCA} = 1.8 ± 0.15 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Pulse duration (data input)	t_w	—	2.3	—	47	ns
			3.0	—	45	
			4.5	—	41	
Data rate	f_D	C_L = 15 pF	2.3	—	21	Mbps
			3.0	—	22	
			4.5	—	24	
		C_L = 150 pF	2.3	—	2.9	
			3.0	—	3.1	
			4.5	—	3.4	

12.3.2. V_{CCA} = 2.5 ± 0.2 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Pulse duration (data input)	t_w	—	3.0	—	45	ns
			4.5	—	41	
Data rate	f_D	C_L = 15 pF	3.0	—	22	Mbps
			4.5	—	24	
		C_L = 150 pF	3.0	—	3.1	
			4.5	—	3.4	

12.3.3. V_{CCA} = 3.3 ± 0.3 V
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Pulse duration (data input)	t_w	—	4.5	—	41	ns
Data rate	f_D	C_L = 15 pF	4.5	—	24	Mbps
		C_L = 150 pF	4.5	—	3.4	

12.4. Capacitive Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Part Number	Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance ($\overline{OE}$, OE)		C_{IN}	—	3.3	3.3	4	pF
Switch terminal OFF-capacitance	TC7WPB8306L8X	$C_{I/O}$	OE=GND, $V_{I/O}$=0V	3.3	3.3	10	
	TC7WPB8307L8X		$\overline{OE}$=V_{CC}, $V_{I/O}$=0V	3.3	3.3	10	
Switch terminal ON-capacitance	TC7WPB8306L8X	$C_{I/O}$	OE=V_{CC}, $V_{I/O}$=0V	3.3	3.3	20	
	TC7WPB8307L8X		$\overline{OE}$=GND, $V_{I/O}$=0V	3.3	3.3	20	

13. DC Test Circuit

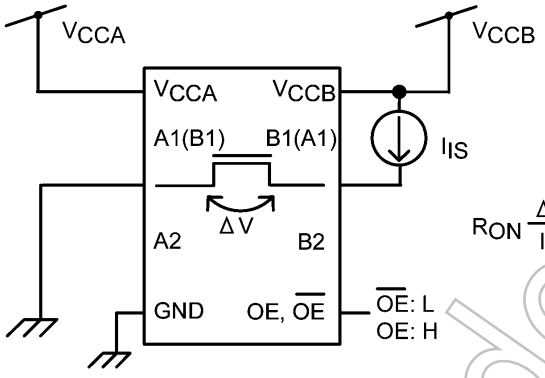


Fig. 13.1 ON-resistance Test Circuits

14. AC Test Circuits/Waveform

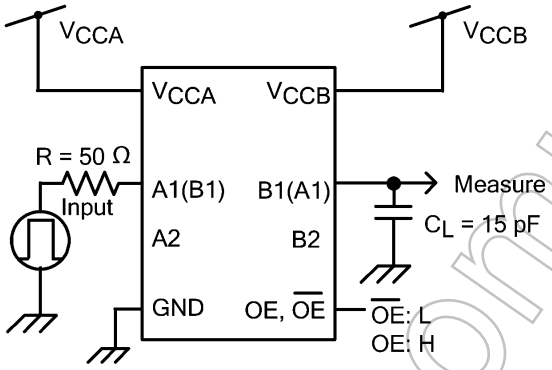


Fig. 14.1 t_{PLH}, t_{PHL} Test Circuits

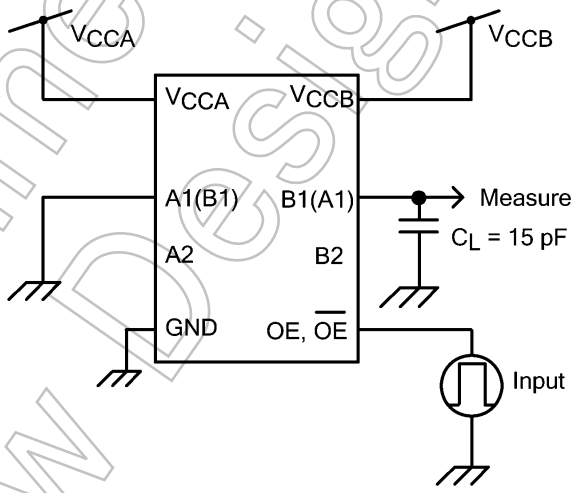


Fig. 14.2 t_{PLZ}, t_{PZL} Test Circuits

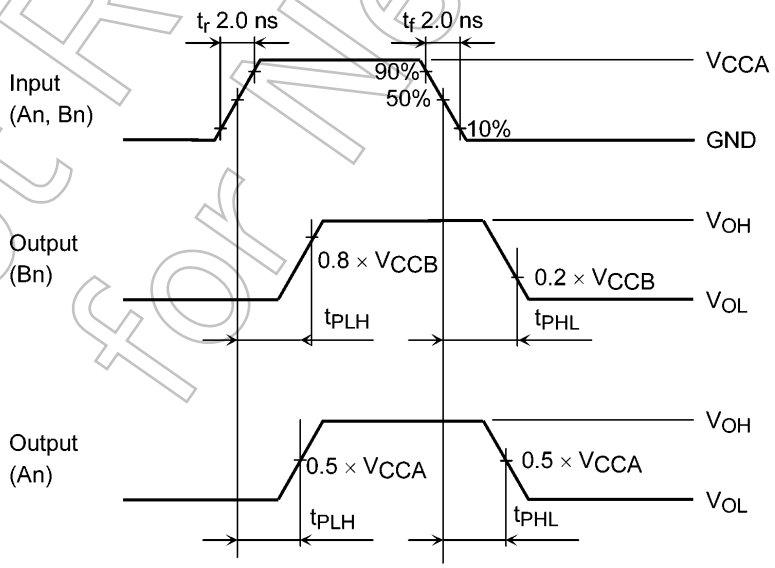


Fig. 14.3 AC Waveform of t_{PLH}, t_{PHL}

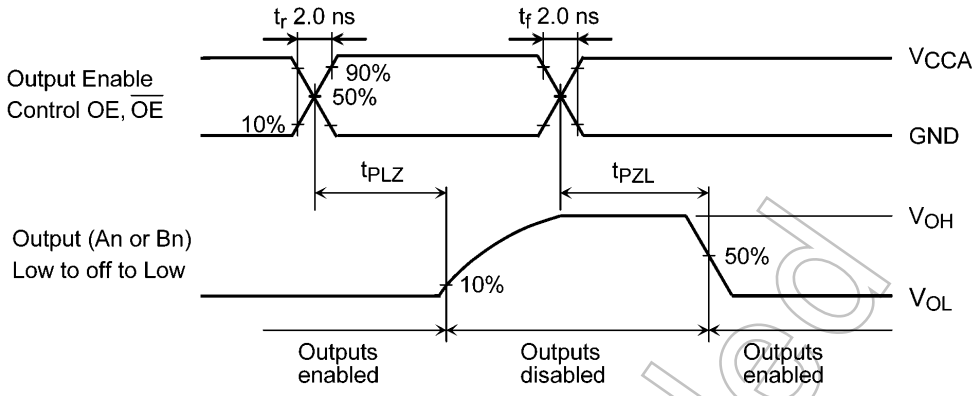
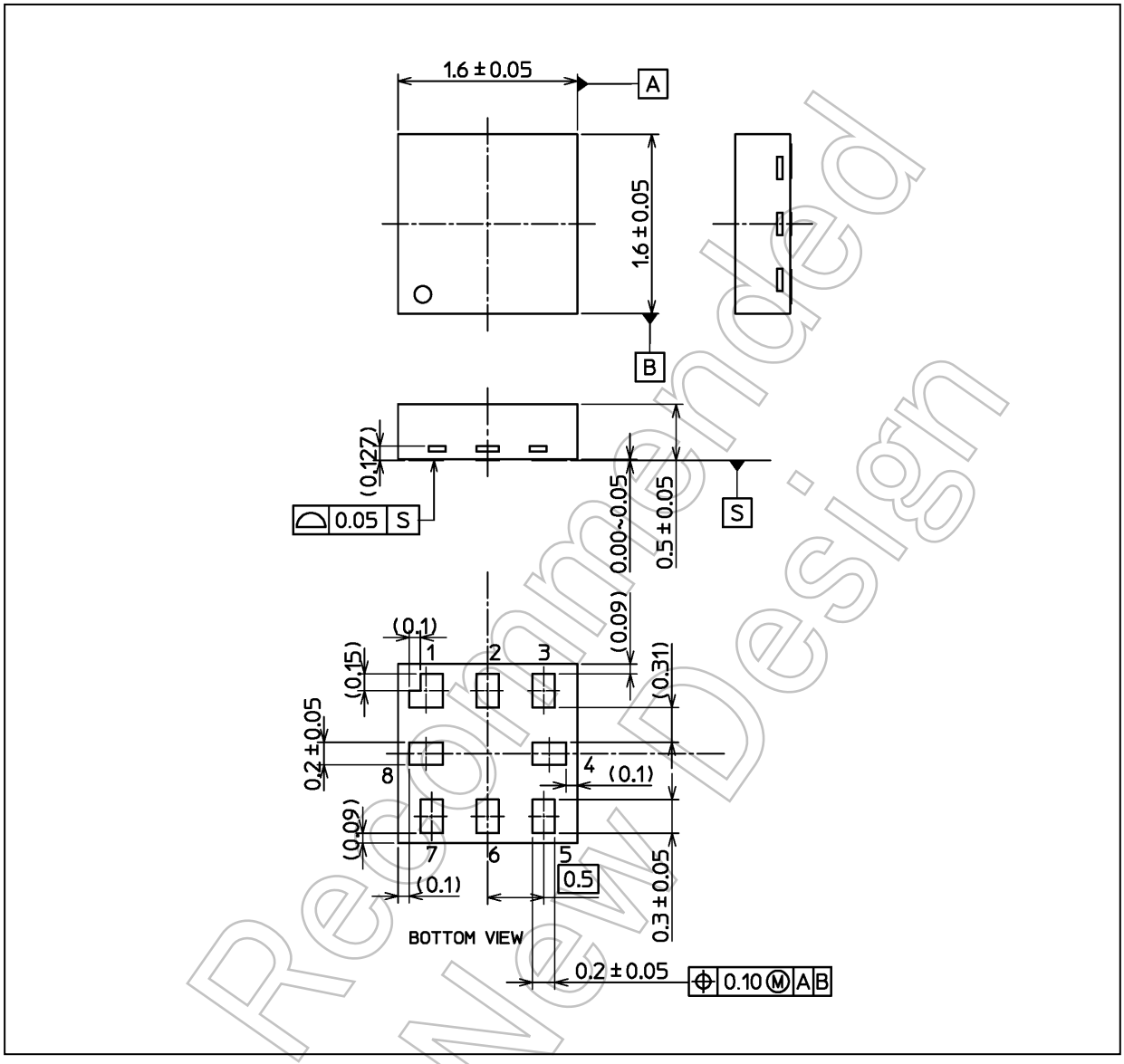


Fig. 14.4 AC Waveform of t_{PLZ}, t_{PZL}

Package Dimensions

Unit: mm



Weight: 0.0039 g (typ.)

Package Name(s)
TOSHIBA: P-UFLGA8-0202-0.50-002
Nickname: MP8

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