



# MPQ4425C

36V, 1.5A, 2.2MHz, High-Efficiency,  
Synchronous Step-Down LED Driver,  
AEC-Q100 Qualified

## DESCRIPTION

The MPQ4425C is a high-frequency, synchronous, rectified, step-down, switch-mode white LED (WLED) driver with integrated internal power MOSFETs. It offers a compact solution that can achieve up to 1.5A of continuous output current ( $I_{OUT}$ ) across a wide 4V to 36V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation.

Synchronous mode offers high efficiency across the entire  $I_{OUT}$  load range. Current mode control provides fast transient response and improved loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ4425C requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-13 (2.5mmx3mm) package.

## FEATURES

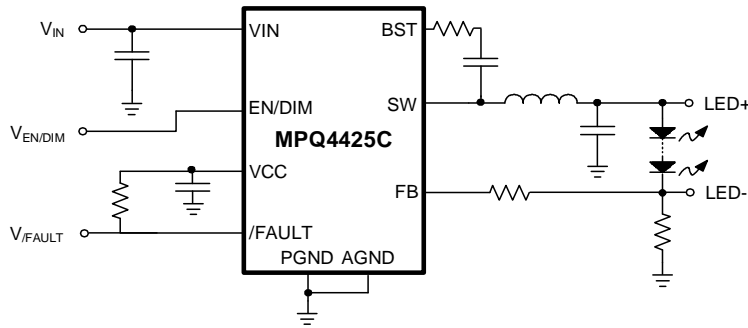
- Built for a Wide Range of Automotive LED Applications:
  - Wide 4V to 36V Operating Input Voltage ( $V_{IN}$ ) Range
  - Up to 1.5A continuous LED current ( $I_{LED}$ )
  - Pulse-Width Modulation (PWM) Dimming with Minimum 100Hz Dimming Frequency ( $f_{DIM}$ )
- High Performance for Improved Thermals:
  - 90mΩ/60mΩ Low  $R_{DS(ON)}$ , Internal Power MOSFETs
  - 0.195V Reference Voltage ( $V_{REF}$ )
  - Synchronous Mode for High-Efficiency
- Reduced EMC/EMI:
  - 2.2MHz Default Switching Frequency ( $f_{sw}$ )
- Full Protection Features:
  - Fault Indication for LED Short, LED Open, and Thermal Shutdown
  - Over-Current Protection (OCP) with Valley Current Detection
  - Thermal Shutdown
- Additional Features:
  - Forced Continuous Conduction Mode (FCCM)
  - Internal Soft Start (SS)
  - CISPR25 Class 5 Compliant
  - Available in a QFN-13 (2.5mmx3mm) Package
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1

## APPLICATIONS

- Fog Lights
- Daytime Running Lights (DRLs)
- Puddle Lights

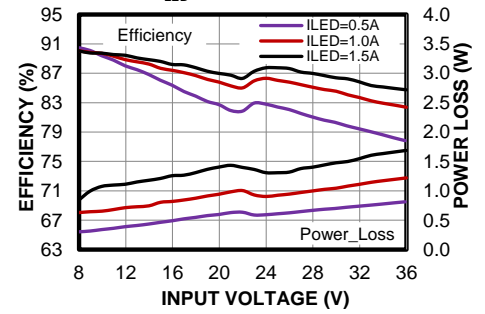
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### TYPICAL APPLICATION



**Efficiency vs. Input Voltage vs. Power Loss**

2 LEDs ( $V_{LED} = 6.4V$ ),  $L = 2.2\mu H$



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4425CGQBE-AEC1***	QFN-13 (2.5mmx3mm)	See Below	Level 1

\* For Tape & Reel, add suffix -Z (e.g. MPQ4425CGQBE-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable Flank

### TOP MARKING (MPQ4425CGQBE-AEC1)

**BUD**  
**YWW**  
**LLL**

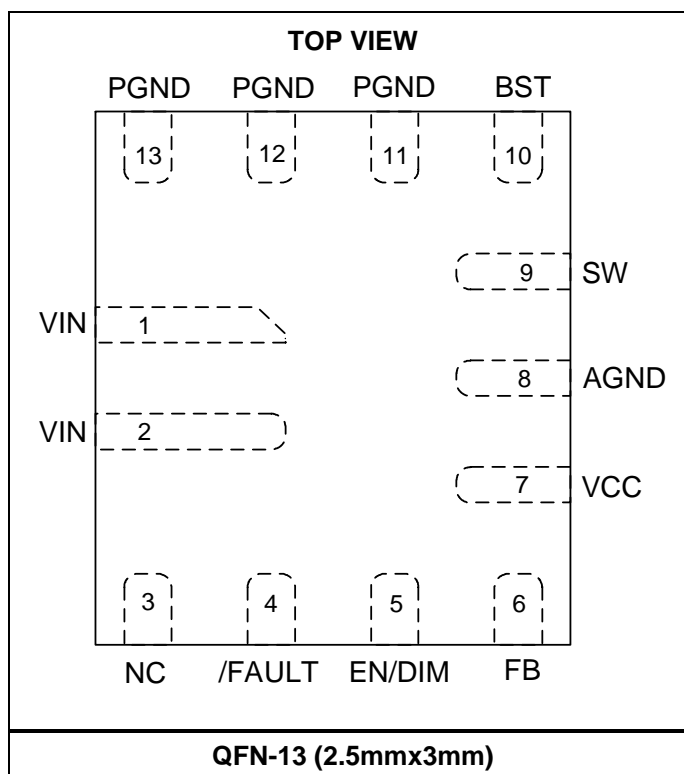
BUD: Product code of the MPQ4425CGQBE-AEC1

Y: Year code

WW: Week code

LLL: Lot number

### PACKAGE REFERENCE



**PIN FUNCTIONS**

Pin #	Name	Description
1, 2	VIN	<b>Supply voltage.</b> The MPQ4425C operates from a 4V to 36V input rail. An input capacitor ( $C_{IN}$ ) is required to decouple the input rail. Connect the VIN pin to the input trace using a wide PCB trace.
3	NC	<b>Do not connect.</b>
4	/FAULT	<b>Fault indicator.</b> The /FAULT pin is an open-drain output. If LED short, LED open, or thermal shutdown occurs, /FAULT is pulled low.
5	EN/DIM	<b>Enable/dimming control.</b> Pull EN above 1.8V to turn the LED driver on; pull EN below 0.7V to turn it off. Apply a 100Hz to 2kHz external clock to the EN/DIM pin for pulse-width modulation (PWM) dimming.
6	FB	<b>LED current feedback input.</b>
7	VCC	<b>Internal bias supply.</b> Decouple the VCC pin using a 0.1 $\mu$ F to 0.22 $\mu$ F capacitor. The VCC capacitor ( $C_{VCC}$ ) should not exceed 0.22 $\mu$ F.
8	AGND	<b>Analog ground.</b> The AGND pin is the reference ground of the logic circuit. The AGND and PGND pins are connected internally. Additional external connections to PGND are not required.
9	SW	<b>Switch output.</b> Use a wide PCB trace to make the SW connection.
10	BST	<b>Bootstrap.</b> Connect a capacitor ( $C_{BST}$ ) between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver. It is strongly recommended connect a 20 $\Omega$ resistor between SW and $C_{BST}$ to reduce spikes on SW.
11, 12, 13	PGND	<b>Power ground.</b> The PGND pin is the reference ground of the power device. PGND requires careful consideration during PCB layout. For the best results, use copper pours and vias to make the PGND connection.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Input voltage ( $V_{IN}$ )	-0.3V to +40V
SW voltage ( $V_{SW}$ )	-0.3V to $V_{IN} + 0.3V$
BST voltage ( $V_{BST}$ )	$V_{SW} + 6V$
All other pins	-0.3V to +6V <sup>(2)</sup>
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(3) (8)</sup>	
QFN-13 (2.5mmx3mm)	2.98W
Junction temperature ( $T_J$ )	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

**Electrostatic Discharge (ESD) Rating**

Human body model (HBM)	Class 2 <sup>(4)</sup>
Charged device model (CDM)	Class C2b <sup>(5)</sup>

**Recommended Operating Conditions**

Supply voltage ( $V_{IN}$ )	4V to 36V
LED current ( $I_{LED}$ )	Up to 1.5A
Operating $T_J$ <sup>(6)</sup>	-40°C to +125°C

<b>Thermal Resistance</b>	$\theta_{JA}$	$\theta_{JC}$
<b>QFN-13 (2.5mmx3mm)</b>		
JESD51-7 <sup>(7)</sup>	60	13... °C/W
EVQ4425C-QB-00A <sup>(8)</sup>	42	2.5.. °C/W

**Notes:**

- 1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
- 2) See the Enable (EN) Control section on page 20 for more details.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) Per AEC-Q100-002.
- 5) Per AEC-Q100-011.
- 6) Operating devices at >125°C junction temperatures is possible. Contact MPS for details.
- 7) Measured on JESD51-7, 4-layer PCB. The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- 8) Measured on the EVQ4425C-QB-00A (6.4cmx6.4cm), 2oz copper thick, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	$I_{IN}$	$V_{EN} = 0V$		12		$\mu A$
Quiescent current	$I_Q$	$V_{EN} = 2V$ , $V_{FB} = 1V$ , no switching		0.6	0.8	mA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_{HS}}$	$V_{BST} - V_{SW} = 5V$		90	160	m $\Omega$
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_{LS}}$	$V_{CC} = 5V$		60	115	m $\Omega$
Switch leakage	$I_{SW\_LKG}$	$V_{EN} = 0V$ , $V_{SW} = 12V$			1	$\mu A$
Current limit <sup>(9)</sup>	$I_{LIMIT}$	<40% duty cycle	2.5	4	5.5	A
Reverse current limit				1.2		A
Switching frequency	$f_{SW}$	$V_{FB} = 100mV$	1800	2200	2600	kHz
Maximum duty cycle	$D_{MAX}$	$V_{FB} = 100mV$	80	87		%
Minimum on time <sup>(9)</sup>	$t_{ON\_MIN}$			46		ns
Feedback voltage	$V_{FB}$	$T_J = 25^{\circ}C$	187	195	203	mV
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	180	195	210	
Feedback current	$I_{FB}$	$V_{FB} = 250mV$		30	200	nA
EN rising threshold	$V_{EN\_RISING}$		1.1	1.45	1.8	V
EN falling threshold	$V_{EN\_FALLING}$		0.7	1	1.3	V
EN hysteresis	$V_{EN\_HYS}$			450		mV
EN current	$I_{EN}$	$V_{EN} = 2V$		5	10	$\mu A$
		$V_{EN} = 0$		0	0.2	$\mu A$
EN turn-off delay	$t_{EN\_OFF\_DELAY}$		10	25	50	ms
$V_{IN}$ under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		3.2	3.5	3.8	V
$V_{IN}$ UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.8	3.1	3.5	V
$V_{IN}$ UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			400		mV
Over-voltage (OV) detection	$V_{OV\_DET}$	/FAULT is pulled low		140		% of $V_{FB}$
OV detection hysteresis	$V_{OV\_DET\_HYS}$			20		% of $V_{FB}$
/FAULT delay	$t_{/FAULT}$			10		$\mu s$
/FAULT sink current capability	$V_{/FAULT}$	Sink 4mA			0.4	V
/FAULT leakage current	$I_{/FAULT\_LKG}$				100	nA
VCC regulator voltage	$V_{CC}$	$I_{CC} = 0mA$	4.6	4.9	5.2	V
VCC load regulation		$I_{CC} = 5mA$		1.5	4	%
Soft-start time <sup>(9)</sup>	$t_{SS}$	$I_{LED} = 1.5A$ , $L = 2.2\mu H$ , 2-series LED load $I_{LED}$ from 10% to 90%		1		ms
Thermal shutdown <sup>(9)</sup>			150	170		$^{\circ}C$
Thermal hysteresis <sup>(9)</sup>				30		$^{\circ}C$

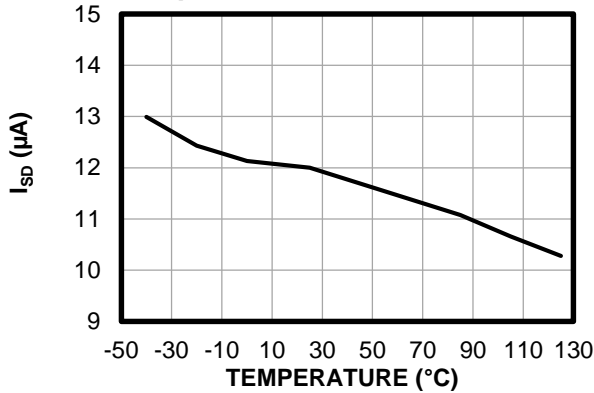
**Note:**

9) Guaranteed by design and characterization. Not tested in production.

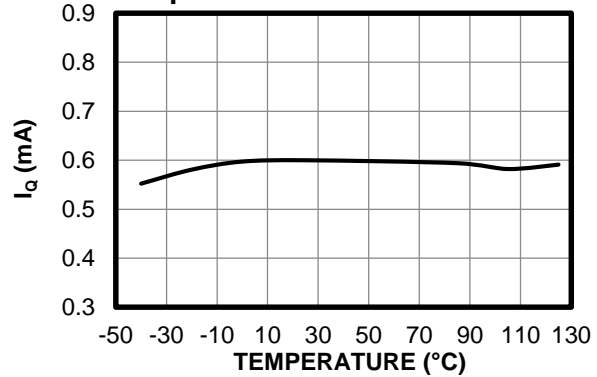
## TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

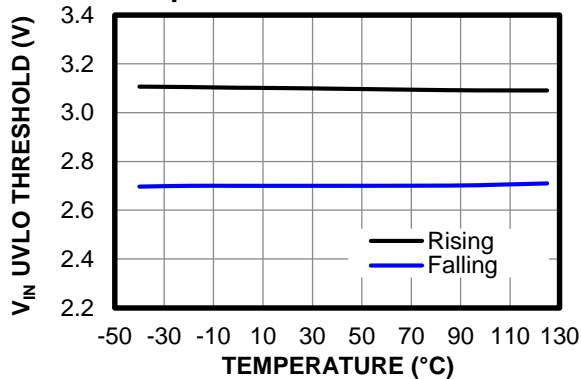
**Shutdown Current vs. Temperature**



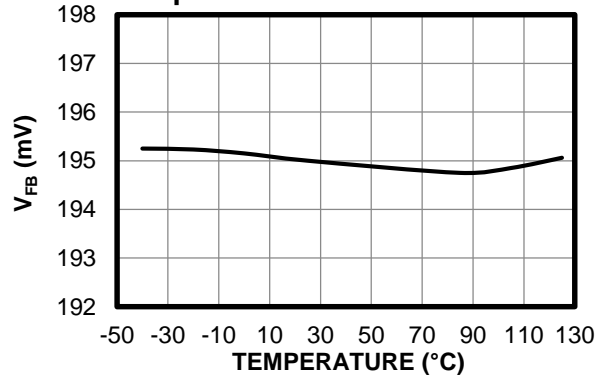
**Quiescent Current vs. Temperature**



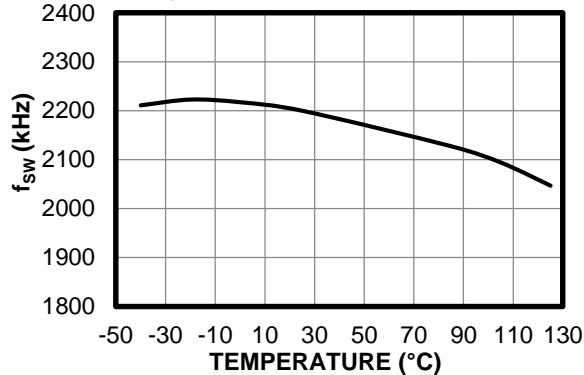
**$V_{IN}$  UVLO Threshold vs. Temperature**



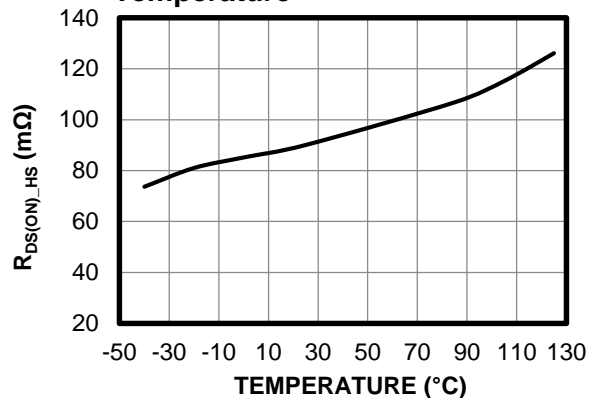
**Feedback Voltage vs. Temperature**



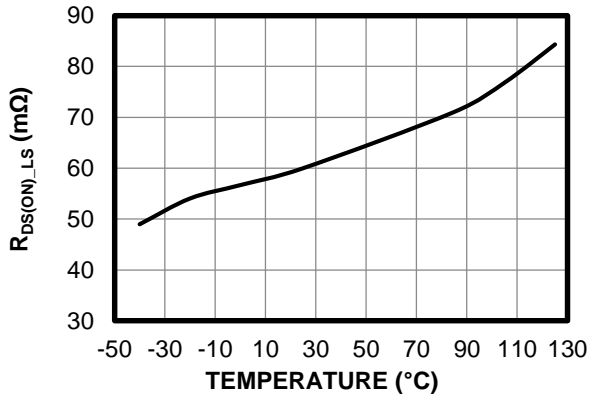
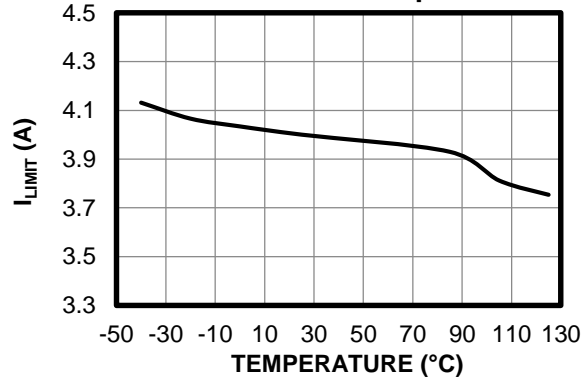
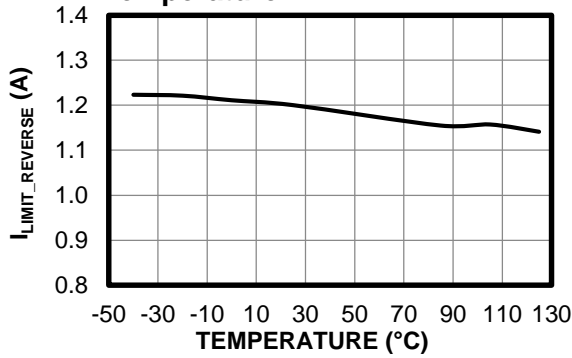
**Switching Frequency vs. Temperature**



**HS-FET On Resistance vs. Temperature**



**TYPICAL CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

**LS-FET On Resistance vs. Temperature**

**Current Limit vs. Temperature**

**Reverse Current Limit vs. Temperature**


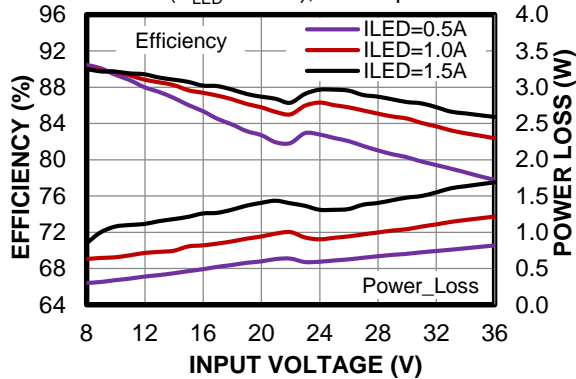


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{sw} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(10)</sup>

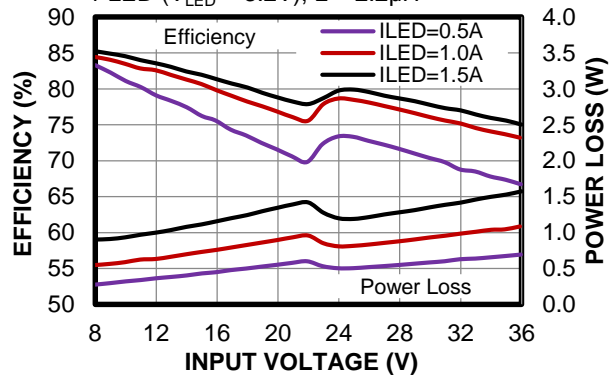
**Efficiency vs. Input Voltage vs. Power Loss**

2 LEDs ( $V_{LED} = 6.4V$ ),  $L = 2.2\mu H$



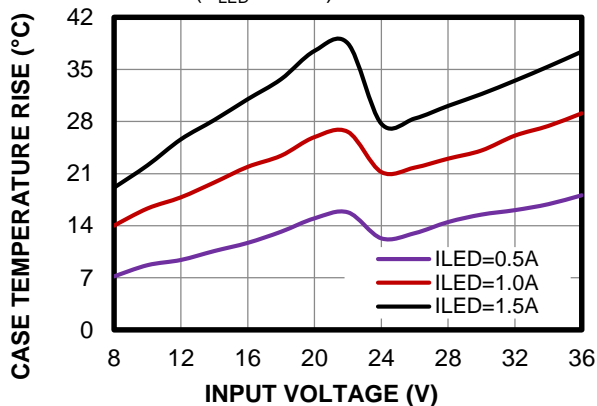
**Efficiency vs. Input Voltage vs. Power Loss**

1 LED ( $V_{LED} = 3.2V$ ),  $L = 2.2\mu H$



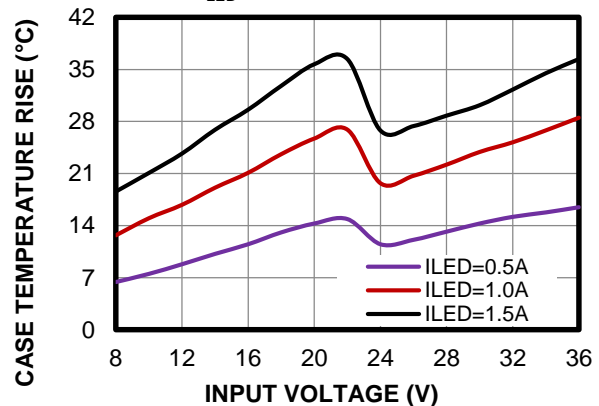
**Case Temperature Rise**

2 LEDs ( $V_{LED} = 6.4V$ )

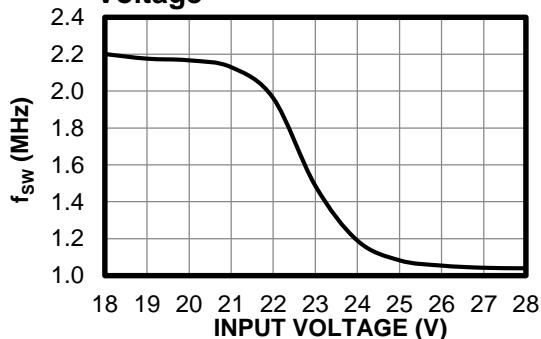


**Case Temperature Rise**

1 LED ( $V_{LED} = 3.2V$ )



**Switching Frequency vs. Input Voltage**



**Note:**

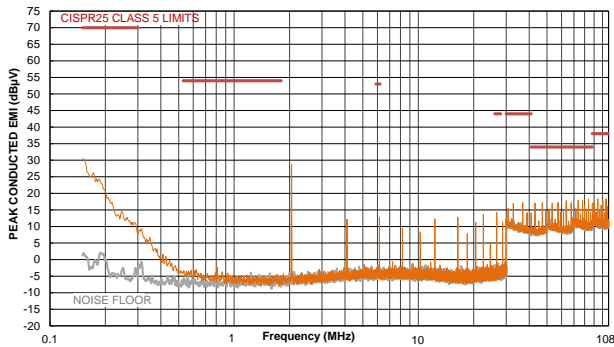
10) The Efficiency and Case Temperature Rise curves are based on Figure 9 on page 26, where the bootstrap (BST) resistor ( $R_{BST}$ ) is  $0\Omega$ , the output and input filters have been removed, and the inductor ( $L$ ) is  $2.2\mu H$  (VCTA25201B-2R2MS6).

## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(11)</sup>

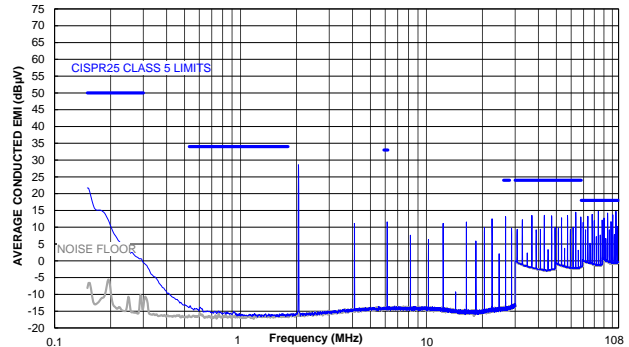
### CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



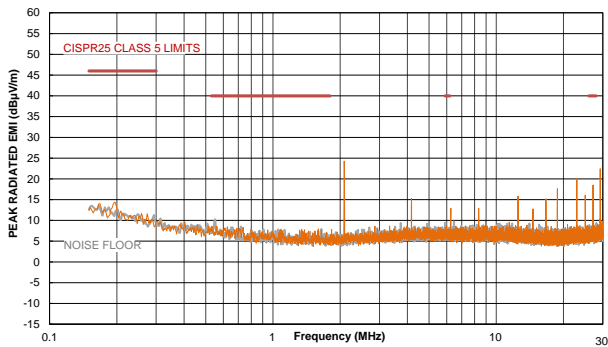
### CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



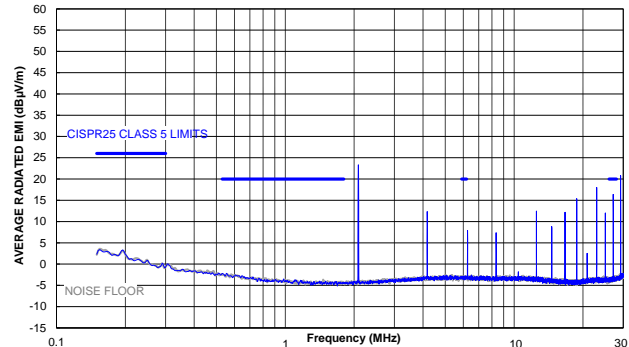
### CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



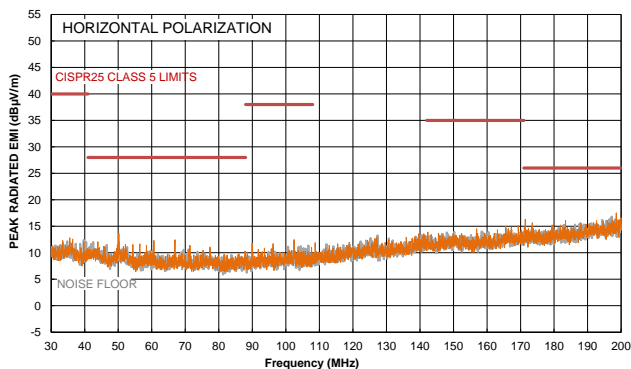
### CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



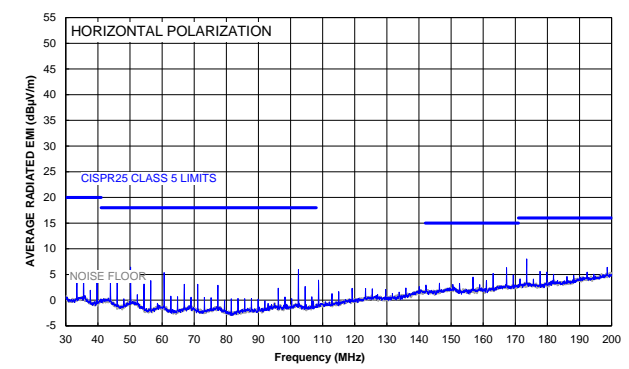
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

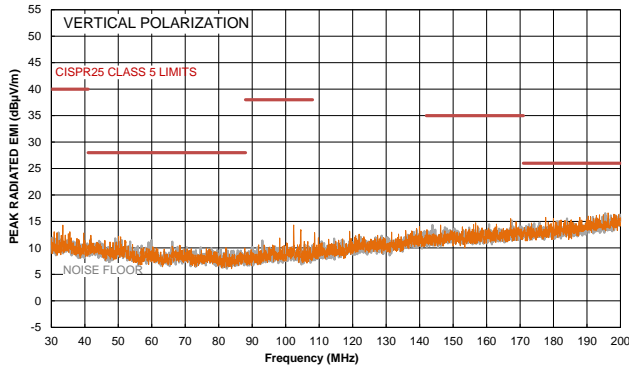


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , with EMI filters,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(11)</sup>

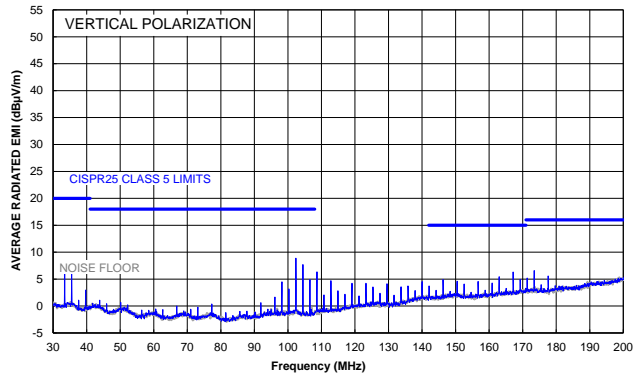
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



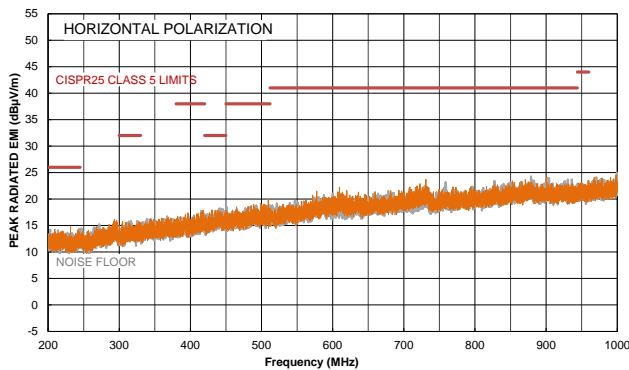
### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



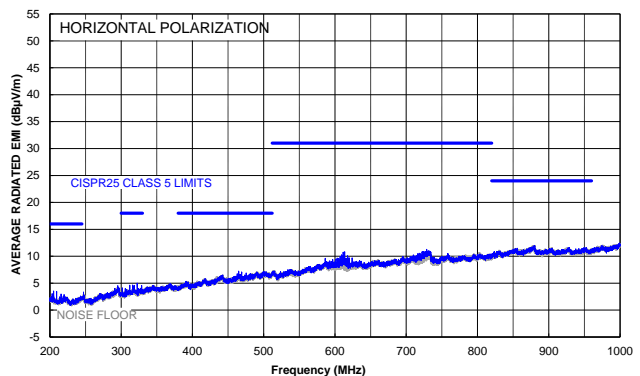
### CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



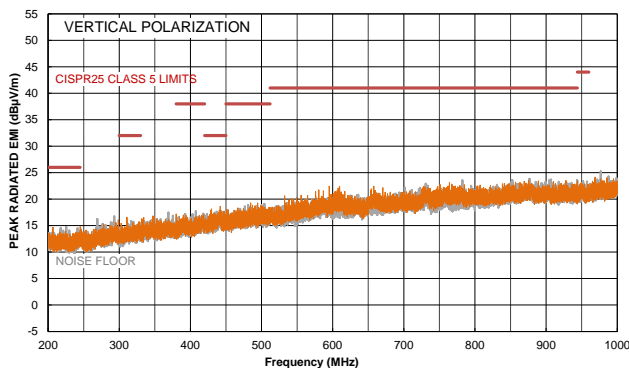
### CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



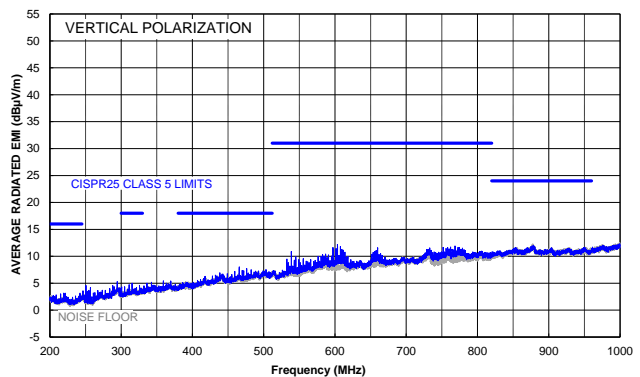
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

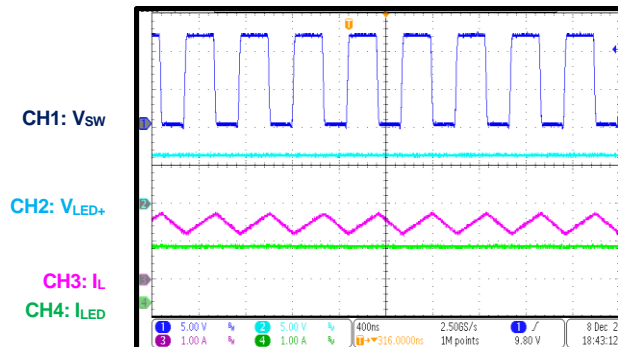
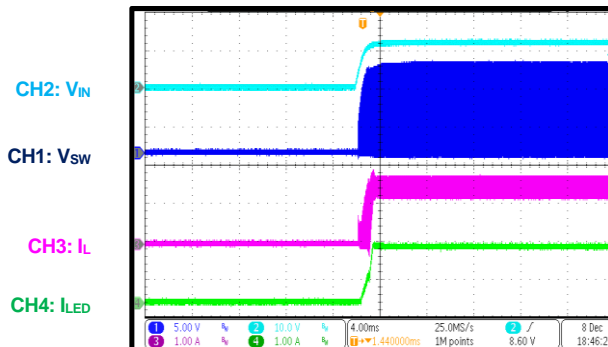
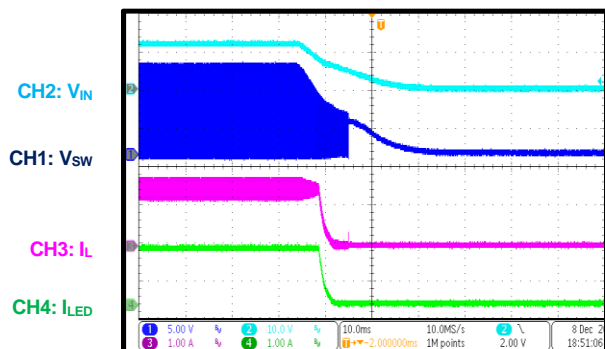
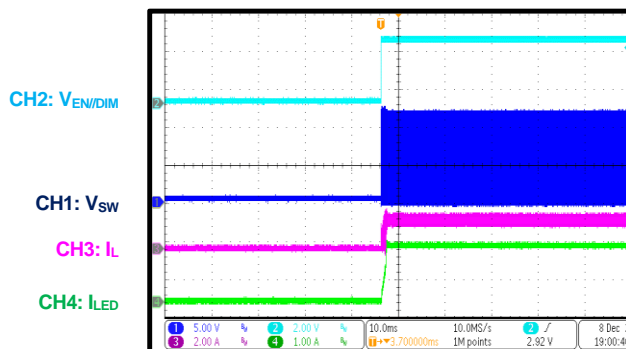
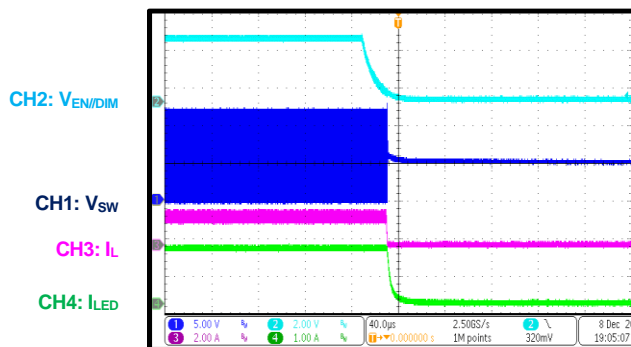
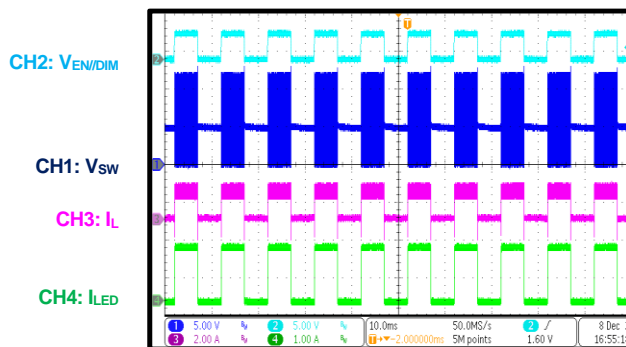
Vertical, 200MHz to 1GHz



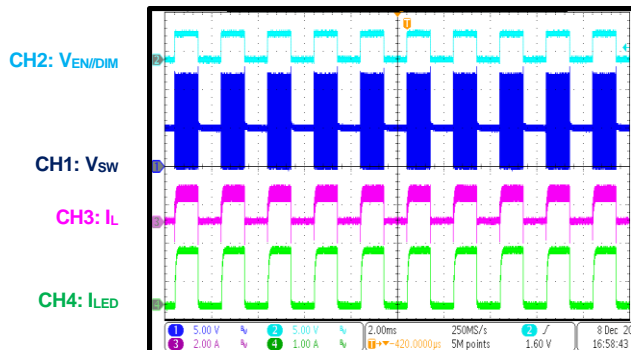
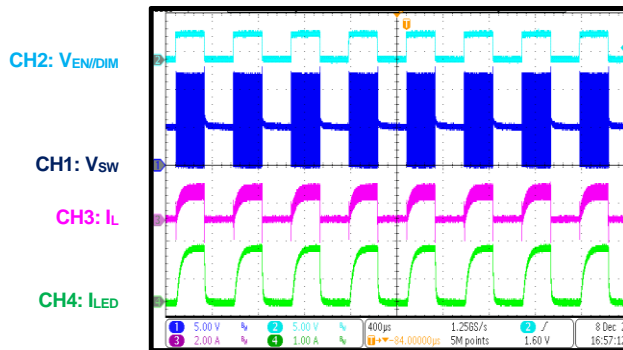
**Note:**

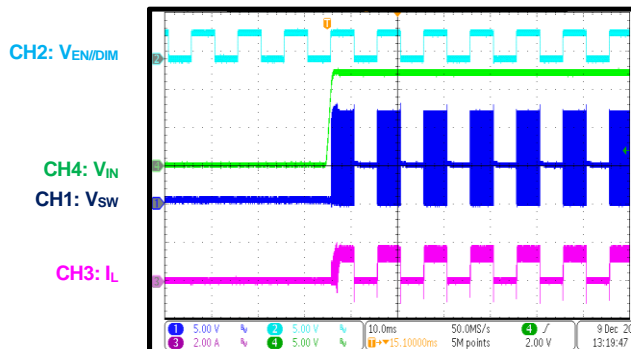
11) The EMI test results are based on Figure 10 on page 26.

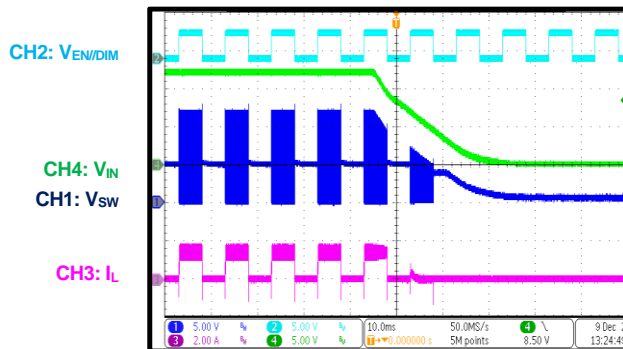
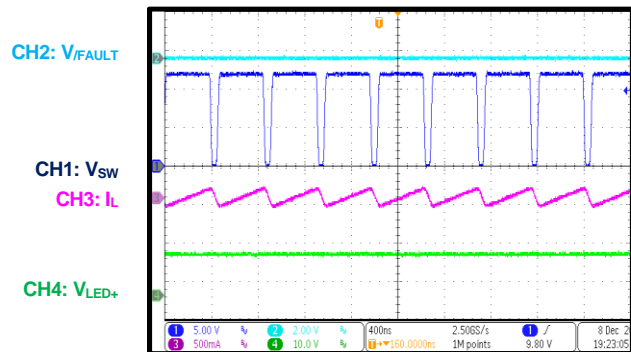
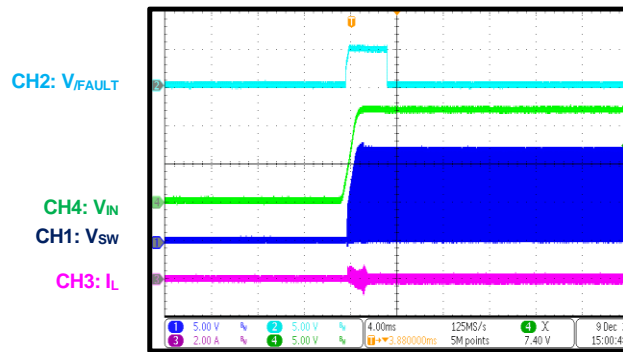
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Steady State**
 $I_{LED} = 1.5A$ 

**Start-Up through VIN**
 $I_{LED} = 1.5A$ 

**Shutdown through VIN**
 $I_{LED} = 1.5A$ 

**Start-Up through EN**
 $I_{LED} = 1.5A$ 

**Shutdown through EN**
 $I_{LED} = 1.5A$ 

**PWM Dimming Steady State**
 $f_{DIM} = 100Hz$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

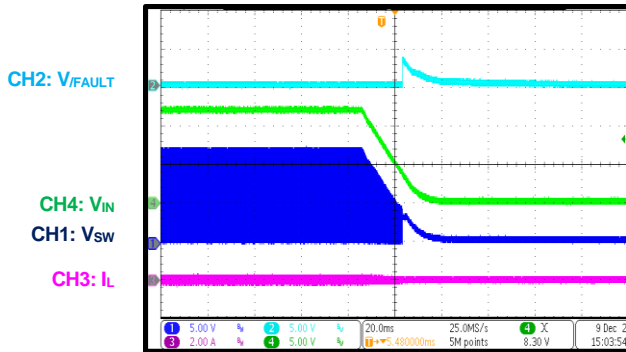
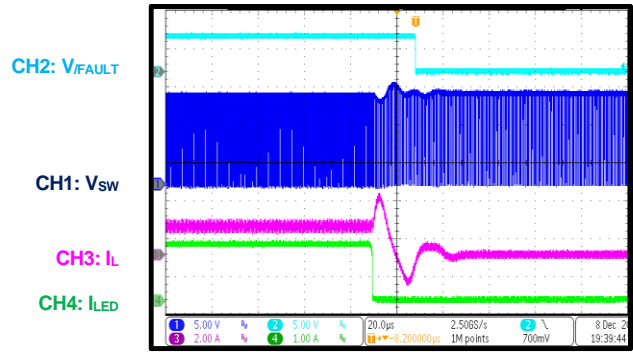
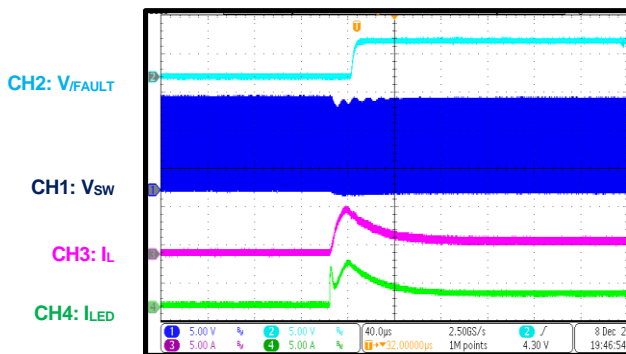
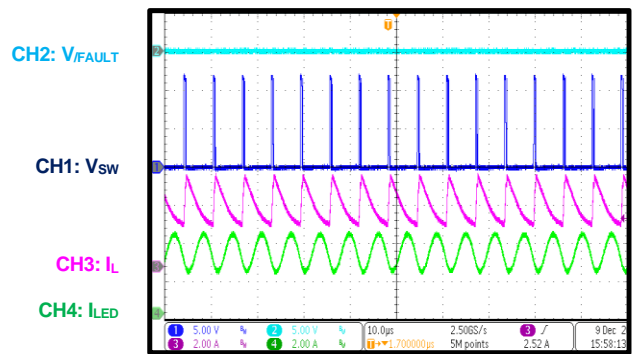
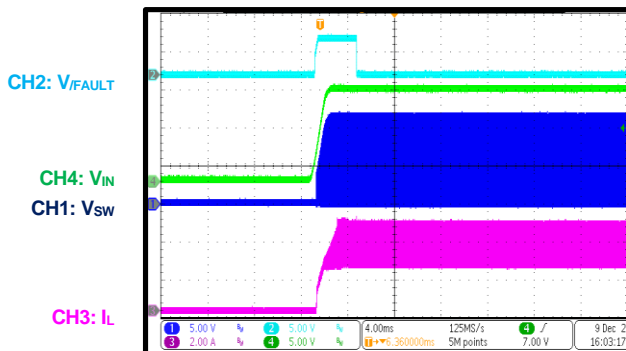
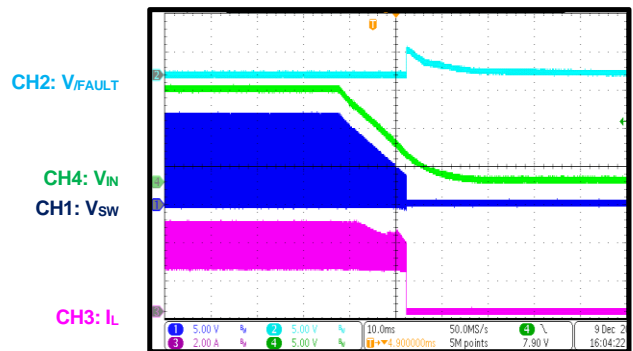
**PWM Dimming Steady State**
 $f_{DIM} = 500Hz$ 

**PWM Dimming Steady State**
 $f_{DIM} = 2kHz$ 

**PWM Dimming**

 Start-up through  $V_{IN}$ 

**PWM Dimming**

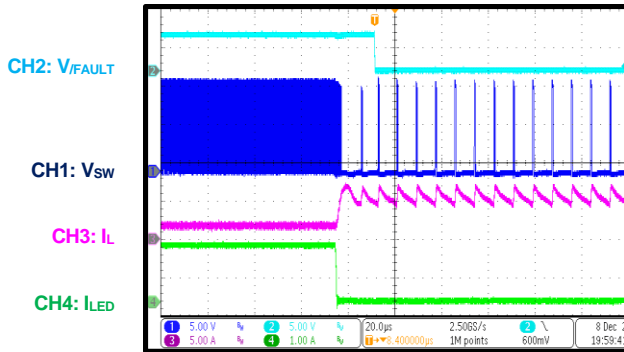
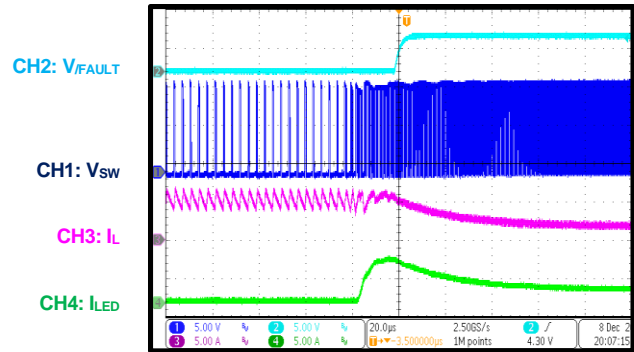
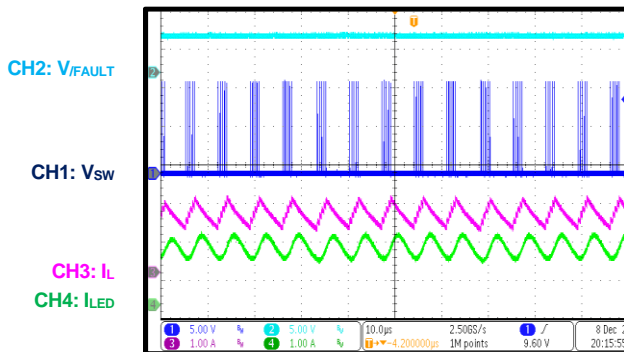
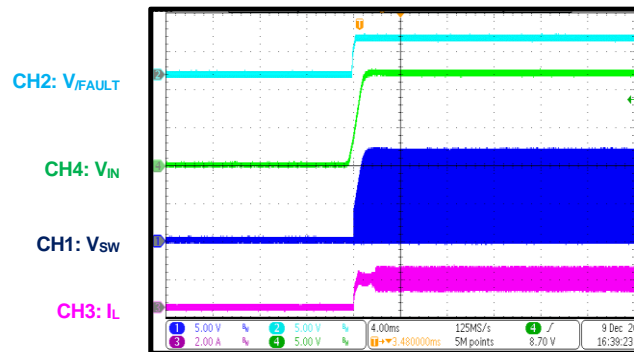
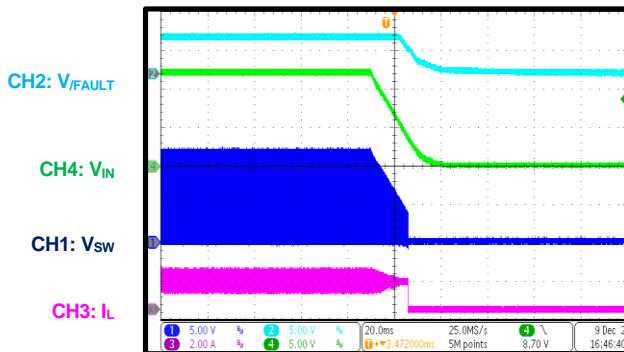
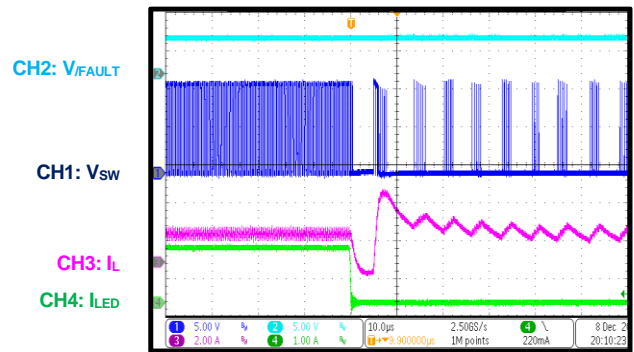
 Shutdown through  $V_{IN}$ 

**LED Open Steady State**

**LED Open Start-Up through  $V_{IN}$** 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

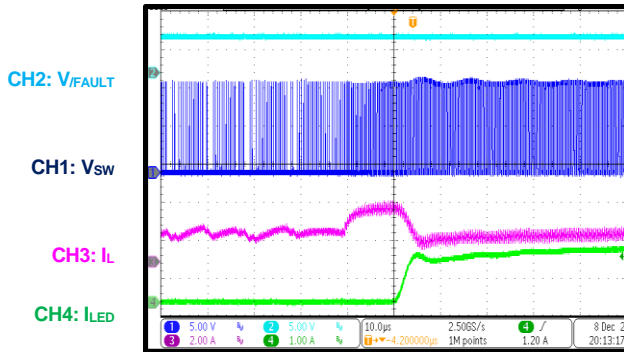
**LED Open Shutdown through VIN**

**LED Open Entry**

**LED Open Recovery**

**LED+ Short to Ground Steady State**

**LED+ Short to Ground Start-Up through VIN**

**LED+ Short to Ground Shutdown through VIN**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

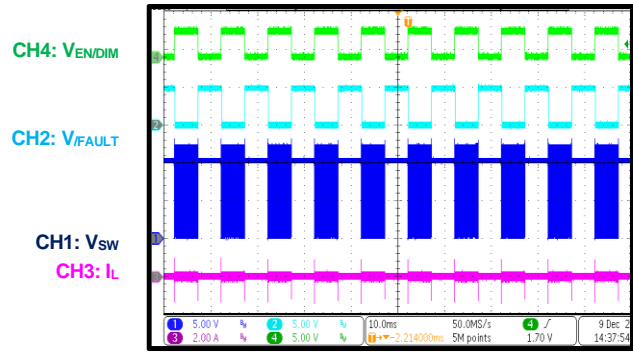
**LED+ Short to Ground Entry**

**LED+ Short to Ground Recovery**

**LED+ Short to LED- Steady State**

**LED+ Short to LED- Start-Up through VIN**

**LED+ Short to LED- Shutdown through VIN**

**LED+ Short to LED- Entry**


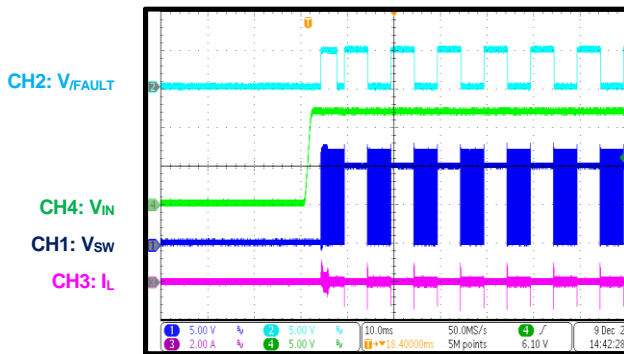
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

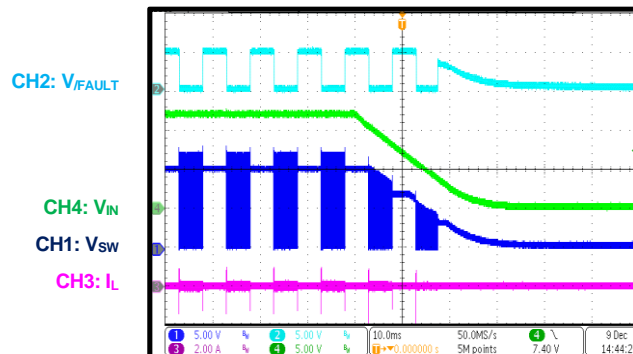
$V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  at  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**LED+ Short to LED- Recovery**

**PWM Dimming**

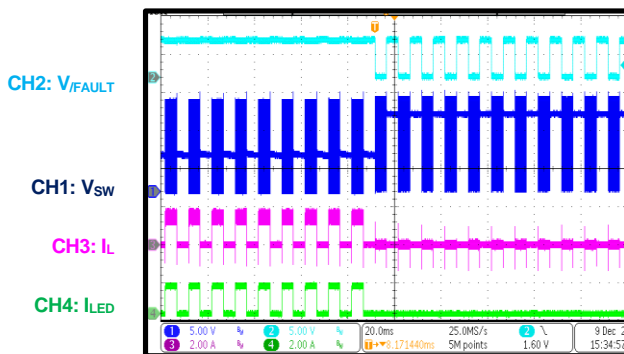
LED open steady state


**PWM Dimming**

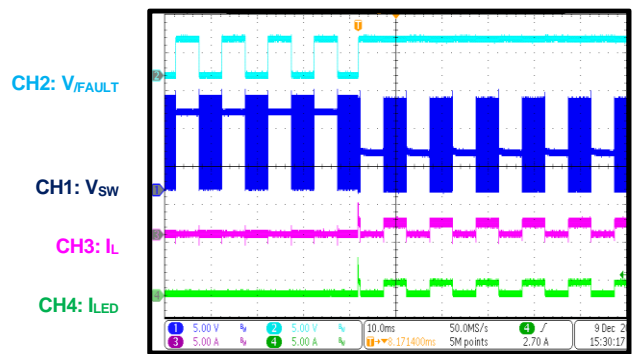
 LED open start-up through  $V_{IN}$ 

**PWM Dimming**

 LED open shutdown through  $V_{IN}$ 

**PWM Dimming**

LED open entry


**PWM Dimming**

LED open recovery

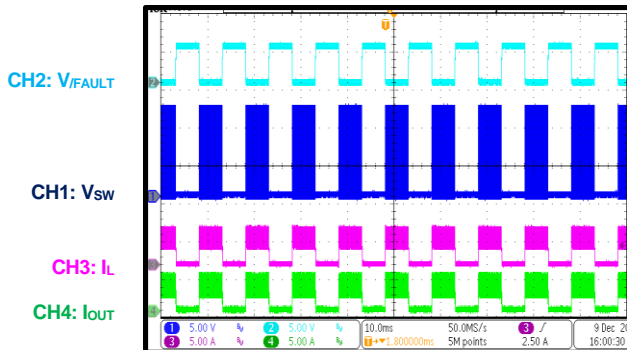


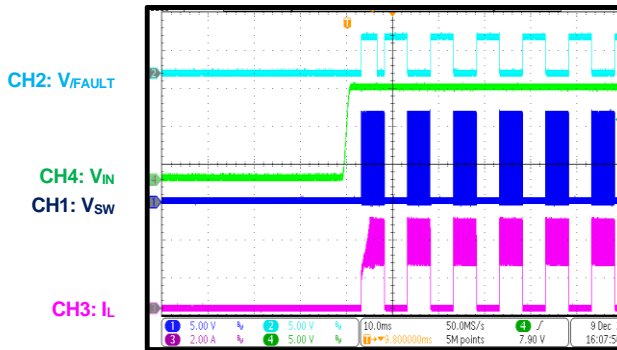


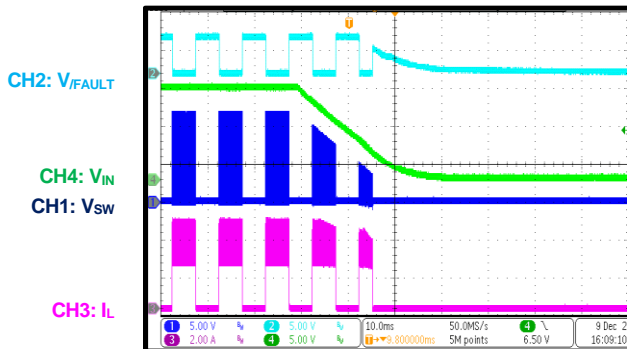
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

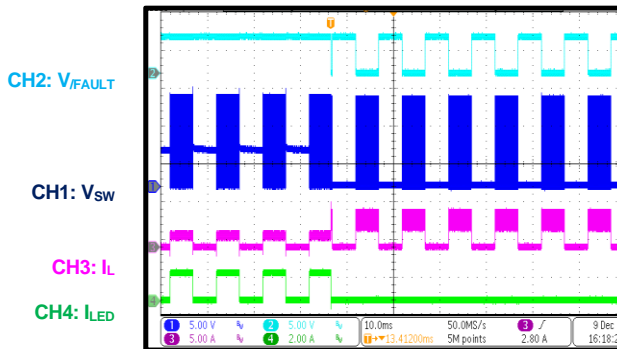
**PWM Dimming**

LED+ short to ground steady state

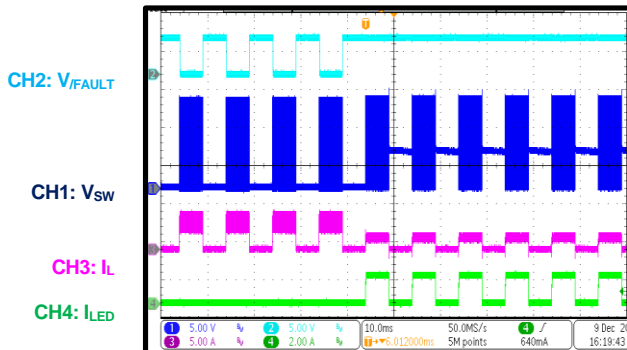

**PWM Dimming**

 LED+ short to ground start-up through  $V_{IN}$ 

**PWM Dimming**

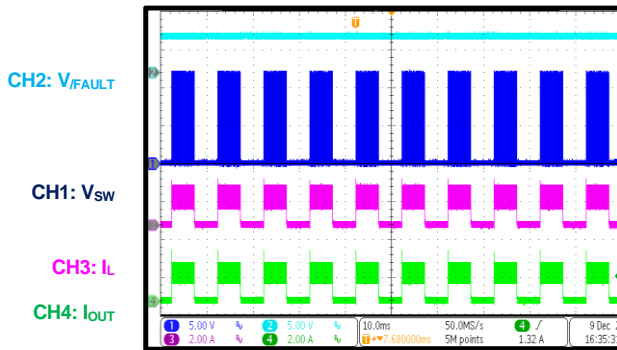
 LED+ short to ground shutdown through  $V_{IN}$ 

**PWM Dimming**

 LED+ short to ground entry,  $I_{PEAK} = 3A$ 

**PWM Dimming**

LED+ short to ground recovery


**PWM Dimming**

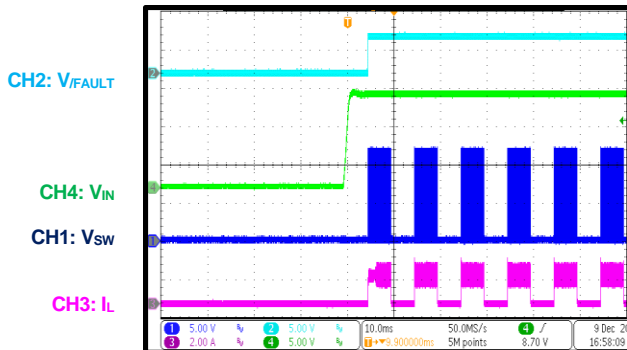
LED+ short to LED- steady state



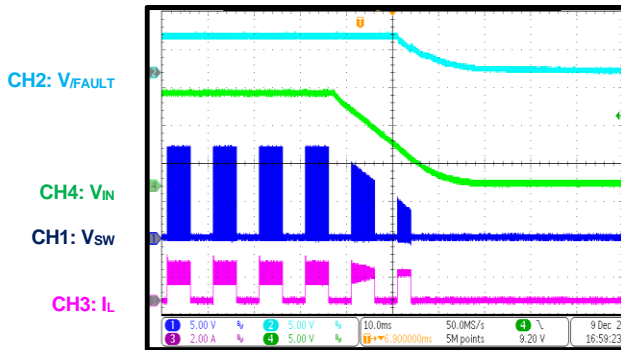
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 12V$ ,  $V_{LED+} - V_{LED-} = 2 \times 3.2V$  @  $I_{LED} = 1.5A$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**PWM Dimming**

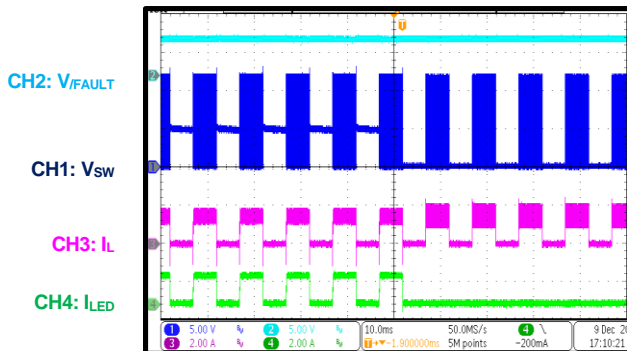
LED+ Short to LED- Input Power-On


**PWM Dimming**

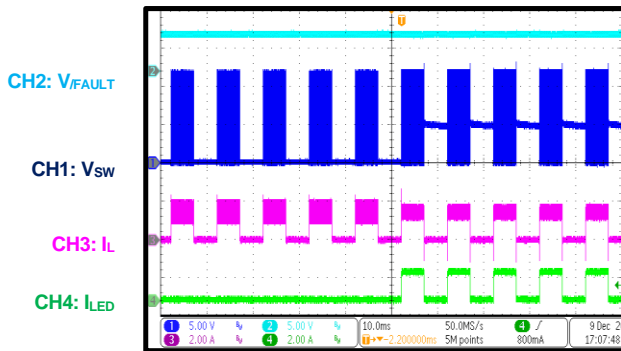
LED+ Short to LED- Input Power-Off


**PWM Dimming**

LED+ Short to LED- Entry


**PWM Dimming**

LED+ Short to LED- Recovery



## FUNCTIONAL BLOCK DIAGRAM

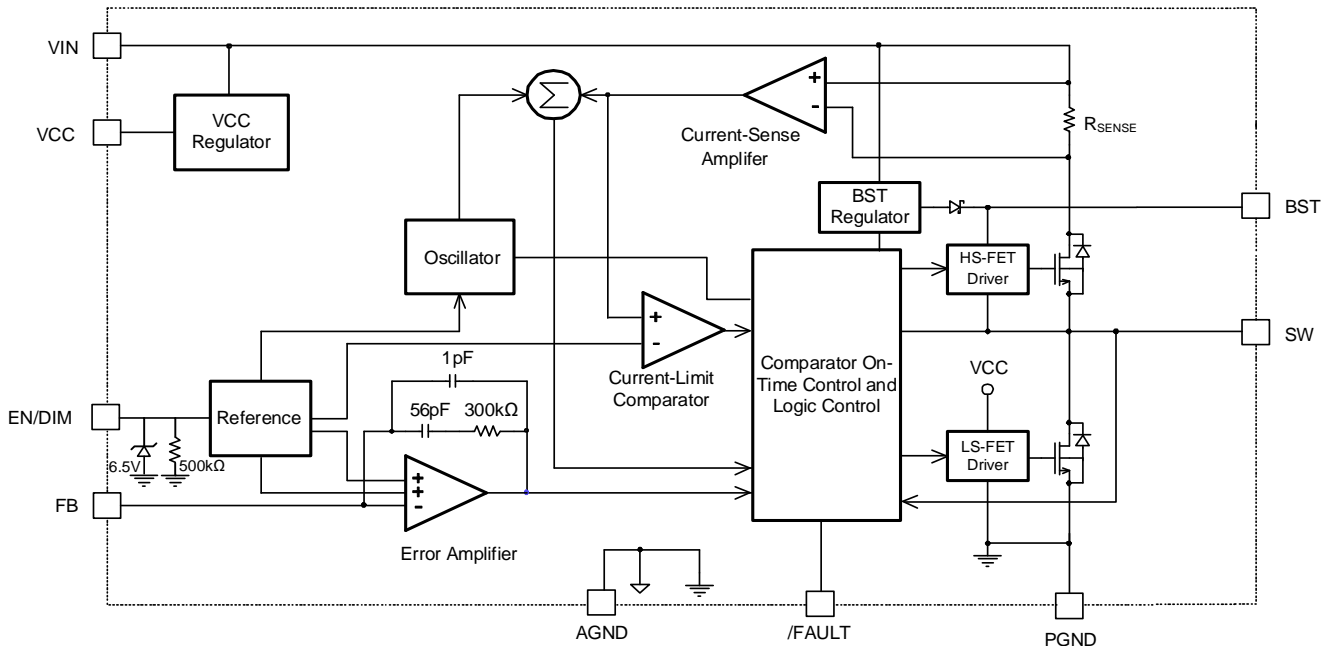


Figure 1: Functional Block Diagram

## OPERATION

The MPQ4425C is a high-frequency, synchronous, rectified, step-down, switch-mode white LED (WLED) driver with integrated internal power MOSFETs. It offers a compact solution that can achieve up to 1.5A of continuous output current ( $I_{OUT}$ ) across a wide 4V to 36V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation.

The MPQ4425C operates with a fixed-frequency in peak current control mode to regulate  $I_{OUT}$ . A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal comparator voltage ( $V_{COMP}$ ). The HS-FET remains off until the next clock cycle begins.

If  $I_{HS}$  does not reach the  $V_{COMP}$  value within 87% of one PWM cycle, the HS-FET turns off.

### Internal Regulator (VCC)

The 4.9V internal VCC regulator powers most of the internal circuitry. This regulator uses the  $V_{IN}$  pin as its input and operates across the entire  $V_{IN}$  range. If  $V_{IN}$  exceeds 4.9V, then VCC is in full regulation. If  $V_{IN}$  drops below 4.9V, then the output decreases with  $V_{IN}$ . Decouple VCC using a 0.1 $\mu$ F ceramic decoupling capacitor.

### Forced Continuous Conduction Mode (FCCM)

The MPQ4425C employs forced continuous conduction mode (FCCM) to ensure that the part operates with a fixed frequency at no loads to full loads. The advantage of FCCM is the controllable frequency and lower output voltage ripple ( $\Delta V_{OUT}$ ) at light loads.

### Frequency Foldback

The MPQ4425C enters frequency foldback once  $V_{IN}$  exceeds 21V. The frequency decreases to half its nominal value (1.1MHz).

Frequency foldback also occurs during soft start (SS) and short-circuit protection (SCP).

### Error Amplifier (EA)

The error amplifier (EA) compares the feedback (FB) voltage ( $V_{FB}$ ) to the internal reference ( $V_{REF}$ ) (0.195V), and outputs a current proportional to the difference between the two. This current

charges or discharges the internal compensation network to form  $V_{COMP}$ , which controls  $I_{HS}$ . The optimized internal compensation network minimizes the external component count and simplifies control loop design.

### Enable (EN) Control

EN/DIM is a control pin that enables and disabled the WLED driver. Pull EN/DIM high to turn the WLED driver on; pull EN/DIM low for 25ms or float EN/DIM to turn it off. An internal 500k $\Omega$  resistor connected between EN/DIM and ground allows EN/DIM to be floated.

EN/DIM is clamped internally via a 6.5V series Zener diode (see Figure 2).

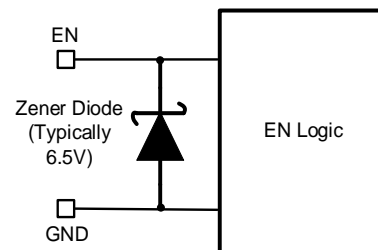


Figure 2: Zener Diode Connection

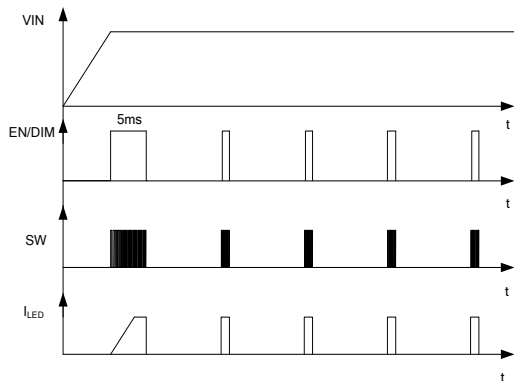
Connect the EN/DIM input to  $V_{IN}$  via a pull-up resistor ( $R_{EN/DIM\_PU}$ ) to limit the EN current ( $I_{EN}$ ) below 100 $\mu$ A. For example, if 12V are connected to  $V_{IN}$ , then  $R_{EN/DIM\_PU}$  should be  $\geq 55k\Omega$ .

Connecting EN/DIM to a voltage source without a pull-up resistor requires the voltage source amplitude to be limited to  $\leq 6V$ . This is to prevent damage to the Zener diode.

### Pulse-Width Modulation (PWM) Dimming

Apply an external 100Hz to 2kHz PWM waveform to the EN/DIM pin for PWM dimming. The average LED current ( $I_{LED}$ ) is proportional to the PWM duty. The minimum amplitude of the PWM signal is 1.8V. If the dimming signal is applied before the chip starts up, then the dimming signal's on time ( $t_{ON}$ ) should be longer than 5ms to ensure soft start finishes. Then  $I_{OUT}$  can be built, and after the pulse can decrease. If the dimming signal is applied after soft start finishes, then this 5ms limit is not required.

Figure 3 on page 21 shows the timing while PWM dimming is active.


**Figure 3: Timing with PWM Dimming**

### Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) protection protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage ( $V_{OUT}$ ) of the internal regulator (VCC).

### Internal Soft Start (SS)

Soft start (SS) prevents  $V_{OUT}$  from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage ( $V_{SS}$ ). If  $V_{SS}$  drops below the internal  $V_{REF}$ , then  $V_{SS}$  overrides  $V_{REF}$ , and the EA uses  $V_{SS}$  as the reference. If  $V_{SS}$  exceeds  $V_{REF}$ , the EA uses  $V_{REF}$  as the reference.

Float  $/FAULT$  during SS (unless thermal shutdown is triggered). If an LED short or open fault occurs during SS, then  $/FAULT$  is pulled high. If an LED short or open fault is still present once SS is complete,  $/FAULT$  is pulled low.

### Fault Indicator

The  $/FAULT$  pin is the open drain of a MOSFET, and is used for fault indication.  $/FAULT$  should be connected to VCC or another voltage source via a resistor (e.g. 100k $\Omega$ ).  $/FAULT$  is pulled high during normal operation. An LED short fault, LED open fault, or thermal shutdown occurs,  $/FAULT$  is pulled down to indicate a fault has occurred.

During a shutdown through EN,  $/FAULT$  is pulled high. During a start-up through EN,  $/FAULT$  is pulled low once SS is complete. If an LED short or open fault is still present once SS is complete or if thermal shutdown is triggered,  $/FAULT$  is pulled low.

During a shutdown with PWM dimming,  $/FAULT$

is pulled high. If an LED short or open fault is still present or if thermal shutdown is triggered during a start-up with PWM dimming,  $/FAULT$  is pulled low.

### Over-Current Protection (OCP)

The MPQ4425C employs cycle by cycle peak current limiting with valley-current detection. The inductor current ( $I_L$ ) is monitored while the high-side MOSFET (HS-FET) is on. If  $I_L$  exceeds the value set by  $V_{COMP}$ , then the HS-FET turns off. The low-side MOSFET (LS-FET) turns on to discharge the energy, and  $I_L$  decreases. The HS-FET remains off until the inductor valley current drops below the valley current limit (even while the internal clock pulse is high). If  $I_L$  does not drop below the valley current limit while the internal clock pulse is high, then the HS-FET skips the clock, and the switching frequency ( $f_{SW}$ ) decreases to half its nominal value. Both the peak and valley current limits prevent  $I_L$  runaway during an overload (OL) or short-circuit (SC) fault.

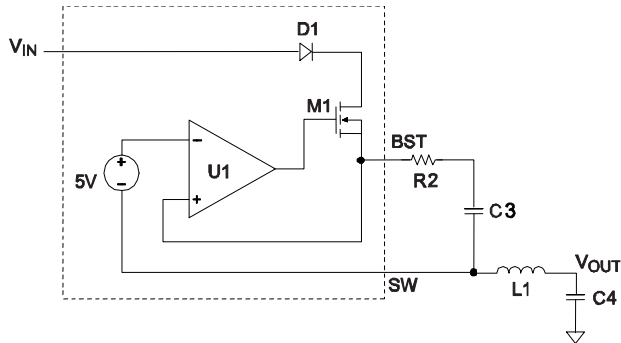
### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (typically 170°C), then the entire chip shuts down. Once the temperature drops below 140°C, the device initiates a new SS and resumes normal operation.

### Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor ( $C_{BST}$ ) powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a 2.2V rising threshold and a 150mV hysteresis. The  $V_{IN}$  pin regulates  $C_{BST}$  internally via D1, M1, C3, L1, and C4 (see Figure 4). If  $(V_{IN} - V_{SW})$  exceeds 5V, then the MPQ4425C (U1) regulates M1 to maintain the BST voltage ( $V_{BST}$ ) at 5V.

If  $V_{IN}$  exceeds  $V_{SW}$ ,  $C_{BST}$  can be charged. If the HS-FET is on, then  $V_{IN}$  and  $V_{SW}$  are almost the same, and  $C_{BST}$  cannot be charged. If the LS-FET is on, the  $(V_{IN} - V_{SW})$  can reach its maximum for fast charging. If there is no  $I_L$ , then  $V_{SW}$  equals  $V_{OUT}$ , and the difference between  $V_{IN}$  and  $V_{OUT}$  can charge  $C_{BST}$ . It is recommended to place a 20 $\Omega$  resistor between SW and  $C_{BST}$  to reduce the SW voltage spike.



**Figure 4: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

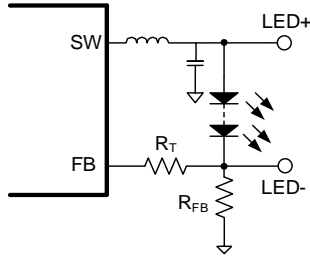
If both  $V_{IN}$  and  $V_{EN}$  exceed their respective thresholds, the part starts up. The reference block starts up first to generate a stable  $V_{REF}$  and current. Then the internal regulator starts up to provide a stable supply for the remaining circuitry.

Three events can shut down the chip:  $V_{IN}$  going low,  $V_{EN}$  going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid triggering any faults. Then  $V_{COMP}$  and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

## APPLICATION INFORMATION

### Setting the LED Current

The external FB resistor ( $R_{FB}$ ) sets  $I_{LED}$  (see Figure 5).



**Figure 5: Feedback Network**

$V_{FB}$  is 0.195V.  $I_{LED}$  can be calculated with Equation (1):

$$I_{LED} = \frac{0.195V}{R_{FB}} \quad (1)$$

**The resistor ( $R_T$ )** sets the loop bandwidth. A lower  $R_T$  results in a higher bandwidth, which can cause an insufficient phase margin. To ensure loop stability, choose an  $R_T$  value that provides an acceptable tradeoff between the bandwidth and phase margin. Table 1 lists recommended  $R_{FB}$  and  $R_T$  values for common outputs with 1- or 2-series LEDs.

**Table 1: Resistor Values for Common LED Currents**

$I_{LED}$ (A)	$R_{FB}$ (m $\Omega$ )	$R_T$ (k $\Omega$ )
0.5	400 (1%)	200 (1%)
1	200 (1%)	150 (1%)
1.5	133 (1%)	100 (1%)

### Selecting the Input Capacitor ( $C_{IN}$ )

The step-down converter has a discontinuous input current ( $I_{IN}$ ), and requires a capacitor to supply AC current to the converter while maintaining the DC  $V_{IN}$ . Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7 $\mu$ F to 10 $\mu$ F capacitor is sufficient. It is strongly recommended to use another low-value capacitor (e.g. 0.1 $\mu$ F) with a small package size (0603) to absorb high-frequency switching noise. Place this capacitor as close to the VIN pin and ground as possible.

Since the input capacitor ( $C_{IN}$ ) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in  $C_{IN}$  ( $I_{CIN}$ ) can be estimated with Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (3)$$

For simplification, choose a  $C_{IN}$  with an RMS current rating greater than half of the maximum load current ( $I_{LOAD\_MAX}$ ).

$C_{IN}$  can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1 $\mu$ F) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.  $V_{IN}$  ripple ( $\Delta V_{IN}$ ) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

### Selecting the Output Capacitor ( $C_{OUT}$ )

The output capacitor ( $C_{OUT}$ ) maintains the DC  $V_{OUT}$ . Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to reduce  $\Delta V_{OUT}$ .  $\Delta V_{OUT}$  can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}\right) \quad (5)$$

For ceramic capacitors, the capacitance dominates the impedance at  $f_{SW}$ , and causes the majority of  $\Delta V_{OUT}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at  $f_{SW}$ . For simplification,  $\Delta V_{OUT}$  can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The characteristics of  $C_{OUT}$  also affect the stability of the regulation system. The MPQ4425C can be optimized for a wide range of capacitances and ESR values.

### Selecting the Inductor

For most applications, a  $1\mu\text{H}$  to  $10\mu\text{H}$  inductor with a DC current rating of at least 25% greater than  $I_{LOAD\_MAX}$  is recommended. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower  $\Delta V_{OUT}$ ; however, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current ( $\Delta I_L$ ) to be approximately 30% of  $I_{LOAD\_MAX}$ . Then the inductance (L) can be calculated with Equation (8):

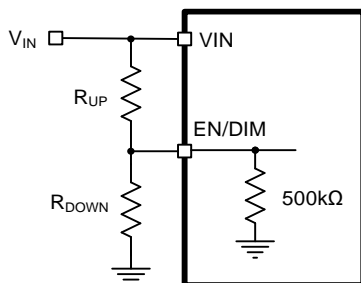
$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Choose  $\Delta I_L$  to be approximately 30% of  $I_{LOAD\_MAX}$ . The peak  $I_L$  ( $I_{L\_PEAK}$ ) can be calculated with Equation (9):

$$I_{LP} = I_{LED} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### Setting the $V_{IN}$ Under-Voltage Lockout (UVLO) Threshold

The MPQ4425C has an internal, fixed UVLO threshold. The rising threshold is 3.5V, and the falling threshold is about 3.1V. For applications that require a higher UVLO, place an external resistor divider between the  $V_{IN}$  and EN/DIM pins to raise the UVLO threshold (see Figure 6).



**Figure 6: Adjustable UVLO Using EN/DIM Divider**

The UVLO rising threshold ( $V_{IN\_UVLO\_RISING}$ ) can be calculated with Equation (10):

$$V_{IN\_UVLO\_RISING} = \left(1 + \frac{R_{UP}}{500\text{k}\Omega/R_{DOWN}}\right) \times V_{EN\_RISING} \quad (10)$$

Where  $V_{EN\_RISING}$  is 1.45V.

The UVLO falling threshold ( $V_{IN\_UVLO\_FALLING}$ ) can be calculated with and Equation (11):

$$V_{IN\_UVLO\_FALLING} = \left(1 + \frac{R_{UP}}{500\text{k}\Omega/R_{DOWN}}\right) \times V_{EN\_FALLING} \quad (11)$$

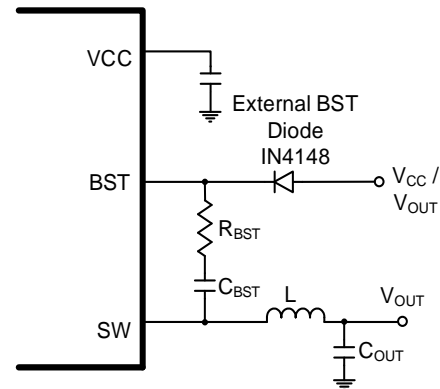
Where  $V_{EN\_FALLING}$  is 1V.

Ensure that  $R_{UP}$  has a large enough resistance to limit the current flowing through EN/DIM below  $100\mu\text{A}$ .

### BST Resistor and External BST Diode

It is recommended to place a  $20\Omega$  resistor in series with  $C_{BST}$  to reduce the SW voltage spike. A higher resistance results in a lower SW voltage spike; however, a higher resistance can decrease efficiency.

If the duty cycle is high ( $>65\%$ ), then adding an external BST diode can enhance the efficiency of the regulator. A 2.5V to 5V power supply can be used to power the external BST diode.  $V_{CC}$  and  $V_{OUT}$  are the best choices supplying the circuit (see Figure 7).



**Figure 7: Optional External BST Diode**

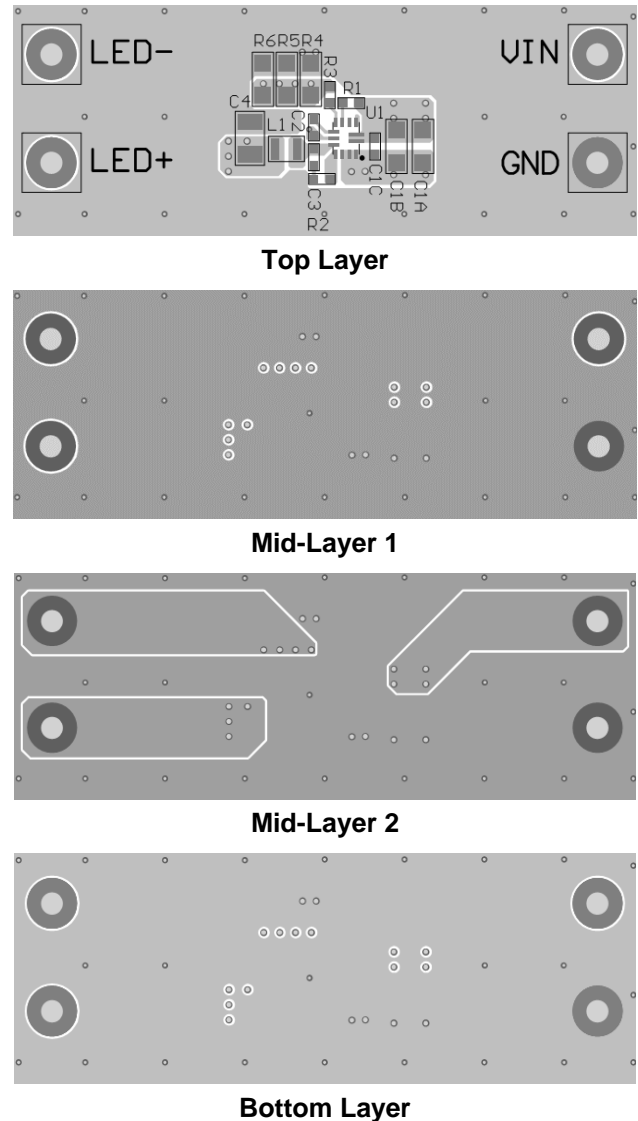
The recommended external BST diode is the IN4148, and the recommended  $C_{BST}$  value is between  $0.1\mu\text{F}$  and  $1\mu\text{F}$ .



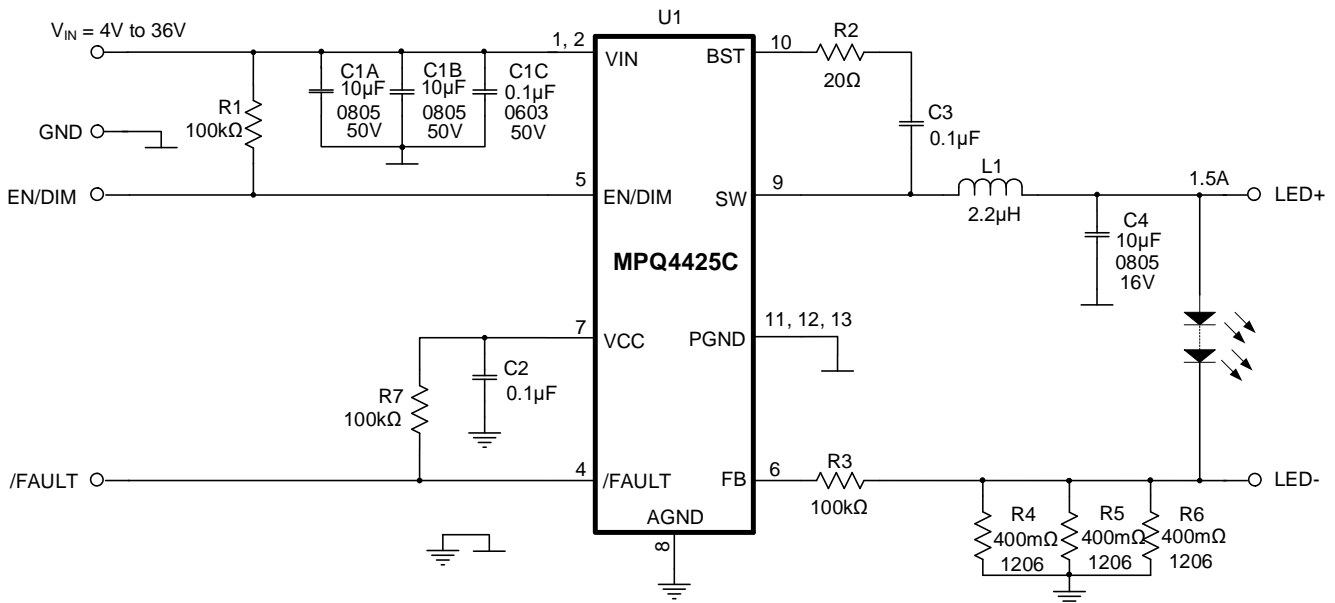
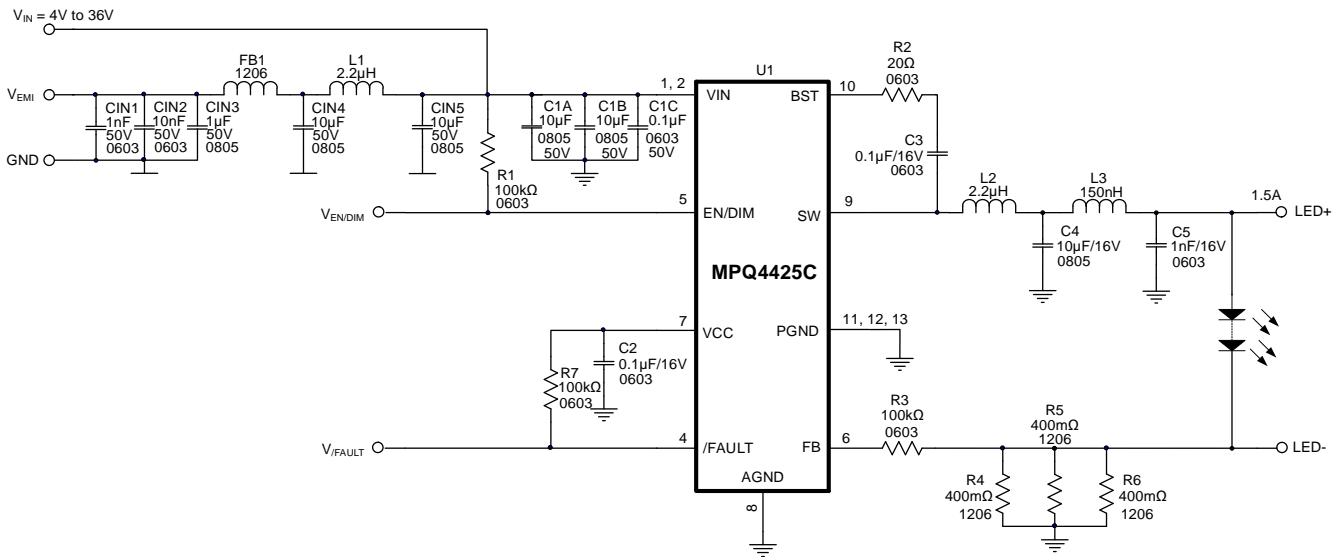
**PCB Layout Guidelines** <sup>(12)</sup>

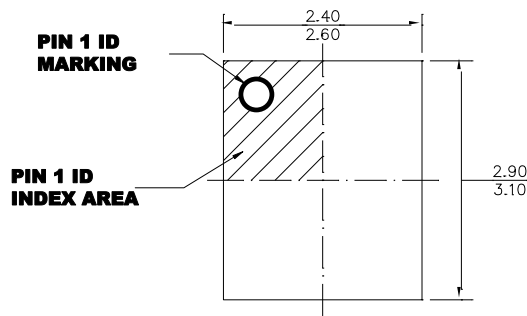
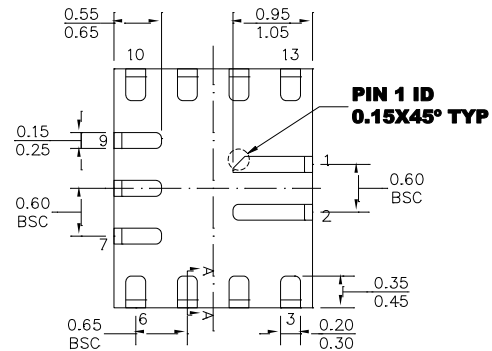
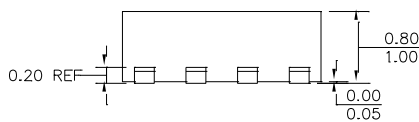
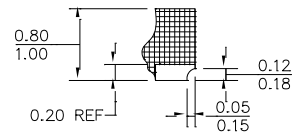
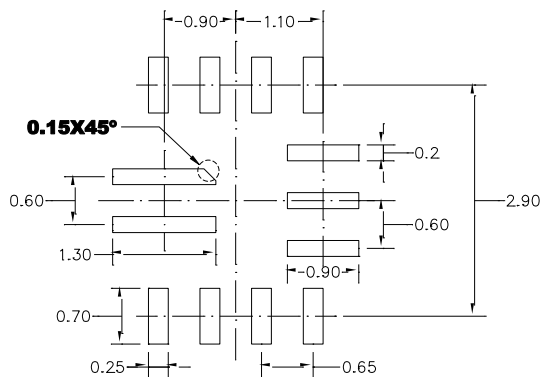
Efficient PCB layout (especially placement of  $C_{IN}$ ) is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

1. Connect PGND to a large ground plane. If the bottom layer of the PCB is a ground plane, add multiple vias near PGND.
2. Connect the high-current paths at PGND and VIN using short, direct, and wide traces.
3. Place the ceramic input capacitors – especially the small-packaged input bypass capacitor (0603) – as close to the VIN and PGND pins as possible to minimize high-frequency noise.
4. Keep the connection between the input capacitor and VIN as short and wide as possible.
5. Place the VCC capacitor as close to the VCC and GND pins as possible.
6. Route SW and BST away from sensitive analog areas, such as FB.
7. Place the feedback resistors close to the IC to keep the FB trace as short as possible.
8. Connect the power planes to the internal layers using multiple vias.

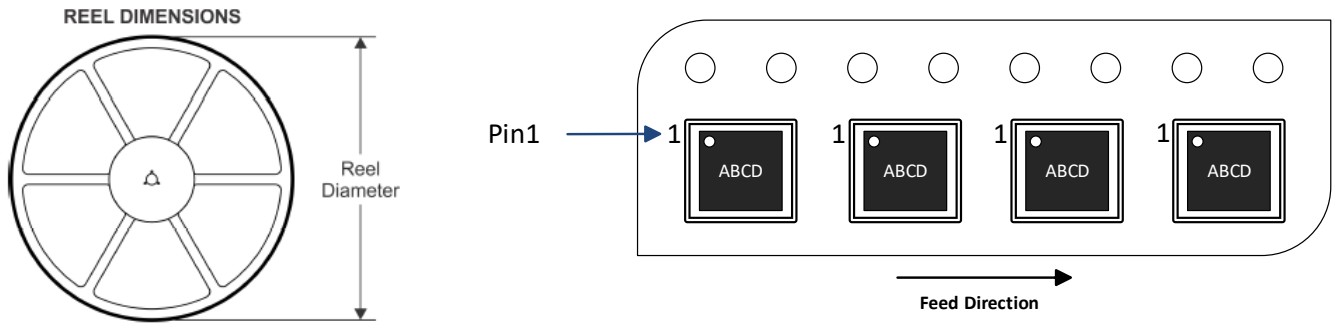

**Figure 8: Recommended PCB Layout**
**Note:**

12) The recommended PCB layout is based on Figure 9 on page 26.

**TYPICAL APPLICATION CIRCUITS**

**Figure 9: Typical Application Circuit ( $I_{LED} = 1.5A$ )**

**Figure 10: Typical Application Circuit with EMI Filters ( $I_{LED} = 1.5A$ )**

**PACKAGE INFORMATION**
**QFN-13 (2.5mmx3mm)**
**Wettable Flank**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

**SECTION A-A**

**RECOMMENDED LAND PATTERN**
**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

**CARRIER INFORMATION**


Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4425CGQBE-AEC1	QFN-13 (2.5mmx3mm)	5000	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/17/2022	Initial Release	-

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