

## FEATURES

**ADG901** absorptive switch

**ADG902** reflective switch

Enables user to pass dc signals up to 0.5 V without dc blocking capacitor

Operational from 0 Hz up to 4.5 GHz at  $-3$  dB frequency

40 dB off isolation at 1 GHz typical

0.8 dB insertion loss at 1 GHz typical

17 dBm P1dB at 1 GHz typical

Available in 3 mm  $\times$  3 mm, 8-lead MSOP and 8-lead LFCSP

$<1$   $\mu$ A power consumption

CMOS/LVTTL control logic

Specified at 1.65 V to 2.75 V

## APPLICATIONS

Wireless communications

General purpose RF switching

Dual-band applications

High speed filter selection

Digital transceiver front-end switch

IF switching

Tuner modules

Antenna diversity switching list

## GENERAL DESCRIPTION

The **ADG901/ADG902** are wideband switches that use a complementary metal-oxide semiconductor (CMOS) process to provide high isolation and low insertion loss to 1 GHz. The **ADG901** is an absorptive (matched) switch with  $50\ \Omega$  terminated shunt legs, while the **ADG902** is a reflective switch. These devices are designed such that the isolation is high over the dc to 1 GHz frequency range. These switches enable the user to pass dc signals up to 0.5 V without the use of a dc blocking capacitor. They have on-board CMOS control logic, thus eliminating the need for external controlling circuitry. The control inputs are both CMOS and LVTTL compatible. The low power consumption of these CMOS devices makes them ideally suited to wireless applications and general-purpose high frequency switching.

## FUNCTIONAL BLOCK DIAGRAMS

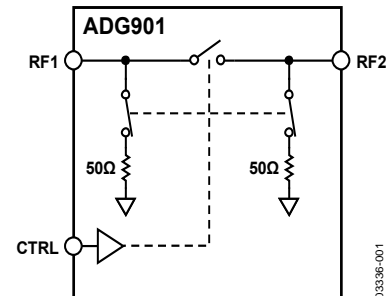


Figure 1. ADG901

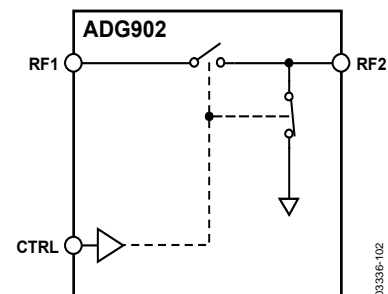


Figure 2. ADG902

## PRODUCT HIGHLIGHTS

- 40 dB Off Isolation at 1 GHz
- 0.8 dB Insertion Loss at 1 GHz
- 17 dBm P1dB at 1 GHz

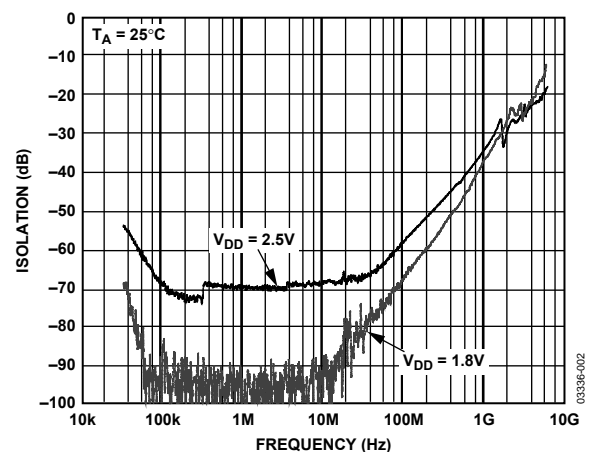


Figure 3. Off Isolation vs. Frequency

Rev. D

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## REVISION HISTORY

### 11/2017—Rev. C to Rev. D

Deleted Figure 3; Renumbered Sequentially.....	1
Added Figure 2; Renumbered Sequentially .....	1
Changes to Features Section, Figure 1, General Description Section, and Product Highlights Section .....	1
Deleted Endnote 4, Table 1; Renumbered Sequentially .....	3
Change to $-3$ dB Frequency Parameter, Table 1.....	3
Added Table 2; Renumbered Sequentially .....	4
Changes to Table 3.....	5
Change to Figure 4 .....	6
Changes to Ordering Guide .....	12

### 5/2016—Rev. B to Rev. C

Changes to Figure 4 and Table 3.....	5
Added Figure 5; Renumbered Sequentially .....	5
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	13

### 10/2005—Rev. A to Rev. B

Changes to Figure 1.....	1
Changes to Table 1.....	3
Changes to Ordering Guide .....	12

### 10/2004—Rev. 0 to Rev. A

Changes to Features .....	1
Changes to Product Highlights .....	1
Changes to Specifications.....	2
Changes to Ordering Guide .....	3
Change to ADG9xx Evaluation Board Section .....	9
Changes to Ordering Guide .....	10

### 8/2003—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 1.65\text{ V to }2.75\text{ V}$ ,  $GND = 0\text{ V}$ , input power = 0 dBm, all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified.<sup>1</sup>

Table 1.

Parameter	Symbol	Test Conditions/Comments	B Version			Unit
			Min	Typ <sup>2</sup>	Max	
<b>AC ELECTRICAL CHARACTERISTICS</b>						
Operating Frequency <sup>3</sup>			DC		2.5	GHz
–3 dB Frequency				4.5		GHz
Input Power		0 V dc bias			7	dBm
		0.5 V dc bias			16	dBm
Insertion Loss	$S_{21}, S_{12}$	DC to 100 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$		0.4	0.7	dB
		500 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$		0.5	0.8	dB
		1000 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$		0.8	1.25	dB
Isolation—RF1 to RF2 CP Package	$S_{21}, S_{12}$	100 MHz	60	61		dB
		500 MHz	43	45		dB
		1000 MHz	34	40		dB
Isolation—RF1 to RF2 RM Package	$S_{21}, S_{12}$	100 MHz	51	60		dB
		500 MHz	37.5	47		dB
		1000 MHz	31	37		dB
Return Loss (On Channel)	$S_{11}, S_{22}$	DC to 100 MHz	20	28		dB
		500 MHz	23	29		dB
		1000 MHz	25	28		dB
Return Loss (Off Channel)	$S_{11}, S_{22}$	DC to 100 MHz	18	23		dB
		500 MHz	17	21		dB
		1000 MHz	15	19		dB
On Switching Time	$t_{ON}$	50% CTRL to 90% RF		3.6	6	ns
Off Switching Time	$t_{OFF}$	50% CTRL to 10% RF		5.8	9.5	ns
Rise Time	$t_{RISE}$	10% to 90% RF		3.1	5.5	ns
Fall Time	$t_{FALL}$	90% to 10% RF		6.0	8.5	ns
1 dB Compression	P1dB	1000 MHz		17		dBm
Third-Order Intermodulation Intercept	IP3	900 MHz/901 MHz, 4 dBm	28.5	36		dBm
Video Feedthrough <sup>4</sup>				2.5		mV p-p
<b>DC ELECTRICAL CHARACTERISTICS</b>						
Input High Voltage	$V_{INH}$	$V_{DD} = 2.25\text{ V to }2.75\text{ V}$	1.7			V
	$V_{INH}$	$V_{DD} = 1.65\text{ V to }1.95\text{ V}$	0.65 $V_{DD}$			V
Input Low Voltage	$V_{INL}$	$V_{DD} = 2.25\text{ V to }2.75\text{ V}$			0.7	V
	$V_{INL}$	$V_{DD} = 1.65\text{ V to }1.95\text{ V}$			0.35 $V_{DD}$	V
Input Leakage Current	$I_I$	$0 \leq V_{IN} \leq 2.75\text{ V}$		$\pm 0.1$	$\pm 1$	$\mu\text{A}$
<b>CAPACITANCE</b>						
RF1/RF2, RF Port On Capacitance	$C_{RF\text{ on}}$	$f = 1\text{ MHz}$		1.2		pF
CTRL Input Capacitance	$C_{CTRL}$	$f = 1\text{ MHz}$		2.1		pF
<b>POWER REQUIREMENTS</b>						
$V_{DD}$			1.65		2.75	V
Quiescent Power Supply Current	$I_{DD}$	Digital inputs = 0 V or $V_{DD}$		0.1	1	$\mu\text{A}$

<sup>1</sup> Temperature range for B version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup> Typical values are at  $V_{DD} = 2.5\text{ V}$  and  $25^\circ\text{C}$ , unless otherwise specified.

<sup>3</sup> Point at which insertion loss degrades by 1 dB.

<sup>4</sup> The dc transience at the output of any port of the switch when the control voltage is switched from high to low or low to high in a  $50\ \Omega$  test setup, measured with 1 ns rise time pulses and 500 MHz bandwidth.

**CONTINUOUS CURRENT PER CHANNEL**

Table 2.

Parameter	25°C	85°C	105°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL						
8-Lead LFCSP						$\theta_{JA} = 48^{\circ}\text{C/W}$ , dc bias = 0.5 V
$V_{DD} = 2.75\text{ V}, V_{SS} = 0\text{ V}$	70	7	3.85	2.8	mA maximum	
$V_{DD} = 1.65\text{ V}, V_{SS} = 0\text{ V}$	56	7	3.85	2.1	mA maximum	
8-lead MSOP						$\theta_{JA} = 206^{\circ}\text{C/W}$ , dc bias = 0.5 V
$V_{DD} = 2.75\text{ V}, V_{SS} = 0\text{ V}$	51.1	7	3.85	2.8	mA maximum	
$V_{DD} = 1.65\text{ V}, V_{SS} = 0\text{ V}$	39.9	7	3.85	2.1	mA maximum	

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Rating
$V_{DD}$ to GND	-0.5 V to +4 V
Inputs to GND	-0.5 V to $V_{DD} + 0.3\text{ V}^1$
Continuous Current	Data <sup>2</sup> + 15%
Input Power <sup>3</sup>	18 dBm
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
$\theta_{JA}$ Thermal Impedance	
MSOP Package	206°C/W
LFCSP Package	
2-Layer Board	84°C/W
4-Layer Board	48°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
ESD	1 kV

<sup>1</sup> RF1/RF2 off port inputs to ground: -0.5 V to  $V_{DD} - 0.5\text{ V}$ .

<sup>2</sup> See Table 2.

<sup>3</sup> Input power is tested with switch in both open and close position. Power is applied on RFx, while RFC is terminated to a 50  $\Omega$  resistor to GND.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

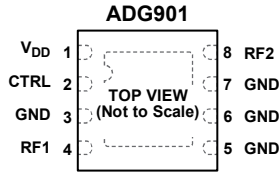
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



**NOTES**  
 1. THE LFCSP PACKAGE HAS AN EXPOSED PAD. THE EXPOSED PAD MUST BE TIED TO THE SUBSTRATE, GND.

Figure 4. 8-Lead LFCSP Pin Configuration

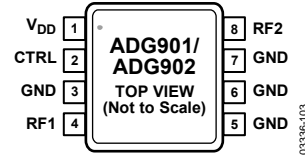


Figure 5. 8-Lead MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Power Supply Input. These devices can be operated from 1.65 V to 2.75 V; decouple V <sub>DD</sub> to GND.
2	CTRL	CMOS or LVTTTL Logic Level. CTRL input must not exceed V <sub>DD</sub> . Logic 0: RF1 isolated from RF2. Logic 1: RF1 to RF2.
3, 5, 6, 7	GND	Ground Reference Point for All Circuitry on the Device.
4	RF1	RF1 Port.
8	RF2	RF2 Port.
	EPAD	Exposed Pad. The LFCSP package has an exposed pad. The exposed pad must be tied to the substrate, GND.

Table 5. Truth Table

CTRL	Signal Path
0	RF1 isolated from RF2
1	RF1 to RF2

TYPICAL PERFORMANCE CHARACTERISTICS

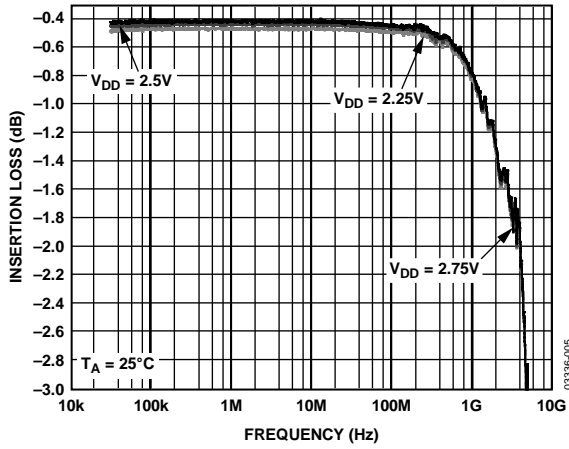


Figure 6. Insertion Loss vs. Frequency over Supplies (S12 and S21)

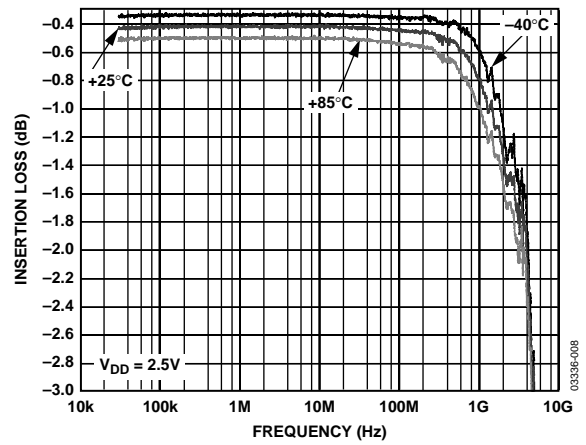


Figure 9. Insertion Loss vs. Frequency over Temperature (S12 and S21)

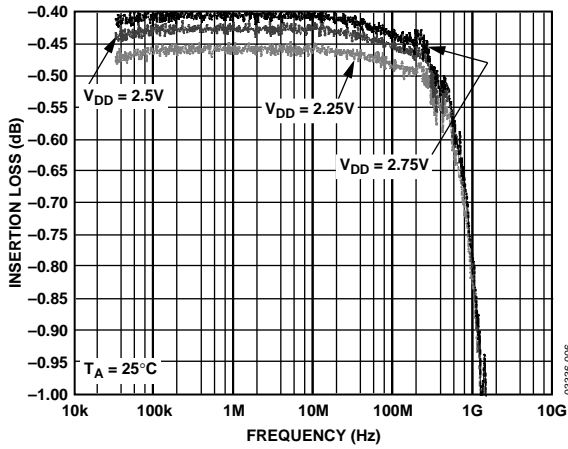


Figure 7. Insertion Loss vs. Frequency over Supplies (S12 and S21) (Zoomed Figure 6 Plot)

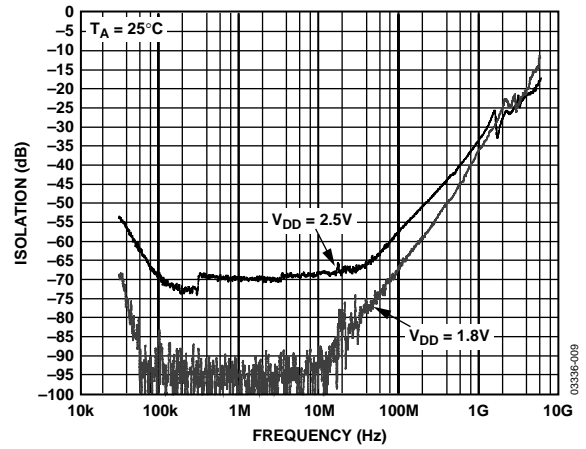


Figure 10. Off Isolation vs. Frequency over Supplies (S12 and S21)

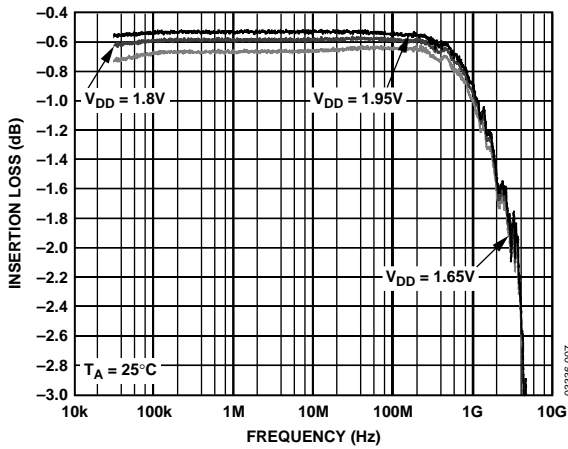


Figure 8. Insertion Loss vs. Frequency over Supplies (S12 and S21)

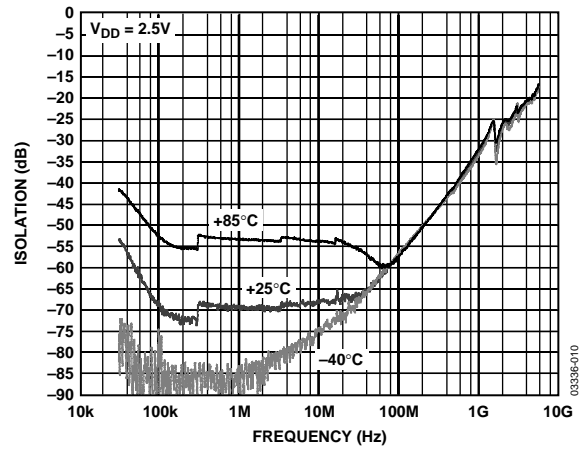


Figure 11. Off Isolation vs. Frequency over Temperature (S12 and S21)

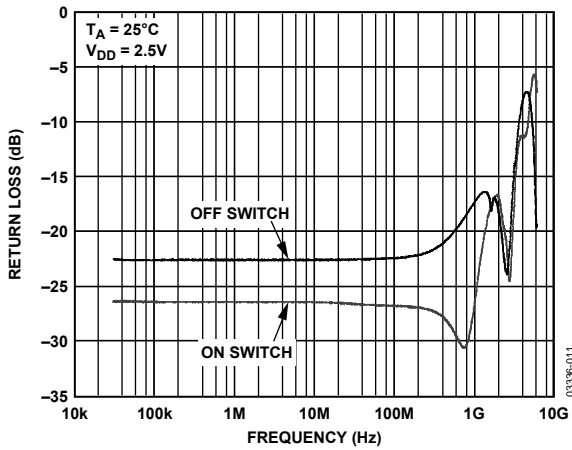


Figure 12. Return Loss vs. Frequency (S11)

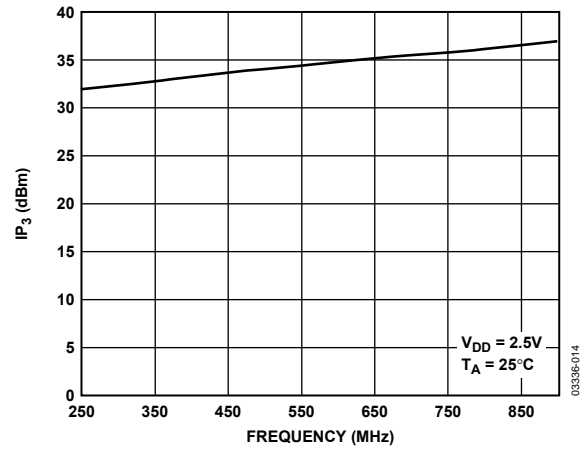


Figure 15. IP<sub>3</sub> vs. Frequency

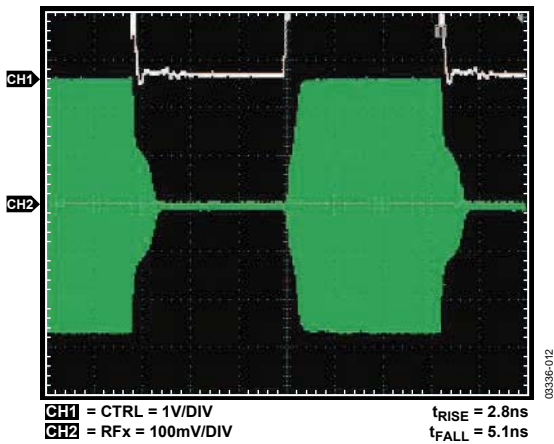


Figure 13. Switch Timing

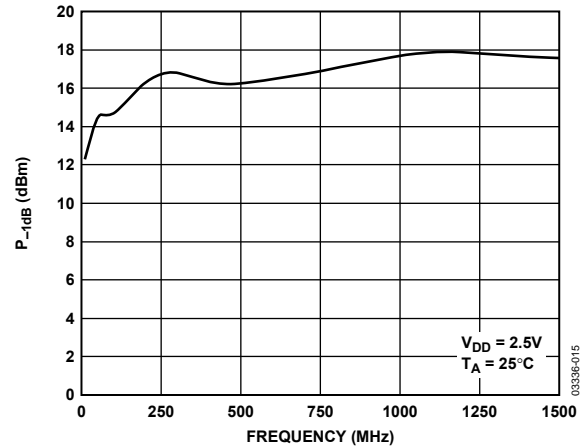


Figure 16. P<sub>-1dB</sub> vs. Frequency

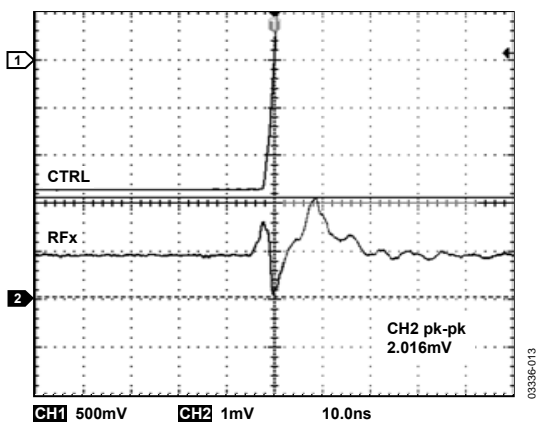


Figure 14. Video Feedthrough



## TERMINOLOGY

**V<sub>DD</sub>**

Most positive power supply potential.

**I<sub>DD</sub>**

Positive supply current.

**GND**

Ground (0 V) reference.

**CTRL**

Logic control input.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

**C<sub>IN</sub>**

Digital input capacitance.

**t<sub>ON</sub>**

Delay between applying the digital control input and the output switching on.

**t<sub>OFF</sub>**

Delay between applying the digital control input and the output switching off.

**t<sub>RISE</sub>**

Rise time. Time for the RF signal to rise from 10% to 90% of the on level.

**t<sub>FALL</sub>**

Fall time. Time for the RF signal to fall from 90% to 10% of the on level.

### Off Isolation

The attenuation between input and output ports of the switch when the switch control voltage is in the off condition.

### Insertion Loss

The attenuation between input and output ports of the switch when the switch control voltage is in the on condition.

### P1dB

1 dB compression point. The RF input power level at which the switch insertion loss increases by 1 dB over its low level value. It is a measure of how much power the on switch can handle before the insertion loss increases by 1 dB.

### IP3

Third-order intermodulation intercept. This is a measure of the power in false tones that occur when closely spaced tones are passed through a switch, whereby the nonlinearity of the switch causes these false tones to be generated.

### Return Loss

The amount of reflected power relative to the incident power at a port. Large return loss indicates good matching. By measuring return loss the voltage standing wave ratio VSWR can be calculated from conversion charts. The VSWR indicates the degree of matching present at a switch RF port.

### Video Feedthrough

The spurious signals present at the RF ports of the switch when the control voltage is switched from high to low or low to high without an RF signal present.

TEST CIRCUITS

Similar setups for ADG902.

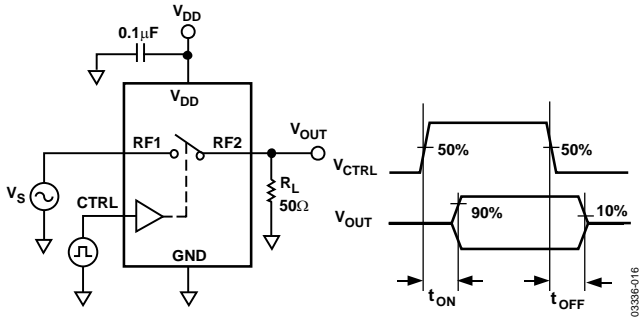


Figure 17. Switching Timing:  $t_{ON}$ ,  $t_{OFF}$

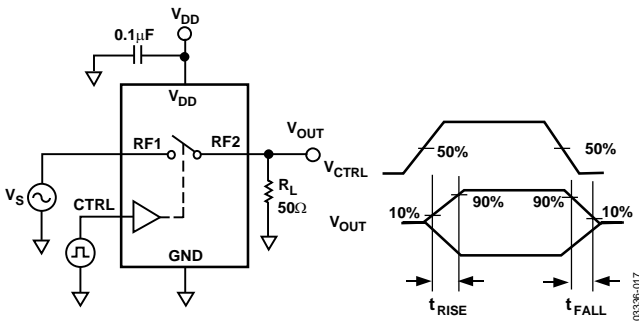


Figure 18. Switch Timing:  $t_{RISE}$ ,  $t_{FALL}$

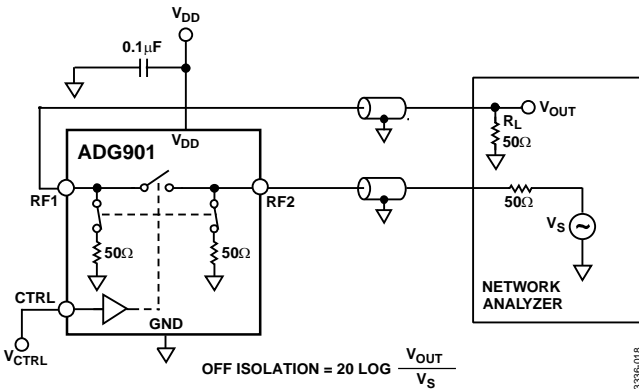


Figure 19. Off Isolation

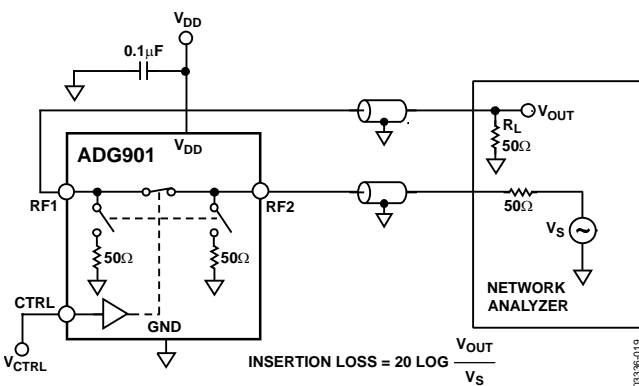


Figure 20. Insertion Loss

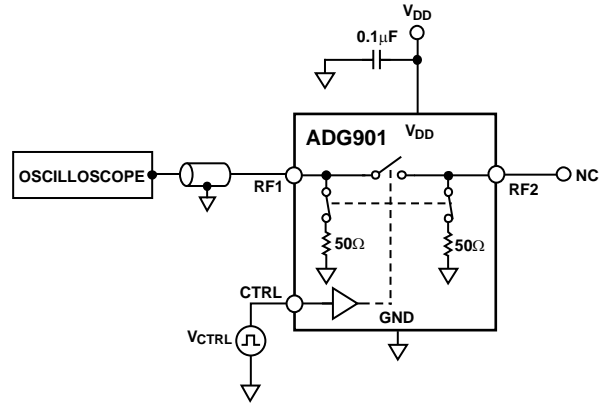


Figure 21. Video Feedthrough

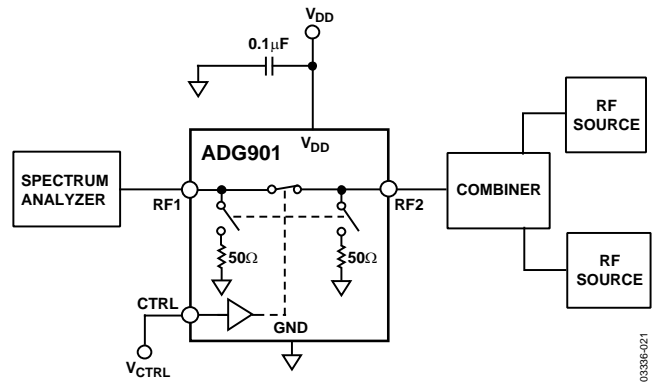


Figure 22. IP3

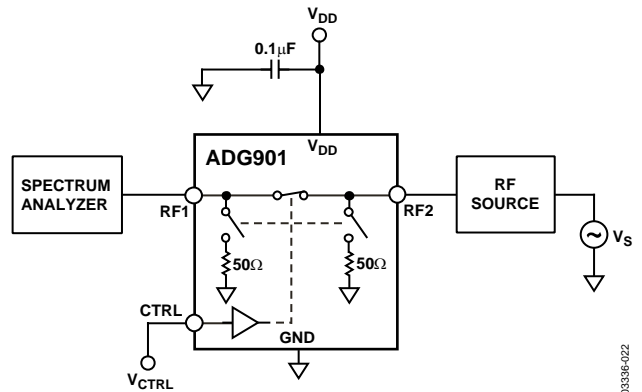


Figure 23. P1dB

## APPLICATIONS INFORMATION

The [ADG901/ADG902](#) are ideal solutions for low power, high frequency applications. The low insertion loss, high isolation between ports, low distortion, and low current consumption of these parts make them excellent solutions for many high frequency switching applications.

Applications include switching between high frequency filters, ASK generators, and FSK generators.

### ABSORPTIVE vs. REFLECTIVE SWITCHES

The [ADG901](#) is an absorptive (matched) switch with  $50\ \Omega$  terminated shunt legs and the [ADG902](#) is a reflective switch with  $0\ \Omega$  terminated shunts to ground. The [ADG901](#) absorptive switch has a good VSWR on each port, regardless of the switch mode. Use an absorptive switch when there is a need for a good VSWR that is looking into the port but not passing the through signal to the common port. The [ADG901](#) is therefore ideal for applications that require minimum reflections back to the RF source. It also ensures that the maximum power is transferred to the load.

The [ADG902](#) reflective switch is suitable for applications where high off port VSWR does not matter and the switch has some other desired performance feature. It can be used in many applications, including high speed filter selection. In most cases, an absorptive switch can be used instead of a reflective switch, but not vice versa.

### ADG901/ADG902 EVALUATION BOARD

The ADG901/ADG902 evaluation board allows designers to evaluate the high performance wideband switches with a minimum of effort. To prove that these devices meet user requirements, the user requires only a power supply and a network analyzer along with the evaluation board. An application note is available with the evaluation board and provides complete information on operating the evaluation board.

The RF1 port (see Figure 24) is connected through a 50 Ω transmission line to the top left SMA Connector J1. RF2 is connected through a 50 Ω transmission line to the top SMA Connector J2. J3 is connected to GND. A through transmission line connects J4 and J5 and this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a 4-layer, FR4 material with a dielectric constant of 4.3 and an overall thickness of 0.062 inches. Two ground layers with grounded planes provide ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.052 inches, clearance to ground plane of 0.030 inches, dielectric thickness of 0.029 inches, and a metal thickness of 0.014 inches.

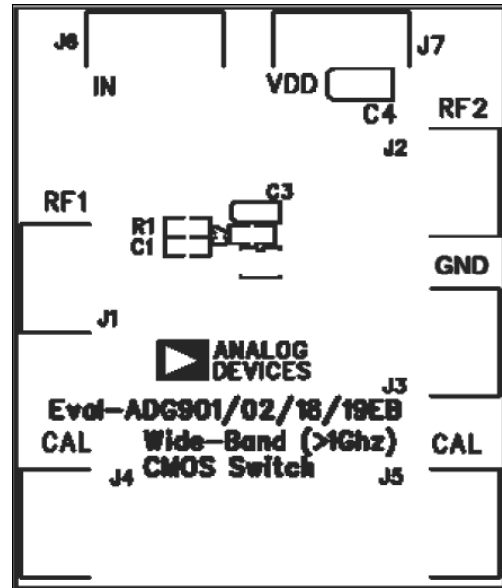
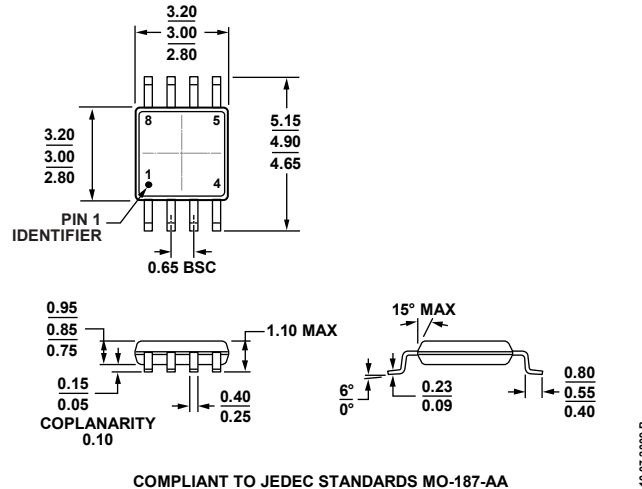


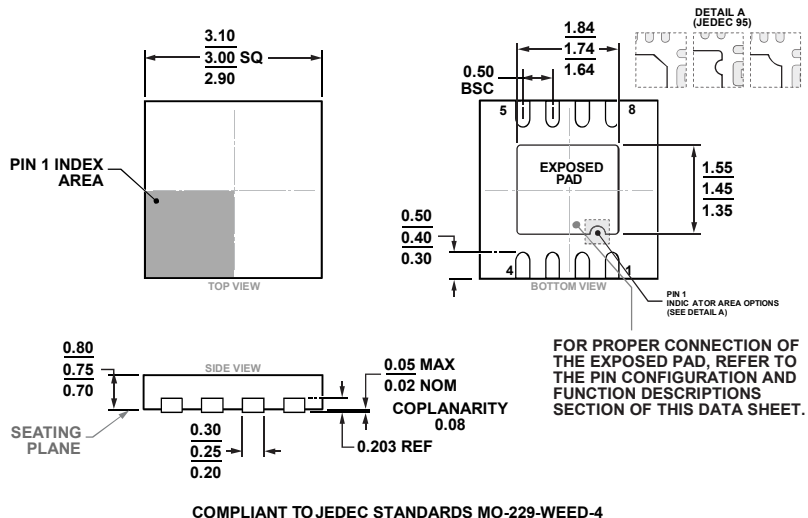
Figure 24. ADG901/ADG902 Evaluation Board Top View

03336-023

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA  
 Figure 25. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEED-4  
 Figure 26. 8-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-8-13)  
 Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADG901BRMZ	-40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1T
ADG901BRMZ-REEL7	-40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1T
ADG901BCPZ-500RL7	-40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	S1T
ADG902BRMZ	-40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1V
EVAL-ADG901EBZ		ADG901 Evaluation Board		
EVAL-ADG902EBZ		ADG902 Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

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