AT5520A

Bias Power Supply for TFT LCD Panels

Features

- **2.5V to 5.5V Input Supply Range**
- **Active-High Enable Control**
- **1.2MHz Current-Mode Boost Regulator**
  - **Fast Transient Response to Pulse Load**
  - **±1% Accurate Output Voltage**
  - **Built-In 20V/1.8A, 0.7Ω N-Channel MOSFET**
  - **High Efficiency up to 90%**
  - **Over-Current Protection**
  - **Output Under-Voltage Protection**
- **High-Performance Operational Amplifier**
  - **±150mA Output Short-Circuit Current**
  - **12V/μs Slew Rate**
  - **12MHz, -3dB Bandwidth**
  - **Rail-to-Rail Input and Output**
- **600kHz Negative Charge Pump Driver for V_{GL}**
- **600kHz Positive Charge Pump Driver for V_{GH}**
- **Power-On Sequence Control**
- **Thermal-Overload Protection**
- **TQFN3X3-16 Package**

Applications

- **Photo Frame**
- **GPS**
- **UMPC**

General Description

The AT5520A includes a high-performance boost regulator, a V_{COM} buffer (unity gain OPA), a V_{GH} charge pump driver, and a VGL charge pump driver for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The boost converter provides the regulated supply voltage for the panel source driver ICs. The converter is a high switching frequency (1.2MHz) current mode regulator with an integrated 20V N-Channel 0.7Ω MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loading while achieving efficiency over 90%. The device can produce output voltage as high as 18V from an input as low as 2.8V.

The V_{COM} buffer can drive the LCD V_{COM} voltage that features high short-circuit current (150mA), fast slew rate (12V/μs), wide bandwidth (12MHz) and rail-to-rail input/output.

A positive and a negative charge-pump driver provide adjustable regulated output voltages V_{GH} and V_{GL} to bias the TFT. Both the charge-pump driver operate with 600kHz switching frequency.

The AT5520A includes internal power-up sequencing, over/under voltage protections of the boost converter, and over temperature protection to ensure in safe operating.

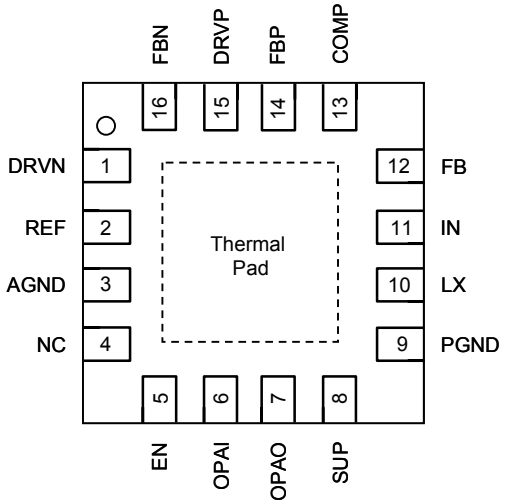
The AT5520A are available in a 16-pin 3X3 TQFN packages.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
AT5520AR41U	5520A	-40°C to +85°C	TQFN3X3-16

Note: R4:TQFN3X3-16
1: Bonding Code
U: Tape & Reel

Pin Configuration



AT5520A TQFN3X3-16

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Rating

IN to GND . . . . . -0.3V to 7V
LX to GND . . . . . .-0.3V to 20V
PGND to GND . . . . . -0.3V to +0.3V
SUP to GND . . . . . .-0.3V to 18V
OPAO, OPAI, DRVP, DRVN to GND
. . . . . .-0.3V to (SUP + 0.3V)
EN, REF, FB, FBP, FBN, COMP, FREQ to GND
. . . . . .-0.3V to (V_{IN} + 0.3V)
Thermal Resistance Junction to Ambient, (θ_{JA})*
TQFN3X3-16 . . . . . .103°C/W

Continuous Power Dissipation (T_A = +25°C)*
TQFN3X3-16 . . . . . .1.21W
Operating Temperature . . . . . .-40°C to 85°C
Junction Temperature . . . . . .+150°C
Storage Temperature . . . . . -65°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
Electrostatic Discharge, VESD
Human Body Mode (HBM) 2000V
Machine Mode (MM) 200V

* Please refer to "EV Board PCB Layout Section".
Stress beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device.

Electrical Characteristics

V_{IN} =3.3V, V_{AVDD}=8.5V, T_A =25°C.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

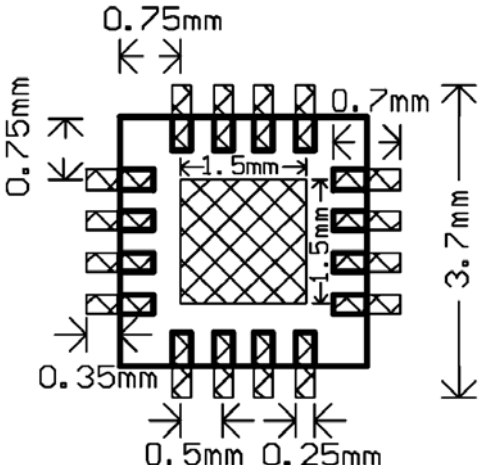
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Input Supply Voltage	V_{IN}		2.5	---	5.5	V
V_{IN} Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	1.8	2.0	2.2	V
		Hysteresis	---	0.1	---	
V_{IN} Quiescent Current	I_Q	V_{FB}=1.3V, LX no switching	---	0.3	0.6	mA
		V_{FB}=1.1V, LX switching	---	0.8	2	mA
V_{IN} Shut Down Current	I_{QSD}		---	---	1	μA
EN Threshold	V_{IH}		---	---	2	V
	V_{IL}		0.8	---	---	
Reference Voltage	V_{REF}		1.176	1.2	1.224	V
Thermal Shutdown Temperature	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	25	---	°C
Main Step-Up Regulator						
Operation Frequency	f_{OSC}		---	1200	---	kHz
Maximum Duty Cycle			85	90	---	%
Feedback Voltage	V_{FB}	No load	1.188	1.2	1.212	V
FB Input Bias Current		V_{FB}=1.5V	-40	---	+40	nA
Transconductance of Error Amplifier	Gm		---	70	---	μA/V
Voltage Gain of Error Amplifier	A_V		---	700	---	V/V
Feedback Voltage Line Regulation		V_{IN}=2.5 to 5.5V	---	0.15	0.25	%/V
LX ON-Resistance	$R_{LX(ON)}$		---	0.7	1	Ω
Current Sense Transconductance			---	4	---	A/V
Current Limit	I_{LIM}		---	1.8	---	A
N-MOSFET Leakage Current		V_{LX}=20V	---	0.1	10	μA

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
VCOM Buffer							
Supply Voltage Range	V_{SUP}			AVDD	---	16	V
Supply Current	I_{OP}			---	0.6	1.2	mA
Input Offset Voltage	V_{OS}	V_{OPAO}= AVDD/2, T_A = 25°C		-15	0	15	mV
Input Bias Current	I_{BIAS}			-100	---	100	nA
Output Voltage Swing High	V_{OH}	I_{OUT} = 100µA		AVDD-20	AVDD-5	---	mV
		I_{OUT} = 5mA		AVDD-0.2	AVDD-0.15	---	V
Output Voltage Swing Low	V_{OL}	I_{OUT} = -100µA		---	5	20	mV
		I_{OUT} = -5mA		---	150	200	mV
Short-Circuit Current		to AVDD/2	Source	100	150	---	mA
			Sink	100	150	---	
-3dB Bandwidth	F_{3dB}			---	12	---	MHz
Gain Bandwidth Product	GBW			---	8	---	MHz
Slew Rate	SR			8	12	---	V/µs
Gate-High Regulator							
Feedback Reference Voltage	V_{FBP}	No load		1.176	1.2	1.224	V
DRVP Switch On-Resistance	R_{ON_P}	V_{SUP}=10V,I_{DRVP}=20mA		---	50	---	Ω
	R_{ON_N}			---	20	---	
Switching Frequency	f_{SW}			---	600	---	kHz
Gate-Low Regulator							
Feedback Reference Voltage	V_{FBN}	No load		0.21	0.24	0.27	V
DRVN Switch On-Resistance	R_{ON_P}	V_{SUP}=10V,I_{DRVN}=20mA		---	30	---	Ω
	R_{ON_N}			---	50	---	
Switching Frequency	f_{SW}			---	600	---	kHz
Fault Detector							
FB Fault Trip Level		V_{FB} Falling		---	0.95	---	V
FBN Fault Trip Level		V_{FBN} Rising		---	0.42	---	V
FBP Fault Trip Level		V_{FBP} Falling		---	0.95	---	V
Fault Delay (UVP Delay)				---	100	---	ms

Minimum Footprint PCB Layout Section

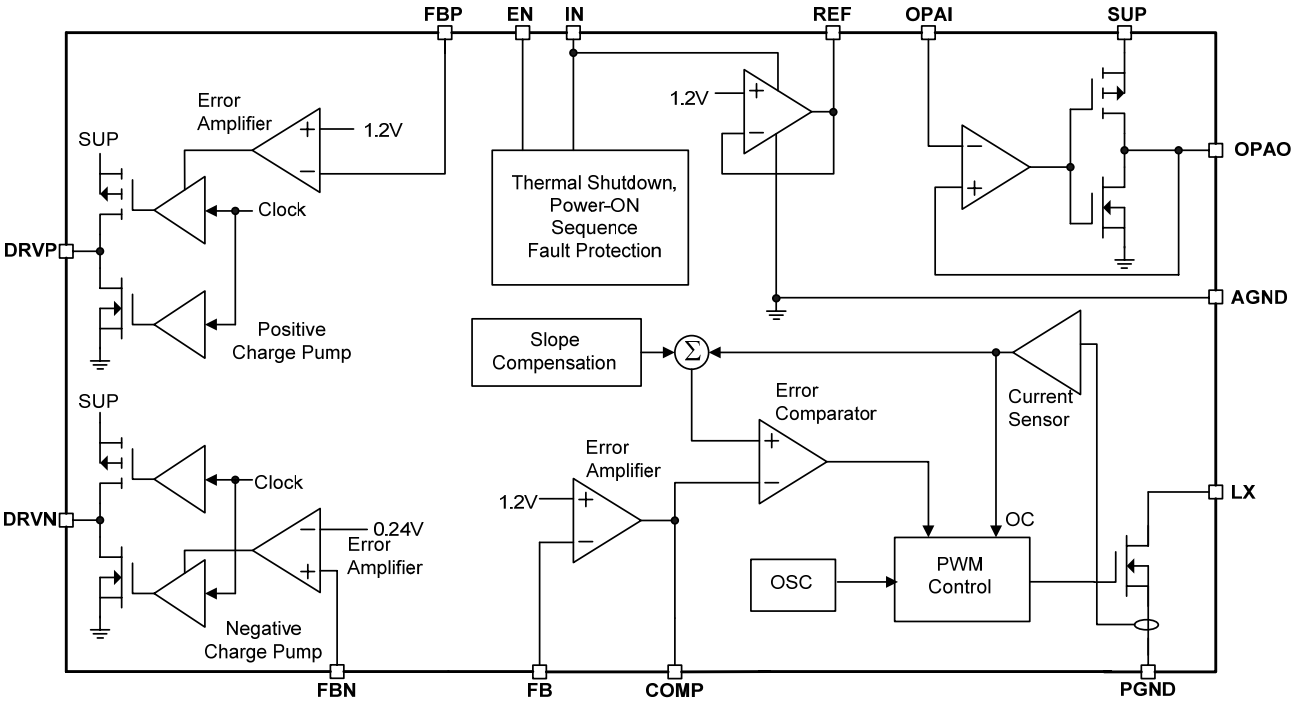
TQFN3X3-16



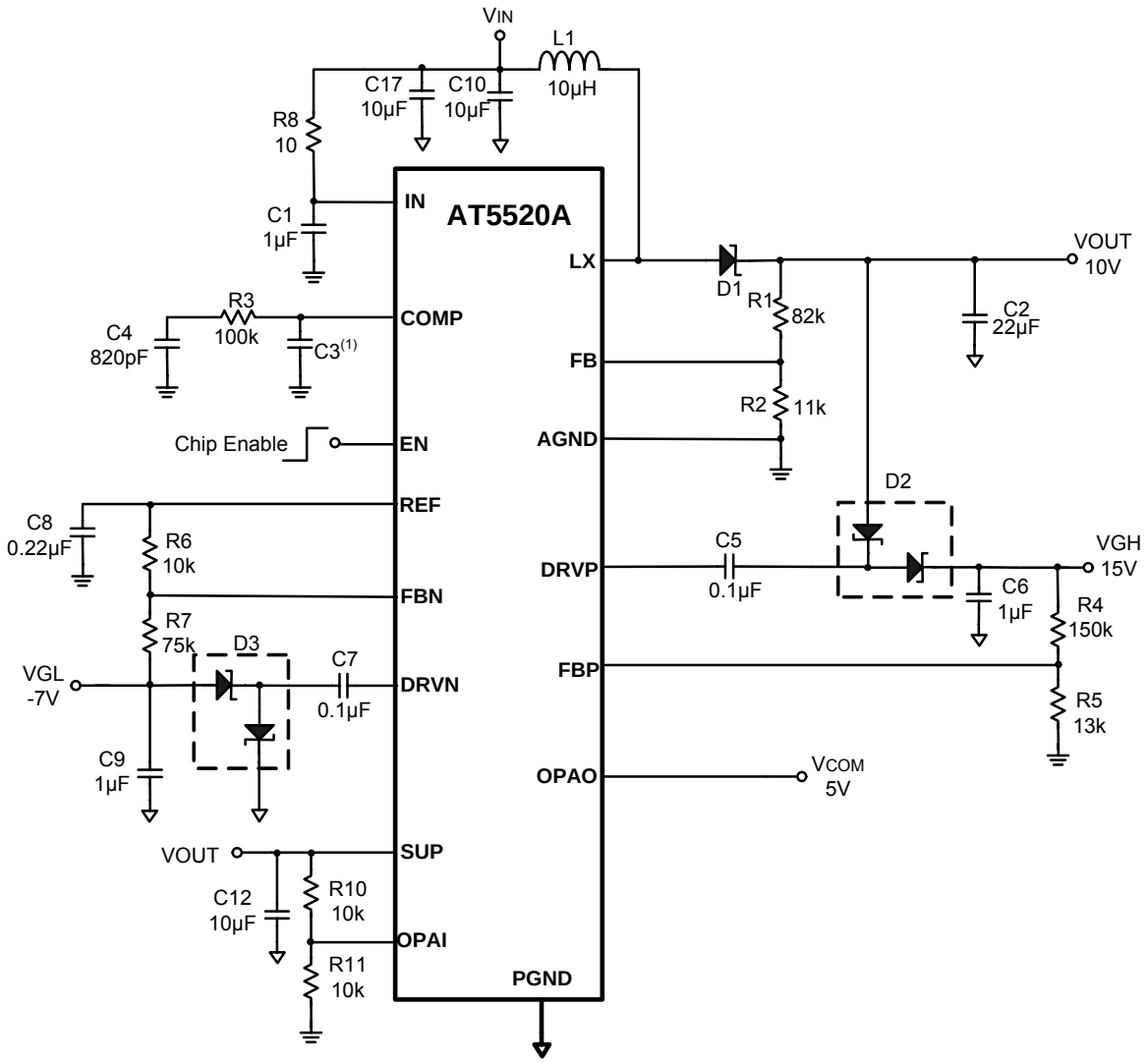
Pin Description

PIN	NAME	FUNCTION
1	DRVN	Driver output pin of the negative charge pump.
2	REF	Reference bypass terminal. Bypass REF to AGND with a minimum of 0.22μF close to this pin.
3	AGND	Analog Ground
4	NC	No Connection
5	EN	Active-High Enable Control Input
6	OPAI	VCOM buffer input pin. If OP function is not used, connect this pin to AGND.
7	OPAO	VCOM buffer output pin. If OP function is not used, make sure this pin floating.
8	SUP	VCOM buffer, VGH, and VGL charge pump power input. Positive supply rail for the operational amplifiers.
9	PGND	Power Ground.
10	LX	Switching pin. Drain of the internal power NMOS for the main step-up regulator
11	IN	Supply Input.
12	FB	Main Boost Regulator Feedback Input. FB regulates to 1.2V nominal. Connect FB to the center of a resistive voltage-divider between the main output and the analog ground (AGND). Place the resistive voltage-divider close to the pin.
13	COMP	Compensation error amplifier pin.
14	FBP	Feedback pin of positive charge pump. Regulates to 1.2V nominal.
15	DRVP	Driver output pin of the positive charge pump.
16	FBN	Feedback pin of negative charge pump. Regulates to 0.24V nominal.
Thermal Pad		Exposed pad should be soldered to PCB board and connected to AGND

Block Diagram



Typical Application Circuits



Note(1):C3 is an optional captacitor which avoids the noise disturbance

Application Information

The AT5520A contains a high performance current mode boost regulator, a gate-on charge pump driver and a gate-off charge pump driver. It also includes of a high- current rail-to rail operation amplifier. The following content contains the detailed description and the information of the component selection.

Boost Regulator

The boost regulator is a high efficiency current-mode PWM architecture with 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. To regulate the output voltage is to set resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal that combined with the current-sense signal will be compared with the COMP voltage to determine the current trip point and duty cycle.

Inductor Selection

A 4.7μH or 10μH inductor is recommended for small ripple applications. Small form factor and high efficiency are the major concerns for most AT5520A applications. Inductor with low core losses and small DCR (cooper wire resistance) are good choice for AT5520A applications.

Capacitor Selection

The small size of ceramic capacitors makes them suitable for AT5520A applications. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U.

Diode Selection

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for AT5520A applications. The forward voltage drop of a Schottky diode represents the conduction losses in the diode, while the diode capacitance (CT or CD) represents the switching losses. For diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes with higher current ratings usually have lower forward voltage drop and larger diode capacitance, which can cause significant switching losses of the AT5520A. A Schottky diode rated at 2A is sufficient for most AT5520A applications.

Output Voltage

The regulated output voltage is calculated by the following formula:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R1}{R2}\right)$$

The recommended value for R2 should be up to 100kΩ without some sacrificing. Place the resistor-divider as close as possible to the chip can reduce noise sensitivity.

Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of R3, C4 as Typical Application Circuit. Choose R3 to set high frequency integrator gain for fast transient response and C4 to set the integrator zero to maintain loop stability. For typical application V_{IN}=3.3V, V_{OUT}=8.5V, C_{OUT}=22μF × 2, L=10μH, the recommended value for compensation is as below:

R3=100kΩ, C4=820pF.

Over Current Protection

The AT5520A main boost converter has the function of peak current protection to limit peak inductor current. It prevents large current damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current condition occurs. Actual current limit is always larger than the nominal value because of the internal circuit delay.

Over Temperature Protection

The AT5520A main boost converter has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 150°C, it will shut down the device. Once the device cools down by approximately 25°C, it will start to operate normally.

FB under voltage Protection

If the AT5520A boost regulator feed-back voltage is under 0.1V, the internal NMOS switch turns off immediately. And the AT5520A restarts up until FB voltage is higher than 0.1V.

Fault protection

During steady-state operation, if the output of the boost converter or any of the charge pump outputs does not exceed its respective fault-detection threshold, the AT5520A activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (100ms typ), the AT5520A sets the fault latch to shut down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) or EN pin toggled to clear the fault latch and reactivate the device.

Voltage Reference

The voltage at REF pin is nominally 1.2V, which can deliver up to 100μA with good regulation. Connect a 0.22μF bypass capacitor between REF and AGND.

Positive Charge Pump

Typical Application Circuit shows an extract of the positive charge-pump driver circuit. During the first half-cycle, the NMOS turns on and charges C5 to the V_{OUT} voltage. During the second half-cycle, the NMOS turns off and the PMOS turns on to charge the DRVP pin up to the SUP voltage. The current of PMOS is controlled by error amplifier to regulate the output voltage V_{GH}. At this cycle, C5 is connected in parallel with C6 and pumps the maximum output voltage to (V_{SUP}+V_{OUT}).

The VGH voltage is set by

$$V_{GH} = 1.2V \times \left(1 + \frac{R4}{R5}\right)$$

Negative Charge Pump

During the first half-cycle, the PMOS turns on and charges C7 to the SUP voltage. During the second half-cycle, the PMOS turns off and the NMOS turns on to discharge the DRVN pin to the ground. The current of NMOS is controlled by error amplifier to regulate the output voltage V_{GL}. At this cycle, C7 is connected in parallel with C9 and pumps the maximum negative output voltage to -SUP.
The V_{GL} is set by

$$V_{GL} = 0.24V \times \left(1 + \frac{R7}{R6}\right) - 1.2V \times \left(\frac{R7}{R6}\right)$$

Operational Amplifier

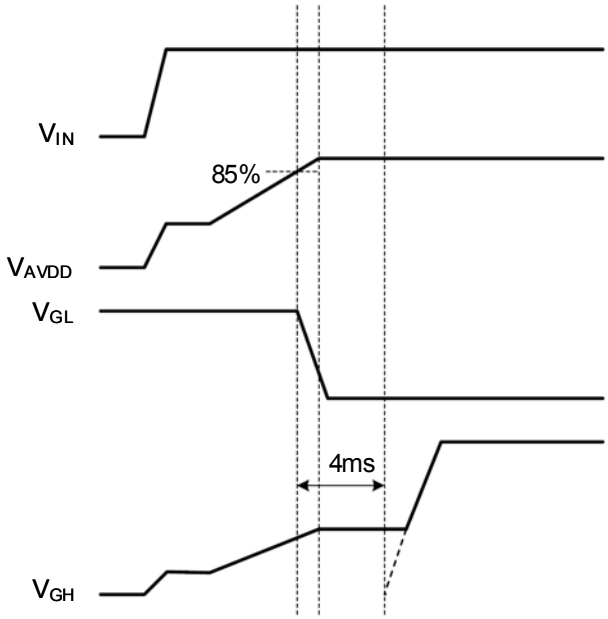
The function of the operational amplifier is to drive the LCD backplane V_{COM}. The operational amplifier features ±150mA output short circuit current, 12V/μs slew rate, and 12MHz bandwidth.

Power-Up Sequence

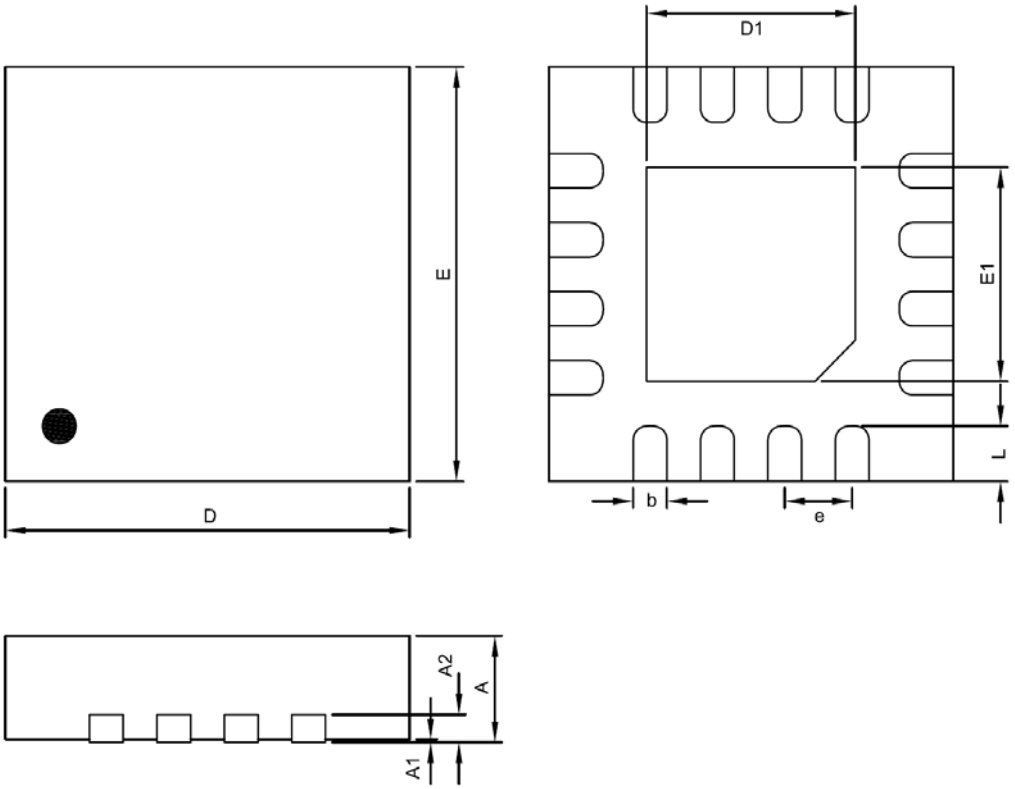
The AT5520A employs soft-start circuitry to reduce supply inrush current during start up conditions. When the device exits under-voltage lockout, the soft-start circuitry will slowly ramp up the output voltage.

Once the voltage on IN exceeds approximately 2V, the reference turns on. With a 0.22μF REF bypass capacitor, the reference reaches its regulation voltage of 1.2V. When the reference voltage exceeds 0.8V, the ICs enable the boost regulator. Once the FB voltage is above 1V, the gate-off charge pump driver is enabled immediately, and gate-on charge pump driver starts up after 4ms (TYP) delay time.

Timing Diagram



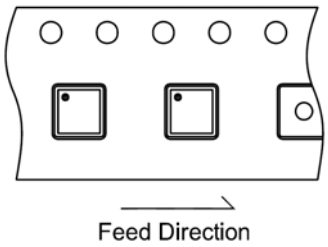
Package Information



TQFN3X3-16 Package

Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	1.50	1.60	1.75	0.0591	0.0630	0.0689
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'Y/REEL
TQFN3X3-16	3,000 ea