General Description

The DS28E07 is a 1024-bit, 1-Wire® EEPROM chip organized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four user memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. Each device has its own guaranteed unique 64-bit ROM identification number (ROM ID) that is factory programmed into the chip. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multiple-device 1-Wire network.

Applications

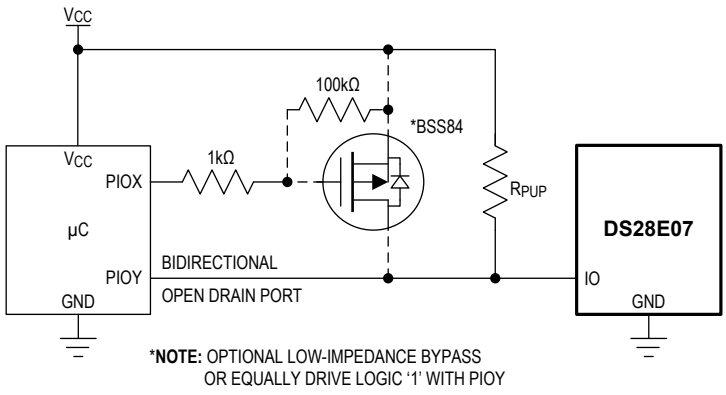
- Accessory/PCB Identification
- Medical Sensor Calibration Data Storage
- Analog Sensor Calibration Including IEEE P1451.4 Smart Sensors
- Ink and Toner Print Cartridge Identification
- After-Market Management of Consumables

Benefits and Features

- Partitioning of Memory Provides Greater Flexibility in Programming User Data
  - 1024 Bits of EEPROM Memory Organized as Four Pages of 256 Bits
  - Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (Write to 0)
- Advanced 1-Wire Protocol Minimizes Interface to Just Single IO Reducing Required Pin Count and Enhancing Reliability
  - Unique Factory-Programmed, Unalterable 64-Bit Identification Number
  - Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise
  - Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps Using 1-Wire Protocol
  - Reads and Writes over a Wide Voltage Range from 3.0V to 5.25V from -40°C to +85°C
  - ±8kV HBM ESD Protection (typ) for IO Pin

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



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Absolute Maximum Ratings

IO Voltage Range to GND .....-0.5V to +6V
IO Sink Current.....±10mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Lead Temperature (reflow) TO-92 .....+250°C
Lead Temperature (reflow) TDFN, TSOC.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSOC
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....127°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....37°C/W
TO-92
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....132°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....4°C/W
TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....55°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 3)	3.0		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Note 3, 4)	300		2200	Ω
Input Capacitance	C_{IO}	(Notes 4, 5)		1000		pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05	1.75	6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 6, 7, 8)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(Notes 3, 9)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 6, 7, 10)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(Notes 6, 7, 11)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 10mA, 4.75V ≤ V_{PUP} ≤ 5.25V			0.5	
Recovery Time (Notes 3, 13)	t_{REC}	Standard speed, R_{PUP} = 2200Ω	5			µs
		Overdrive speed, R_{PUP} = 2200Ω	3			
		Overdrive speed, directly prior to reset pulse, R_{PUP} = 2200Ω	5			
Rising-Edge Hold-off Time (Notes 6, 14)	t_{REH}	Standard speed		1.3		µs
		Overdrive speed		N/A (0)		
Time Slot Duration (Notes 3, 15)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	9			

Electrical Characteristics (continued)

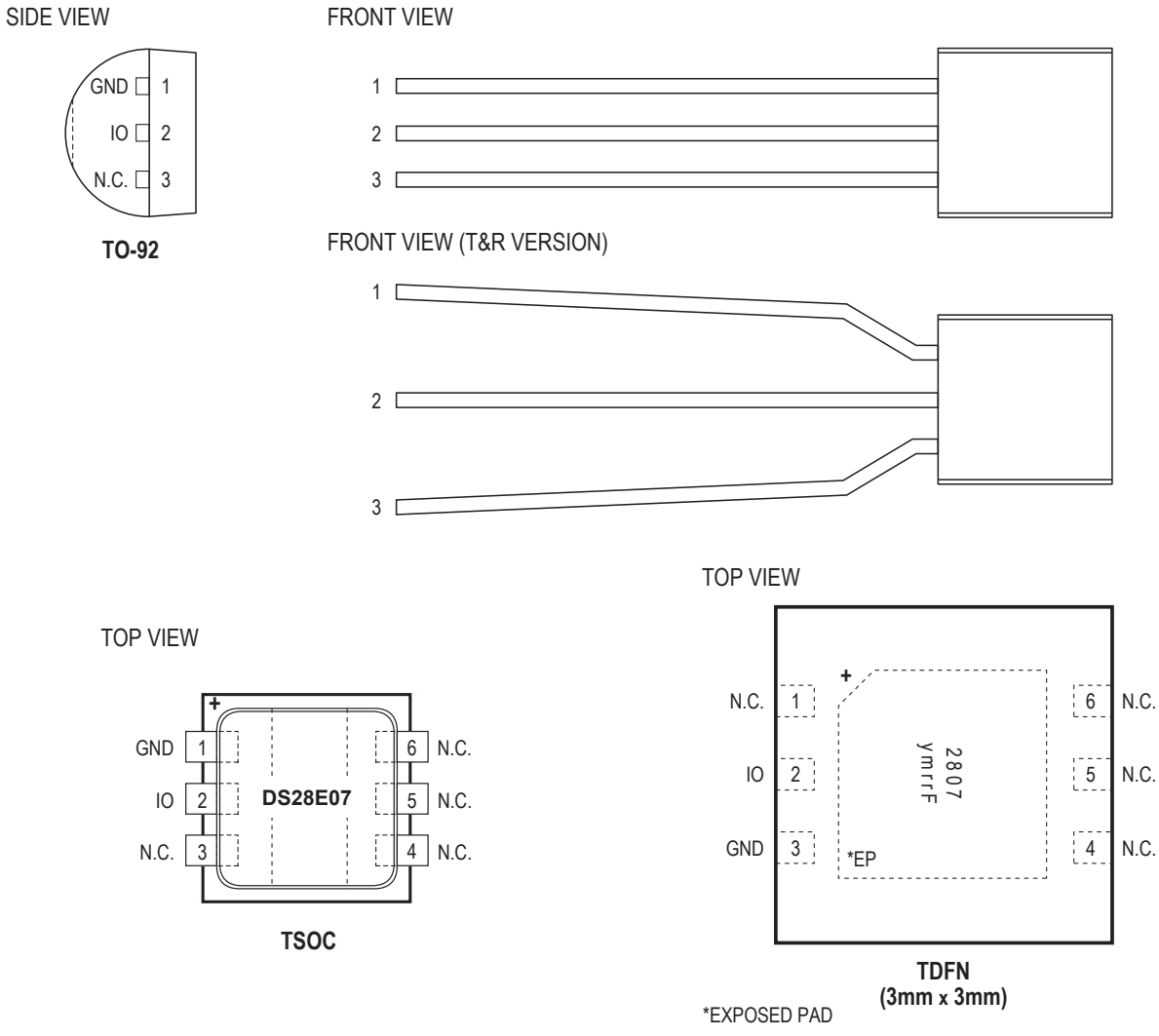
(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire RESET, PRESENSE-DETECT CYCLE						
Reset Low Time (Note 3)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 3, 16)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 3, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		15.5	
Write-One Low Time (Notes 3, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	0.25		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 3, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	0.25		2 - δ	
Read Sample Time (Notes 3, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
EEPROM						
Programming Current	I_{PROG}	(Notes 6, 19)			1.2	mA
Programming Time	t_{PROG}	(Note 20)			12	ms
Write/Erase Cycles (Endurance)	N_{CY}	T_A = +85°C (Notes 21, 22)	1000			—
Data Retention	t_{DR}	T_A = +85°C (Notes 23, 24, 25)	10			Years

Note 2: Limits are 100% production tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.
Note 3: System requirement.
Note 4: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.
Note 5: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 6: Guaranteed by design and/or characterization only. Not production tested.
Note 7: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 8: Voltage below which, during a falling edge on IO, a logic-zero is detected.
Note 9: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.
Note 10: Voltage above which, during a rising edge on IO, a logic-one is detected.
Note 11: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.

Note 13: Applies to a single device attached to a 1-Wire line.
Note 14: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.
Note 15: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 16: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E07 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.
Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.
Note 19: Current drawn from IO during the EEPROM programming interval. The pullup circuit on IO during the programming interval should be such that the voltage at IO is greater than or equal to V_{PUPMIN}. If V_{PUP} in the system is close to V_{PUPMIN}, a low impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.
Note 20: Interval begins t_{REHMAX} after the trailing rising edge on IO for the last time slot of the E/S byte for a valid Copy Scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.
Note 21: Write-cycle endurance is tested in compliance with JESD47G.
Note 22: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 23: Data retention is tested in compliance with JESD47G.
Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
Note 25: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended.

Pin Configurations



Pin Description

PIN			NAME	FUNCTION
TSOC	TO-92	TDFN-EP		
3, 4, 5, 6	3	1, 4, 5, 6	N.C.	Not Connected
2	2	2	IO	1-Wire Bus Interface. Open-drain signal requires an external pullup resistor.
1	1	3	GND	Ground
—	—	—	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS28E07 combines 1024 bits of user EEPROM, 64 bits of administrative data memory, and a 64-bit ROM ID in a single chip. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return. The DS28E07 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory or the administrative data memory. Data is first written to the scratchpad from which it can be read back. After the data has been verified, a Copy Scratchpad command transfers the data to its final memory location. The user memory can have unrestricted write access (factory default), or can be write protected or put in EPROM emulation mode. Write protection prevents changes to the memory data. EPROM emulation mode logically ANDs memory data with incoming new data, which allows changing bits from 1 to 0, but not vice versa. By changing one bit at a time this mode could be used to create nonvolatile nonresettable counters. For more details, refer to Application Note 5042: *Implementing Nonvolatile*, *Nonresettable Counters for Embedded Systems*. The device's 64-bit ROM ID electronically identifies the equipment in which the DS28E07 is used. The ROM ID guarantees unique identification and is also used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other. DS28E07 applications include accessory/PCB identification, medical sensor calibration data storage, analog sensor calibration including IEEE P1451.4 smart sensors, ink and toner print cartridge identification, and after-market management of consumables.

Overview

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS28E07. The DS28E07 has four main data components: four 32-byte pages of user EEPROM, a 64-bit scratchpad, 64 bit of administrative data memory, and a 64-bit ROM ID.

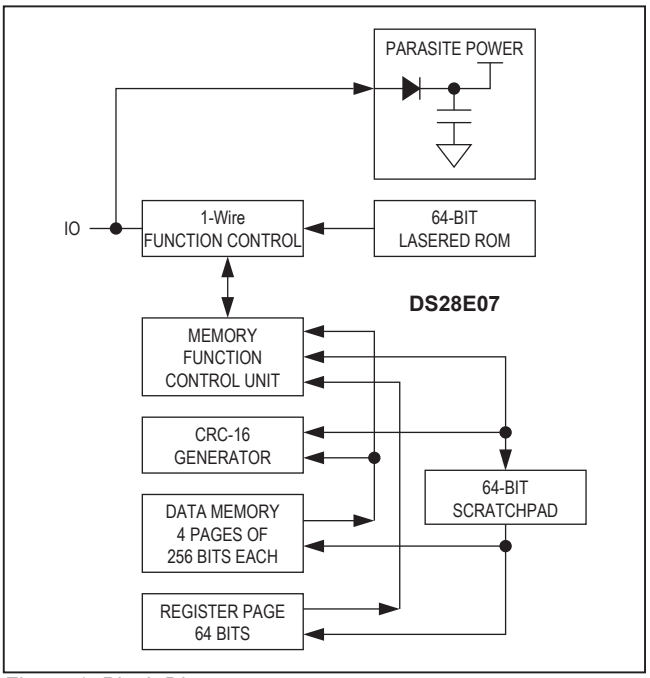


Figure 1. Block Diagram

Figure 2 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive-Skip ROM or Overdrive-Match ROM command byte executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 9. After a ROM function command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 7. **All data is read and written least significant bit first**.

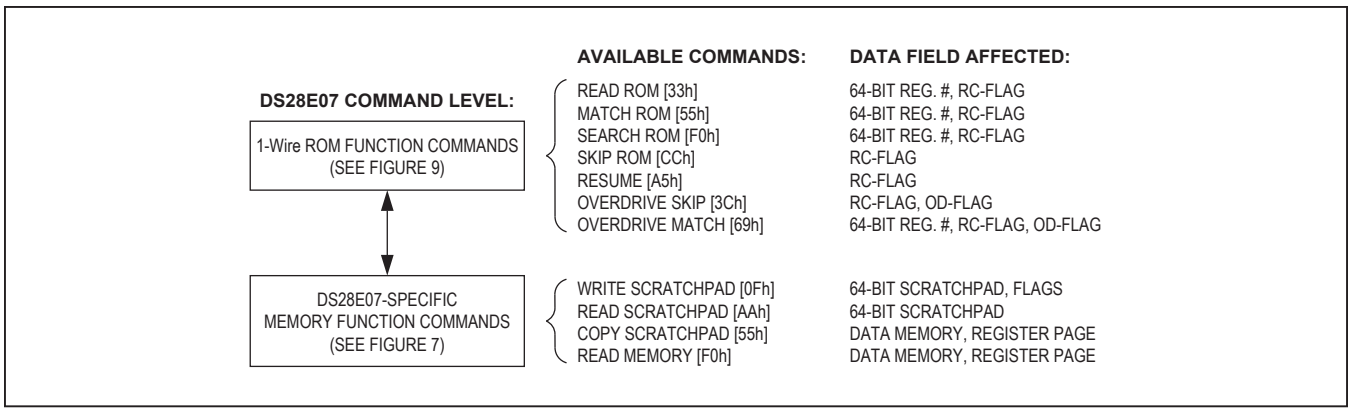


Figure 2. Hierarchical Structure for 1-Wire Protocol

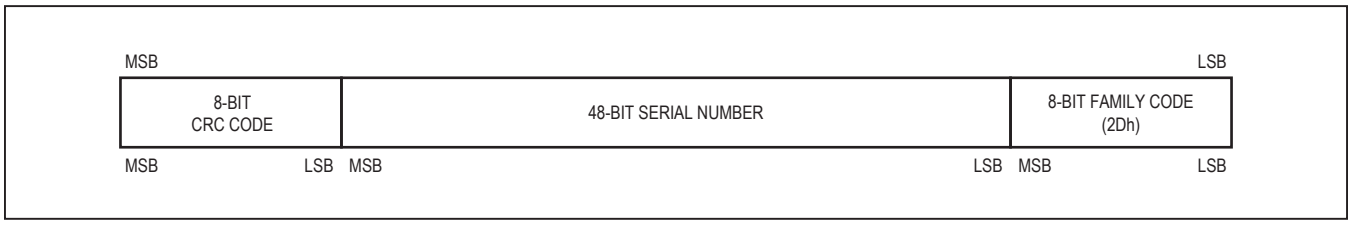


Figure 3. 64-Bit ROM ID

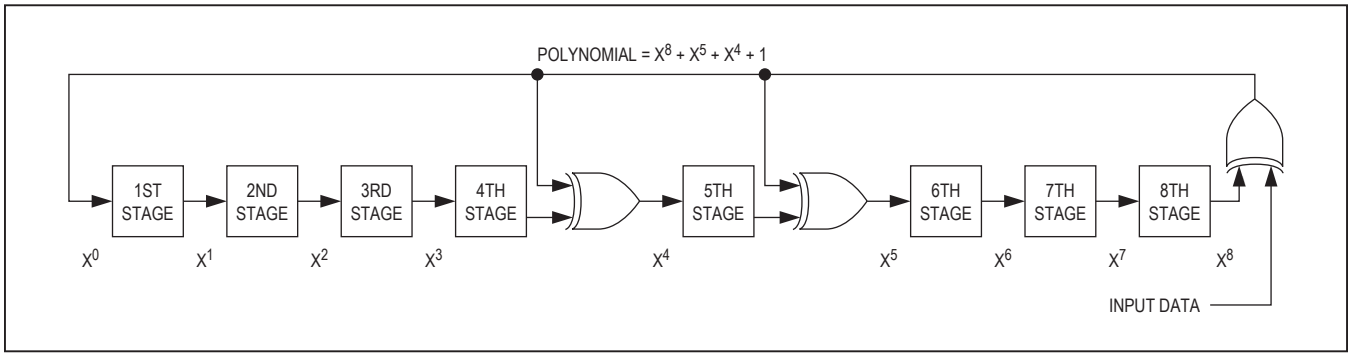


Figure 4. 1-Wire CRC Generator

64-Bit ROM ID

Each DS28E07 contains a unique ROM ID that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products.*

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

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Memory Resources

The memory of the DS28E07 consists of user memory, administrative data, scratchpad, and a ROM ID. Table 1 shows the size, access mode, and purpose of the various memory areas. Brackets around an access mode indicate possible restrictions, such as write protection or read protection. User memory and administrative data are located in a linear address space, as shown in Figure 5. The user memory and the administrative data have unrestricted read access. Each user memory page can be individually set to open (unprotected), write protected, or EPROM mode by setting the associated protection byte in the administrative data. As a factory default, the entire user memory is unprotected and its contents are undefined. The administrative data consists of 4 protection control bytes, a copy-protection byte, the factory byte, and 2 user byte/manufacture ID bytes. The manufacturer ID can be a customer-supplied identification code that assists the application software in identifying the product the DS28E07 is associated with. Contact the factory to set up and register a custom manufacturer ID. Any data read from addresses 0088 to 00FEh is undefined. Address 00FFh provides read access to a byte that tells the chip revision in hexadecimal notation, e.g., A1h.

Table 1. Memory Resources

NAME	SIZE(BYTES)	ACCESS MODE	PURPOSE
User memory (EEPROM)	128	Read, (write)	Application-specific data storage
Administrative data	8	Read, (write), Internal read	Page protection settings, factory bytes, user bytes/manufacturer ID
Scratchpad	8	Read, write, internal read	Intermediate data storage
ROM ID	8	Read, internal read	1-Wire network device address

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 001Fh	R/(W)	User memory Page 0	
0020h to 003Fh	R/(W)	User memory Page 1	
0040h to 005Fh	R/(W)	User memory Page 2	
0060h to 007Fh	R/(W)	User memory Page 3	
0080h*	R/(W)	Protection Control Byte Page 0	55h: Write Protect P0; AAh: EPROM mode P0; 55h or AAh: Write Protect 80h
0081h*	R/(W)	Protection Control Byte Page 1	55h: Write Protect P1; AAh: EPROM mode P1; 55h or AAh: Write Protect 81h
0082h*	R/(W)	Protection Control Byte Page 2	55h: Write Protect P2; AAh: EPROM mode P2; 55h or AAh: Write Protect 82h
0083h*	R/(W)	Protection Control Byte Page 3	55h: Write Protect P3; AAh: EPROM mode P3; 55h or AAh: Write Protect 83h
0084h*	R/(W)	Copy Protection Byte	55h or AAh: Copy Protect 0080:008Fh, and any write-protected Pages
0085h	R	Factory byte. Set at Factory.	AAh:Write Protect 85h, 86h, 87h; 55h: Write Protect 85h, unprotect 86h, 87h
0086h	R/(W)	User Byte/Manufacturer ID	—
0087h	R/(W)	User Byte/Manufacturer ID	—
0088h to 00FEh	R	Reserved	—
00FFh	R	Chip Revision Code	—

**Once programmed to AAh or 55h this address becomes read-only. All other codes can be stored but will neither write protect the address nor activate any function.*

Figure 5. Memory Map

In addition to the main EEPROM array, an 8-byte volatile scratchpad is included. Writes to the EEPROM array are a two-step process. First, data is written to the scratchpad and then copied into the main array. This allows the user to first verify the data written to the scratchpad prior to copying into the main array. The device supports only 8-byte copy operations. For data in the scratchpad to be valid for a copy operation, the address supplied with a Write Scratchpad command must start on an 8-byte boundary, i.e., the three LS-bits of the address must be 000b, and 8 full bytes must be written into the scratchpad.

The protection control bytes determine how incoming data on a Write Scratchpad command is loaded into the scratchpad. A protection setting of 55h (write protect) causes the incoming data to be ignored and the target address main memory data to be loaded into the scratchpad. A protection setting of AAh (EPROM mode) causes the logical AND of incoming data and target address user memory data to be loaded into the scratchpad. Any other protection control byte setting leaves the associated user memory page open for unrestricted write access. Note: For the EPROM mode to function, the entire affected memory page must first be programmed to FFh. Protection-control byte settings of 55h or AAh also write protect the protection-control byte. The protection-control byte setting of 55h does not block the copy. This allows write-protected data to be refreshed (i.e., reprogrammed with the current data) in the device.

The copy-protection byte is used for a higher level of security and should only be used after all other protection control bytes, user bytes, and write-protected pages are set to their final value. If the copy-protection byte is set to 55h or AAh, all copy attempts to the administrative data are blocked. In addition, all copy attempts to write-protected user memory pages (i.e., refresh) are blocked.

Address Registers and Transfer Status

The DS28E07 employs three address registers: TA1, TA2, and E/S (Figure 6). These registers are common to many other 1-Wire devices, but operate slightly differently with the DS28E07. Registers TA1 and TA2 must be loaded with the target address to which the data is written or from which data is read. Register E/S is a read only transfer-status register used to verify data integrity with write commands. E/S bits E[2:0] are loaded with the incoming T[2:0] on a Write Scratchpad command and increment on each subsequent data byte. This is, in effect, a byte-ending offset counter within the 8-byte scratchpad. Bit 5 of the E/S register, called PF, is a logic 1 if the data in the scratchpad is not valid due to a loss of power or if the master sends fewer bytes than needed to reach the end of the scratchpad. For a valid write to the scratchpad, T[2:0] must be 0 and the master must have sent 8 data bytes. Bits 3, 4, and 6 have no function; they always read 0. The highest valued bit of the E/S register, called authorization accepted (AA), acts as a flag to indicate that the data stored in the scratchpad has already been copied to the target memory address. Writing data to the scratchpad clears this flag.

BIT #	7	6	5	4	3	2	1	0
TARGET ADDRESS (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
TARGET ADDRESS (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
ENDING ADDRESS WITH DATA STATUS (E/S) (READ ONLY)	AA	0	PF	0	0	E2	E1	E0

Figure 6. Address Registers

Writing with Verification

To write data to the DS28E07, the scratchpad must be used as intermediate storage. First, the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. Note that Copy Scratchpad commands must be performed on 8-byte boundaries, i.e., the three LSBs of the target address (T2, T1, T0) must be equal to 000b. If T[2:0] are sent with nonzero values, the copy function is blocked. Under certain conditions (see the Write Scratchpad [0Fh] section) the master receives an inverted CRC-16 of the command, address (actual address sent), and data at the end of the Write Scratchpad command sequence. Knowing this CRC value, the master can compare it to the value it has calculated to decide if the communication was successful and proceed to the Copy Scratchpad command. If the master could not receive the CRC-16, it should send the Read Scratchpad command to verify data integrity. As a preamble to the scratchpad data, the DS28E07 repeats the target address TA1 and TA2 and sends the contents of the E/S register. If the PF flag is set, data did not arrive correctly in the scratchpad, or there was a loss of power since data was last written to the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag together with a cleared PF flag indicates that the device did not recognize the Write command.

If everything went correctly, both flags are cleared. Now the master can continue reading and verifying every data byte. After the master has verified the data, it can send the Copy Scratchpad command, for example. This command must be followed exactly by the data of the three address registers, TA1, TA2, and E/S. The master should obtain the contents of these registers by reading the scratchpad. As well, a strong pullup (i.e., low impedance bypass) turns on after the Copy Scratchpad sequence for the duration of t_{PROG} to enhance power delivery. The strong pullup can comprise an external FET circuitry or by driving logic 1 on the PIO of a host system with a good low-impedance drive strength. If neither option is available then the designer can size R_{PUP} accordingly for proper power delivery as to not violate V_{PUP} minimum.

Memory Function Commands

Figure 7 describes the protocols necessary for accessing the memory of the DS28E07. An example on how to use these functions to write to and read from the device is in the *Memory Function Example* section. The communication between the master and the DS28E07 takes place either at standard speed (default, OD = 0) or at overdrive speed (OD = 1). If not explicitly set into overdrive mode, the DS28E07 assumes standard speed.

Write Scratchpad [0Fh]

The Write Scratchpad command applies to the user memory and the writable addresses of the administrative data. For the scratchpad data to be valid for copying to the array, the user must perform a Write Scratchpad command of 8 bytes starting at a valid row boundary. The Write Scratchpad command accepts invalid addresses and partial rows, but subsequent Copy Scratchpad commands are blocked.

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset of T[2:0]. The E/S bits E[2:0] are loaded with the starting byte offset and increment with each subsequent byte. Effectively, E[2:0] is the byte offset of the last full byte written to the scratchpad. Only full data bytes are accepted.

When executing the Write Scratchpad command, the CRC generator inside the DS28E07 (Figure 13) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte as sent by the master. This CRC is generated using the CRC-16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses (TA1 and TA2), and all the data bytes. Note that the CRC-16 calculation is performed with the actual TA1 and TA2 and data sent by the master. The master can end the Write Scratchpad command at any time. However, if the end of the scratchpad is reached (E[2:0] = 111b), the master can send 16 read time slots and receive the CRC generated by the DS28E07.

If a Write Scratchpad command is attempted to a write-protected location, the scratchpad is loaded with the data already existing in memory rather than the data transmitted. Similarly, if the target address page is in EPROM mode, the scratchpad is loaded with the bitwise logical AND of the transmitted data and data already existing in memory.

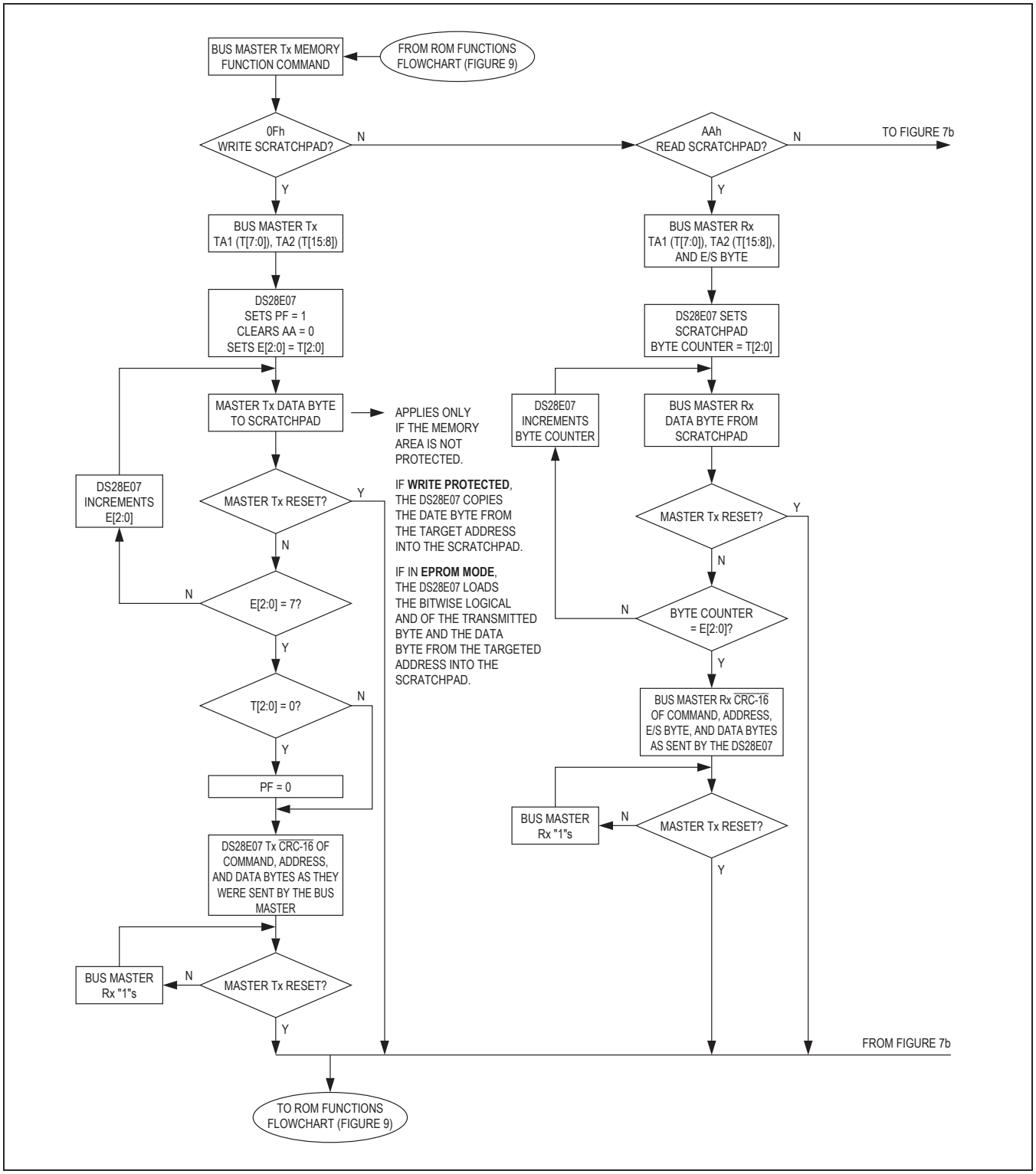

Figure 7a. Memory Function Flowchart

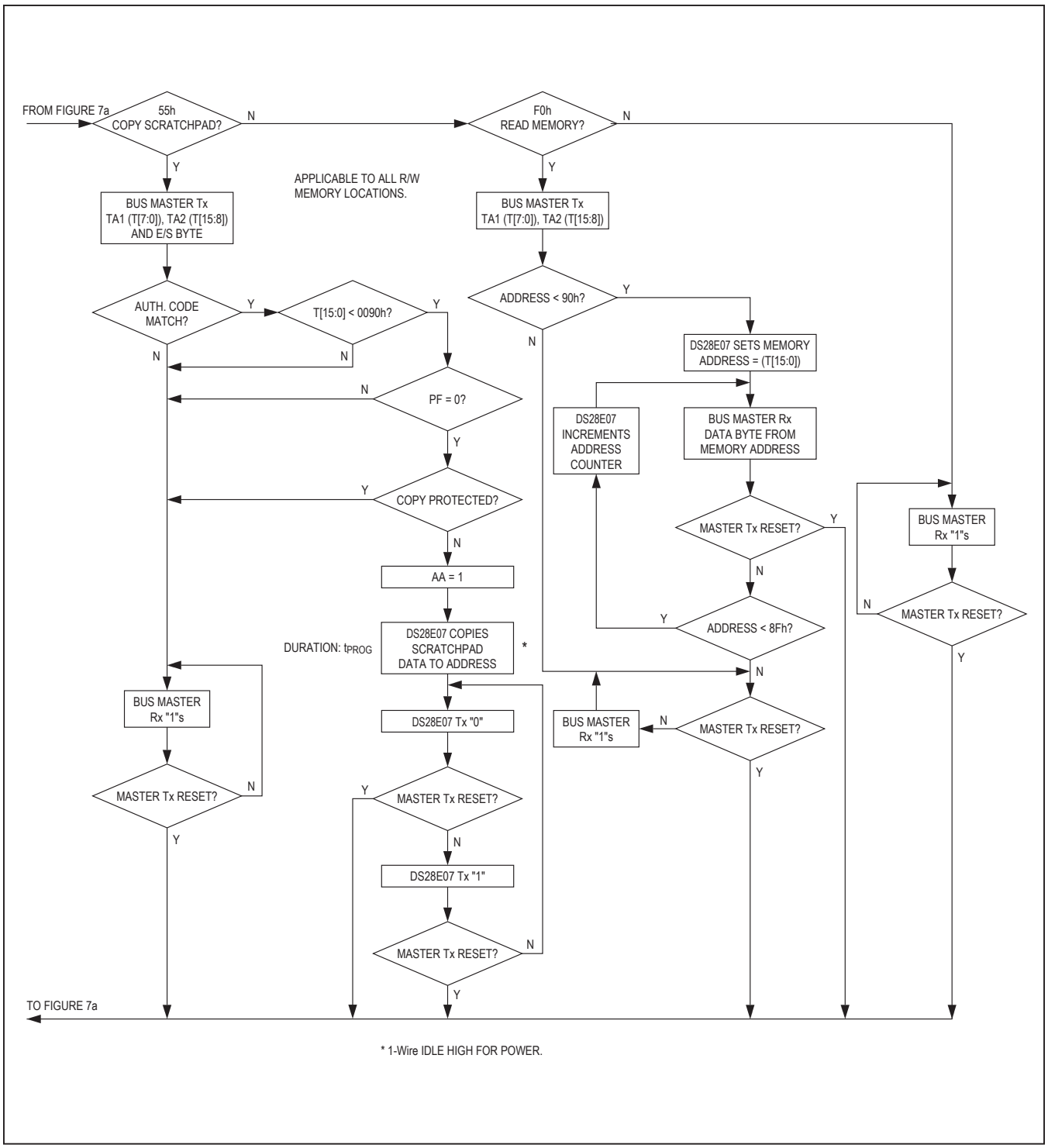

Figure 7b. Memory Function Flowchart (continued)

Read Scratchpad [AAh]

The Read Scratchpad command allows verifying the target address and the integrity of the scratchpad data. After issuing the command code, the master begins reading. The first two bytes are the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data, which may be different from what the master originally sent. This is of particular importance if the target address is within the administrative data section or a page in either write-protection mode or EPROM mode. See the Write Scratchpad [0Fh] section for details. The master should read through the scratchpad (E[2:0] - T[2:0] + 1 bytes), after which it receives the inverted CRC based on data as it was sent by the DS28E07. If the master continues reading after the CRC, all data is logic 1.

Copy Scratchpad [55h]

The Copy Scratchpad command is used to copy data from the scratchpad to writable memory sections. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which should have been obtained by an immediately preceding Read Scratchpad command. This 3-byte pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the target address is valid, the PF flag is not set, and the target memory is not copy protected, then the AA flag is set and the copy begins. All 8 bytes of scratchpad contents are copied to the target memory location. The duration of the device's internal data transfer is t_{PROG} during which the voltage on the 1-Wire bus must not fall below V_{PUP} minimum. Best practice is to generate a strong pullup that turns on after the Copy Scratchpad sequence for the duration of t_{PROG} to enhance power delivery. A pattern of alternating 0s and 1s are transmitted after the data has been copied until the master issues a reset pulse. If the PF flag is set or the target memory is copy protected, the copy does not begin and the AA flag is not set.

Read Memory [F0h]

The Read Memory command is the general function to read data from the DS28E07. After issuing the command, the master must provide the 2-byte target address. After these 2 bytes, the master reads data beginning from the target address and can continue until address 00FFh. If the master continues reading, the result is logic 1s. The device's internal TA1, TA2, E/S, and scratchpad contents are not affected by a Read Memory command.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS28E07 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E07 is open drain with an internal circuit equivalent to that shown in Figure 8.

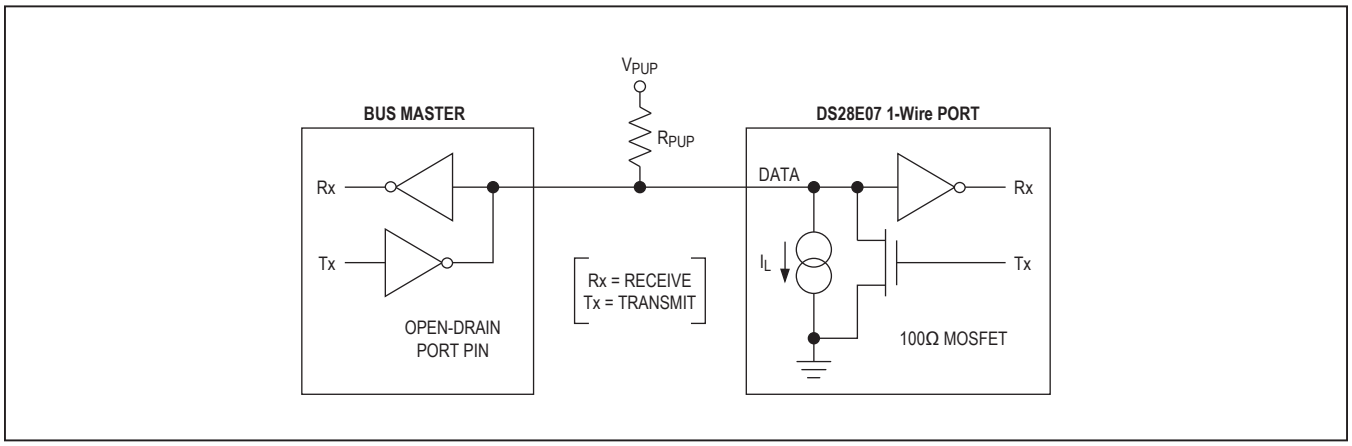

Figure 8. Hardware Configuration

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E07 supports both a standard and overdrive communication speed of 15.4kbps (max) and 125kbps (max), respectively. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E07 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 15.5µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E07 through the 1-Wire port is as follows:

- Initialization
- ROM function command
- Memory function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E07 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E07 supports. All ROM function commands are 8 bits long. A list of these commands follows. See Figure 9.

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E07's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E07 on a multidrop bus. Only the DS28E07 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit in the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

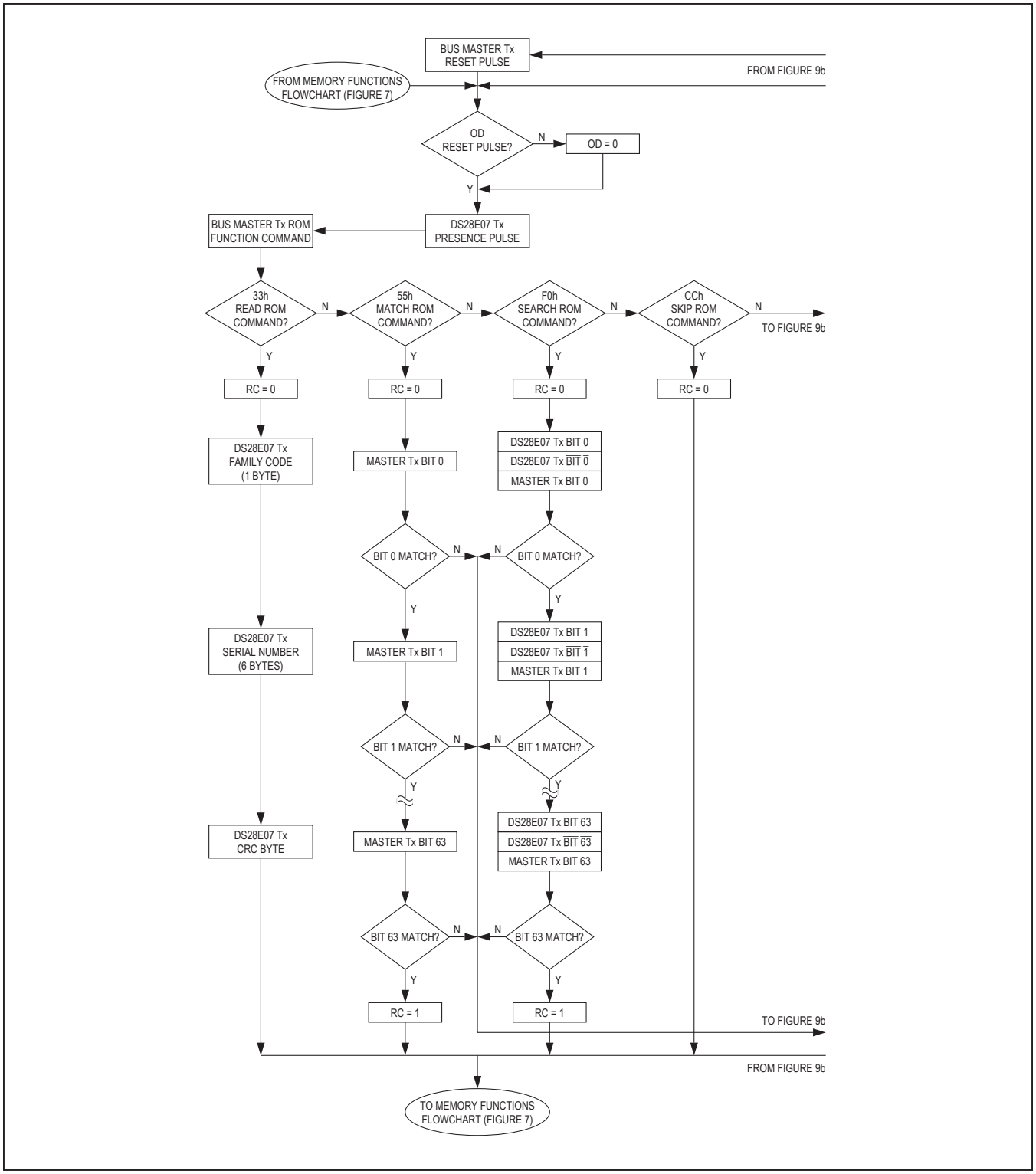

Figure 9a. ROM Functions Flow Chart

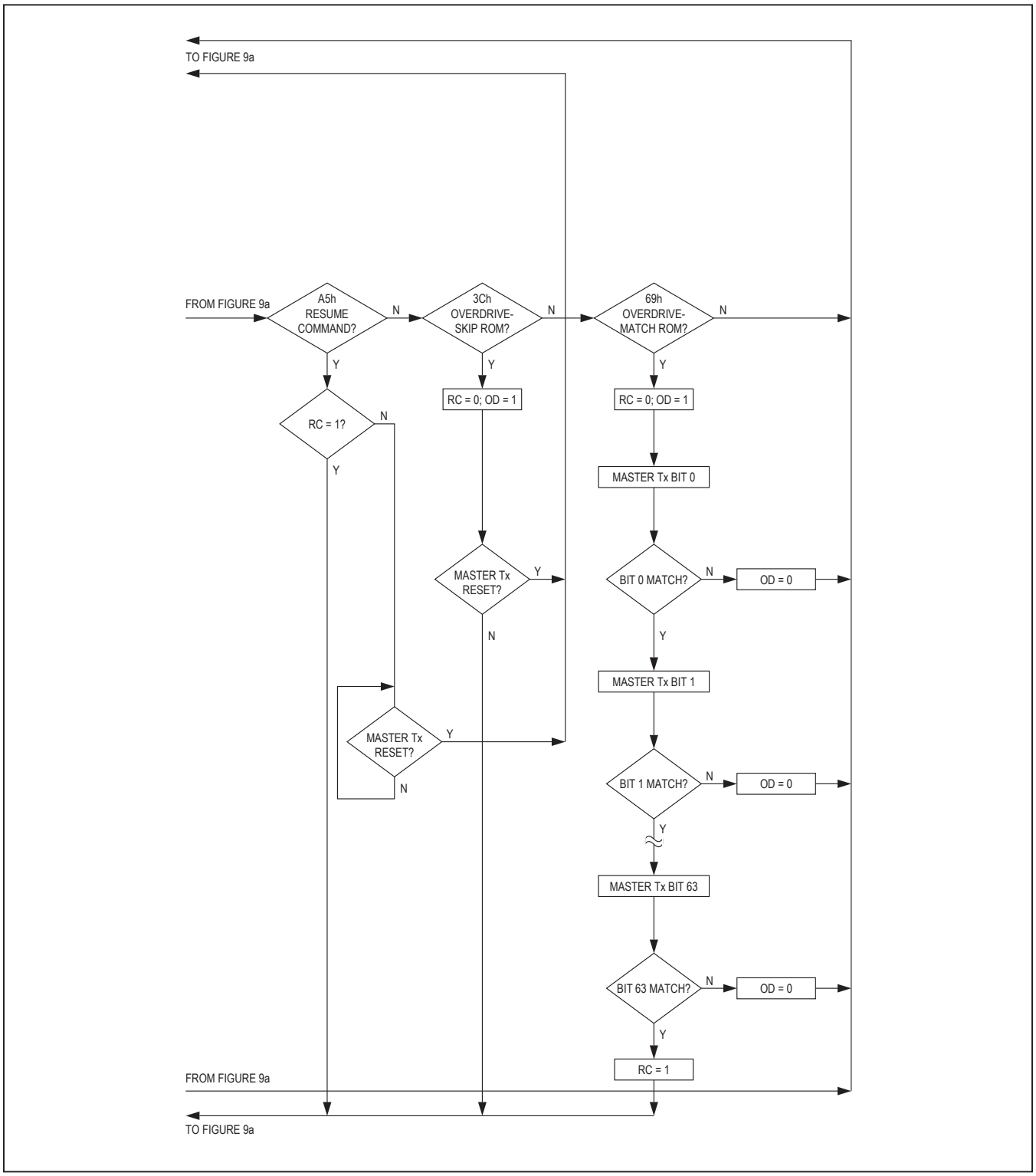

Figure 9b. ROM Functions Flow Chart (continued)

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the memory function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E07 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28E07 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E07 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

1-Wire Signaling

The DS28E07 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E07 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the overdrive mode, the DS28E07 communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 10 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E07 when determining a logical level, not triggering any events.

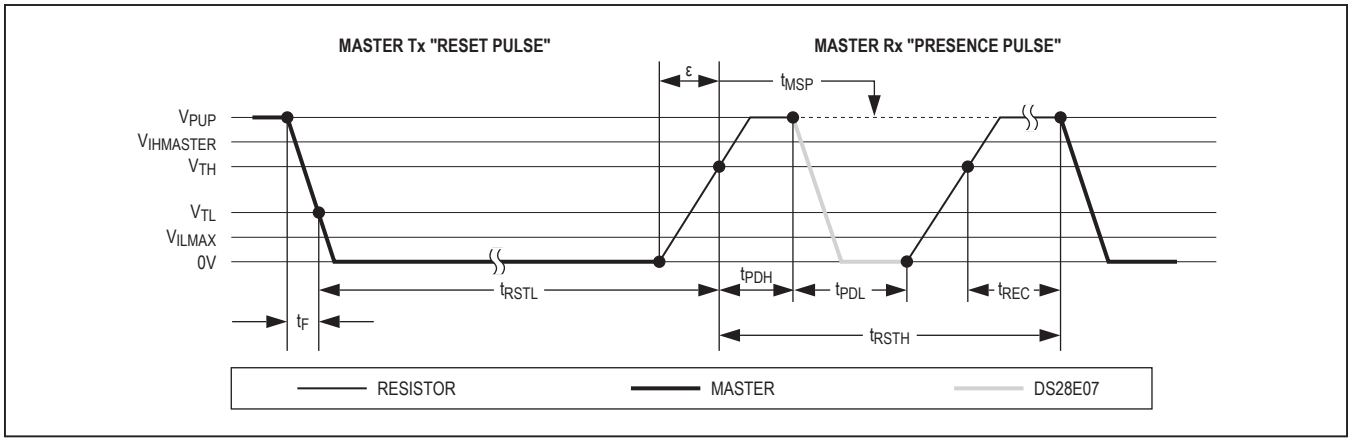

Figure 10. Initialization Procedure: Reset and Presence Pulse

Figure 10 shows the initialization sequence required to begin any communication with the DS28E07. A reset pulse followed by a presence pulse indicates that the DS28E07 is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS28E07 is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode. If the device is in overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. When the threshold V_{TH} is crossed, the DS28E07 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28E07 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS28E07 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 11 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E07 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E07 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E07 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E07 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of $t_{RL} + \delta$ (rise time) on one side and the internal timing generator of the DS28E07 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E07 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E07 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

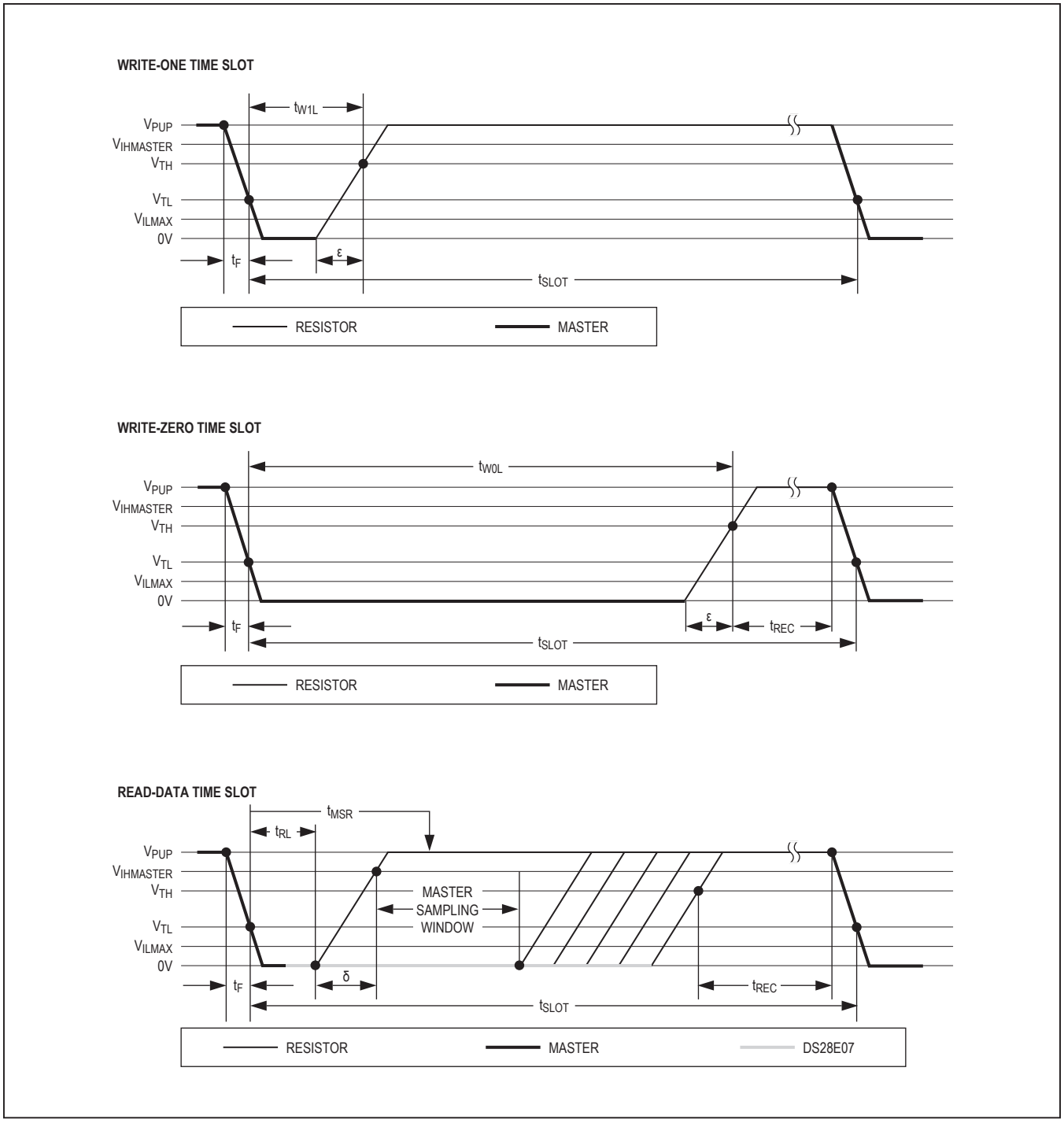

Figure 11. Read/Write Timing Diagrams

Improved Network Behavior (Switchpoint Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E07 uses a 1-Wire front-end that is less sensitive to noise.

The DS28E07's 1-Wire front-end has the following features:

1) There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
2) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but does not go below V_{TH} - V_{HY}, it is not recognized (Figure 12, Case A). The hysteresis is effective at any 1-Wire speed.
3) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below the V_{TH} - V_{HY} threshold (Figure 12, Case B, $t_{GL} < t_{REH}$). Deep voltage drops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and are taken as the beginning of a new time slot (Figure 12, Case C, $t_{GL} \geq t_{REH}$).

CRC Generation

The DS28E07 uses two different types of CRCs. One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM ID. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM ID and compare it to the value stored within the DS28E07 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28E07 chip (Figure 13) calculates a new 16- bit CRC, as shown in the command flowchart (Figure 7). The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error.

With the Write Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, and all the data bytes as they were sent by the bus master. The DS28E07 transmits this CRC only if E[2:0] = 111b.

With the Read Scratchpad command, the CRC is generated by first clearing the CRC generator and then shifting in the command code, the target addresses TA1 and TA2, the E/S byte, and the scratchpad data as they were sent by the DS28E07. The DS28E07 transmits this CRC only if the reading continues through the end of the scratchpad. For more information on generating CRC values, refer to Application Note 27.

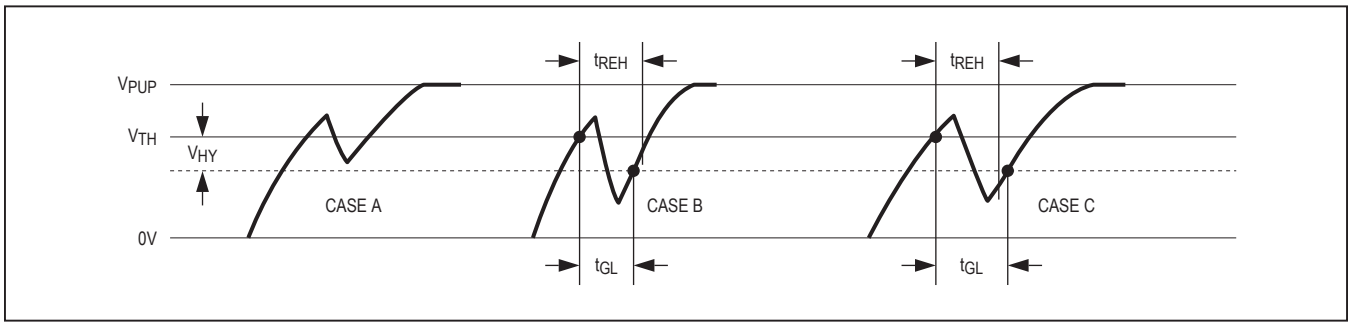

Figure 12. Noise Suppression Scheme

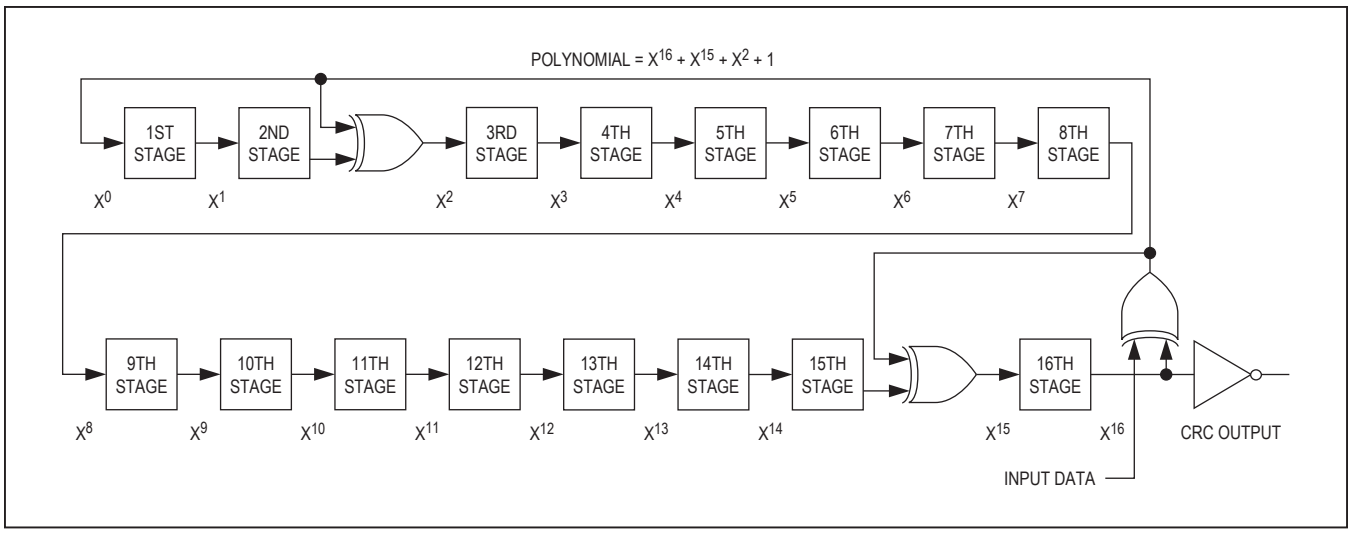

Figure 13. CRC-16 Hardware Description and Polynomial

Command-Specific 1-Wire Communication Protocol—Color Codes

Master to Slave	Slave to Master	Programming

Command-Specific 1-Wire Communication Protocol—Legend

SYMBOL	DESCRIPTION
RST	1-Wire Reset Pulse generated by master.
PD	1-Wire Presence Pulse generated by slave.
Select	Command and data to satisfy the ROM function protocol (e.g. Skip ROM [CCh], etc…).
WS	Command “Write Scratchpad [0Fh]”.
RS	Command “Read Scratchpad [AAh]”.
CPS	Command “Copy Scratchpad [55h]”.
RM	Command “Read Memory [F0h]”.
TA	Target Address TA1, TA2.
TA-E/S	Target Address TA1, TA2 with E/S byte.
<8 – T2:T0 bytes>	Transfer of as many bytes as needed to reach the end of the scratchpad for a given target address.
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the memory.
$\overline{\text{CRC16}}$	Transfer of an inverted $\overline{\text{CRC16}}$.
FF loop	Indefinite loop where the master reads FF bytes.
AA loop	Indefinite loop where the master reads AA bytes.
Programming	Data transfer to EEPROM; no activity on the 1-Wire bus permitted during this time.

1-Wire Communication Examples

Write Scratchpad (CANNOT FAIL)

RST	PD	Select	WS	TA	<8 – T2:T0 bytes>	$\overline{\text{CRC16}}$	FF loop

Read Scratchpad (CANNOT FAIL)

RST	PD	Select	RS	TA-E/S	<8 – T2:T0 bytes>	$\overline{\text{CRC16}}$	FF loop

Copy Scratchpad (success)

RST	PD	Select	CPS	TA-E/S	Programming	AA loop

Copy Scratchpad (invalid ADDRESS or PF = 1 or COPY protected)

RST	PD	Select	CPS	TA-E/S	FF loop

Read Memory (success)

RST	PD	Select	RM	TA	<data to EOM>	FF loop

Read Memory (invalid address)

RST	PD	Select	RM	TA	FF loop

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E07+	-40°C to +85°C	3 TO-92
DS28E07+T	-40°C to +85°C	3 TO-92 (2k pcs)
DS28E07P+	-40°C to +85°C	6 TSOC
DS28E07P+T	-40°C to +85°C	6 TSOC (4k pcs)
DS28E07Q+T	-40°C to +85°C	6 TDFN-EP* (2.5k pcs)

+Denotes a lead-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
3 TO-92 (Bulk)	Q3+1	**21-0248**	—
3 TO-92 (T&R)	Q3+4	**21-0250**	—
6 TSOC	D6+1	**21-0382**	**90-0321**
6 TDFN-EP	T633+2	**21-0137**	**90-0058**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/15	Initial release	—
1	5/16	Removed future product references	22
2	1/17	Added row to Output Low Voltage parameter and removed Note 12 (remaining Notes were not renumbered per request)	2, 4

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