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FAIRCHILD SEMICONDUCTOR®

September 2012

FSL206MR
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET: 650V
- Precision Fixed Operating Frequency: 67kHz
- No-Load <150mW at 265V_{AC} without Bias Winding; <25mW with Bias Winding for FSL206MR, <30mW with Bias Winding for FSL206MRBN
- No Need for Auxiliary Bias Winding
- Frequency Modulation for Attenuating EMI
- Line Under-Voltage Protection (LUVP)
- Pulse-by-Pulse Current Limiting
- Low Under-Voltage Lockout (UVLO)
- Ultra-Low Operating Current: 300µA
- Built-In Soft-Start and Startup Circuit
- Various Protections: Overload Protection (OLP), Over-Voltage Protection (OVP), Thermal Shutdown (TSD), Abnormal Over-Current Protection (AOCP) Auto-Restart Mode for All Protections

Applications

- SMPS for STB, DVD, and DVCD Player
- SMPS for Auxiliary Power

Related Resources

- *Fairchild Power Supply WebDesigner – Flyback Design and Simulation – In Minutes at No Expense*
- *AN-4137 — Design Guidelines for Offline Flyback Converters Using FPS™*
- *AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147 — Design Guidelines for RCD Snubber of Flyback*
- *AN-4150 — Design Guidelines for Flyback Converters Using FSQ-Series Fairchild Power Switch (FPS™)*

Description

The FSL206MR integrated Pulse-Width Modulator (PWM) and SenseFET is specifically designed for high-performance offline Switched-Mode Power Supplies (SMPS) while minimizing external components. This device integrates high-voltage power regulators that combine an avalanche-rugged SenseFET with a Current-Mode PWM control block.

The integrated PWM controller includes: a 7.8V regulator, eliminating the need for auxilliary bias winding; Under-Voltage Lockout (UVLO) protection; Leading-Edge Blanking (LEB); an optimized gate turn-on/turn-off driver; EMI attenuator; Thermal Shutdown (TSD) protection; temperature-compensated precision current sources for loop compensation; soft-start during startup; and fault-protection circuitry such as Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), and Line Under-Voltage Protection (LUVP).

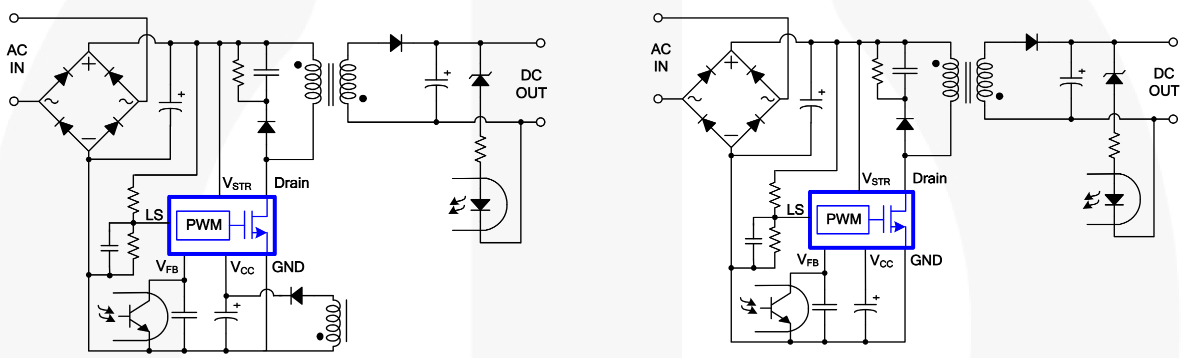
The internal high-voltage startup switch and the Burst-Mode operation with very low operating current reduce the power loss in Standby Mode. As a result, it is possible to reach a power loss of 150mW with no bias winding and 25mW (for FSL206MR) or 30mW (for FSL206MRBN) with a bias winding under no-load conditions when the input voltage is 265V_{AC}.

Ordering Information

Part Number	Operating Temperature	Top Mark	PKG	Packing Method	Output Power Table[1]			
					Current Limit	$R_{DS(ON),MAX}$	$230V_{AC}$ ±15%[2]	85 ~ $265V_{AC}$
							Open Frame[3]	Open Frame[3]
FSL206MRN	-40 ~ 115°C	FSL206MR	8-DIP	Rail	0.6A	19Ω	12W	7W
FSL206MRL			8-LSOP					
FSL206MRBN		L206MRB	8-DIP					

Notes:
1. The junction temperature can limit the maximum output power.
2. $230V_{AC}$ or $100/115V_{AC}$ with doubler. The maximum power with CCM operation.
3. Maximum practical continuous power in an open-frame design at 50°C ambient.

Application Diagram



(a) With Bias Winding (b) Without Bias Winding

Figure 1. Typical Application

Internal Block Diagram

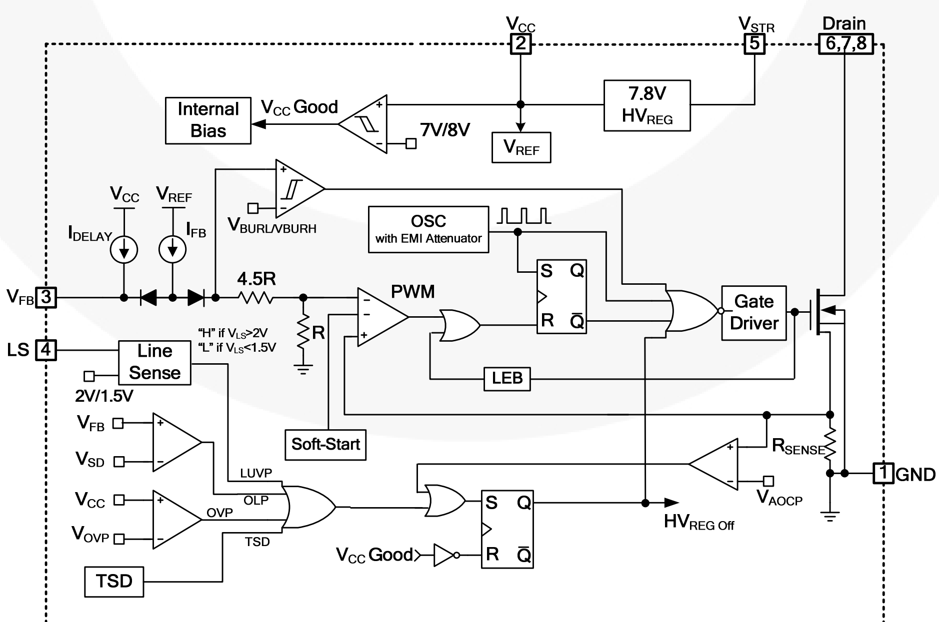


Figure 2. Internal Block Diagram

Pin Configuration

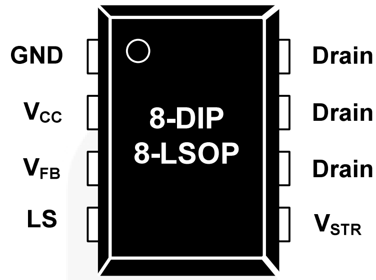


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	**Positive Supply Voltage Input**. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{STR}) via an internal switch during startup *(see Internal Block Diagram section)*. It is not until V_{CC} reaches the UVLO upper threshold (8V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V_{FB}	**Feedback Voltage**. Non-inverting input to the PWM comparator, with a 0.11mA current source connected internally and a capacitor and opto-coupler typically connected externally. There is a delay while charging external capacitor C_{FB} from 2.4V to 5V using an internal 2.7µA current source. This delay prevents false triggering under transient conditions, but allows the protection mechanism to operate under true overload conditions.
4	LS	Line Sense Pin. This pin is used to protect the device when the input voltage is lower than the rated input voltage range. If this pin is not used, connect to ground.
5	V_{STR}	**Startup**. Connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once V_{CC} reaches 8V, all internal blocks are activated. After that, the internal high-voltage regulator (HV REG) turns on and off irregularly to maintain V_{CC} at 7.8V.
6, 7, 8	Drain	**Drain**. Designed to connect directly to the primary lead of the transformer and capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage	-0.3	650.0	V
V_{DS}	Drain Pin Voltage	-0.3	650.0	V
V_{CC}	Supply Voltage		26	V
V_{LS}	LS Pin Voltage	-0.3	Internally Clamped Voltage(4)	V
V_{FB}	Feedback Voltage Range	-0.3	Internally Clamped Voltage(4)	V
I_{DM}	Drain Current Pulsed(5)		1.5	A
E_{AS}	Single-Pulsed Avalanche Energy(6)		11	mJ
P_D	Total Power Dissipation		1.3	W
T_J	Operating Junction Temperature	-40	+150	°C
T_A	Operating Ambient Temperature	-40	+125	°C
T_{STG}	Storage Temperature	-55	+150	°C
ESD	Human Body Model, JESD22-A114		4	KV
	Charged Device Model, JESD22-C101		2	

Notes:

4. V_{FB} is clamped by internal clamping diode (13V I_{CLAMP_MAX} < 100µA). After shutdown, before V_{CC} reaching V_{STOP}, $V_{SD} < V_{FB} < V_{CC}$.
5. Repetitive rating: pulse-width limited by maximum junction temperature.
6. L=21mH, starting T_J=25°C.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance(7)	93	°C/W

Notes:

7. JEDEC recommended environment, JESD51-2 and test board, JESD51-10 with minimum land pattern for 8DIP and JESD51-3 with minimum land pattern for 8LSOP.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC} = 0V, I_D = 250μA	650			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V			50	μA
		V_{DS} = 520V, V_{GS} = 0V, T_A = 125°C(8)			250	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance(9)	V_{GS} = 10V, I_D = 0.3A		14	19	Ω
C_{iSS}	Input Capacitances	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		162		pF
C_{OSS}	Output Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		14.9		pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		2.7		pF
t_r	Rise Time	V_{DS} = 325V, I_D = 0.5A, R_G = 25Ω		6.1		ns
t_f	Fall Time	V_{DS} = 325V, I_D = 0.5A, R_G = 25Ω		43.6		ns
Control Section						
f_{OSC}	Switching Frequency	V_{FB} = 4V, V_{CC} = 10V	61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation	-25°C < T_J < 85°C		±5	±10	%
f_M	Frequency Modulation(8)			±3		KHz
D_{MAX}	Maximum Duty Cycle	V_{FB} = 4V, V_{CC} = 10V	66	72	78	%
D_{MIN}	Minimum Duty Cycle	V_{FB} = 0V, V_{CC} = 10V	0	0	0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = 0V, V_{CC} Sweep	7	8	9	V
V_{STOP}		After Turn On	6	7	8	V
I_{FB}	Feedback Source Current	V_{FB}= 0V, V_{CC} = 10V	90	110	130	μA
$t_{S/S}$	Internal Soft-Start Time	V_{FB} = 4V, V_{CC} = 10V	10	15	20	ms
Burst Mode Section						
V_{BURH}	Burst-Mode HIGH Threshold Voltage	V_{CC} = 10V, V_{FB} Increase; FSL206MR	0.66	0.83	1.00	V
		FSL206MRB	0.40	0.50	0.60	V
V_{BURL}	Burst-Mode LOW Threshold Voltage	V_{CC} = 10V, V_{FB} Decrease; FSL206MR	0.59	0.74	0.89	V
		FSL206MRB	0.28	0.35	0.42	V
HYS_{BUR}	Burst-Mode Hysteresis	FSL206MR		90		mV
		FSL206MRB		150		mV
Protection Section						
I_{LIM}	Peak Current Limit	V_{FB} = 4V, di/dt = 300mA/μs, V_{CC} = 10V	0.54	0.60	0.66	A
t_{CLD}	Current Limit Delay(8)			100		ns
V_{SD}	Shutdown Feedback Voltage	V_{CC} = 10V	4.5	5.0	5.5	V
I_{DELAY}	Shutdown Delay Current	V_{FB} = 4V	2.1	2.7	3.3	μA
t_{LEB}	Leading-Edge Blanking Time(8)		250			ns
V_{AOCP}	Abnormal Over-Current Protection(8)			0.7		V
V_{OVP}	Over-Voltage Protection	V_{FB} = 4V, V_{CC} Increase	23.0	24.5	26.0	V
V_{LS_OFF}	Line-Sense Protection On to Off	V_{FB} = 3V, V_{CC} = 10V, V_{LS} Decrease	1.9	2.0	2.1	V
V_{LS_ON}	Line-Sense Protection Off to On	V_{FB} = 3V, V_{CC} = 10V, V_{LS} Increase	1.4	1.5	1.6	V
TSD	Thermal Shutdown Temperature(8)		125	135	150	°C
HYS_{TSD}	TSD Hysteresis Temperature(8)			60		°C

Continued on the following page…

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
High Voltage Regulator Section						
V_{HVR}	HV Regulator Voltage	V_{FB} = 0V, V_{STR} = 40V		7.8		V
Total Device Section						
I_{OP1}	Operating Supply Current (Control Part Only, without Switching)	V_{CC} = 15V, 0V<V_{FB}<V_{BURL}		0.3	0.5	mA
I_{OP2}	Operating Supply Current (Control Part Only, without Switching)	V_{CC} = 8V, 0V<V_{FB}<V_{BURL}		0.25	0.45	mA
I_{OP3}	Operating Supply Current(8) (While Switching)	V_{CC} = 15V, V_{BURL}<V_{FB}<V_{SD}			1.3	mA
I_{CH}	Startup Charging Current	V_{CC} = 0V, V_{STR} > 40V	1.6	1.9	2.2	mA
I_{START}	Startup Current	V_{CC} = Before V_{START}, V_{FB} = 0V		100	150	μA
V_{STR}	Minimum V_{STR} Supply Voltage	V_{CC} = V_{FB} = 0V, V_{STR} Increase		26		V

Notes:
8. Though guaranteed by design, not 100% tested in production.
9. Pulse test: pulse width=300ms, duty cycle=2%.

Typical Performance Characteristics

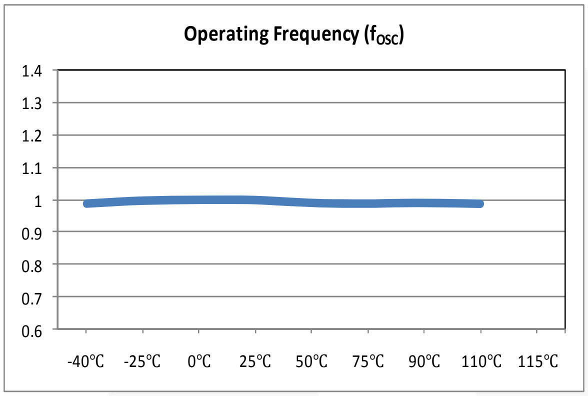


Figure 4. Operating Frequency vs. Temperature

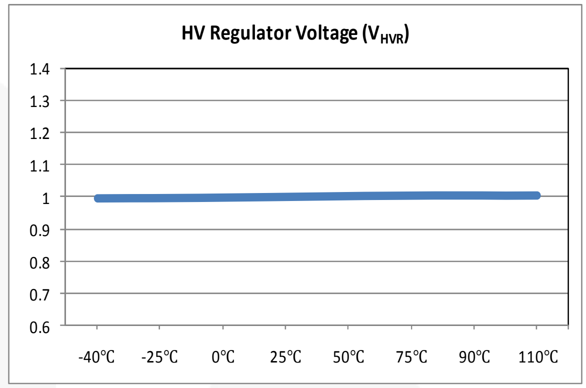


Figure 5. HV Regulator Voltage vs. Temperature

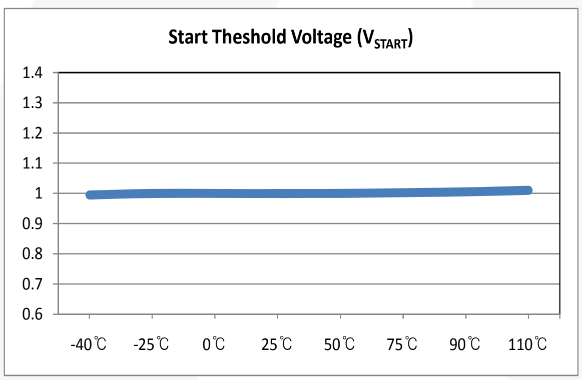


Figure 6. Start Threshold Voltage vs. Temperature

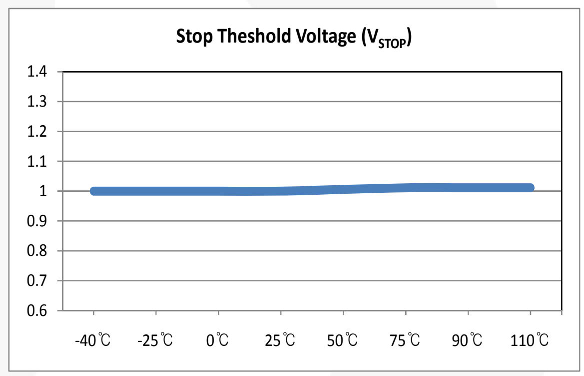


Figure 7. Stop Threshold Voltage vs. Temperature

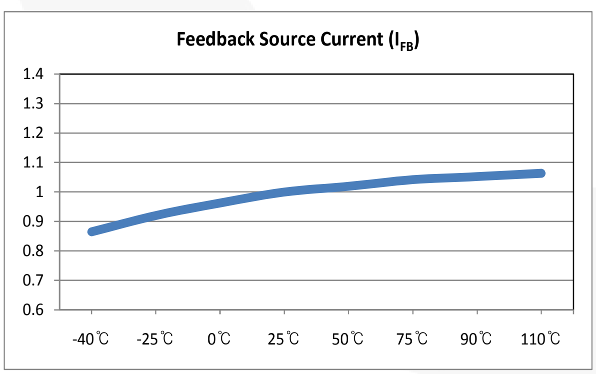


Figure 8. Feedback Source Current vs. Temperature

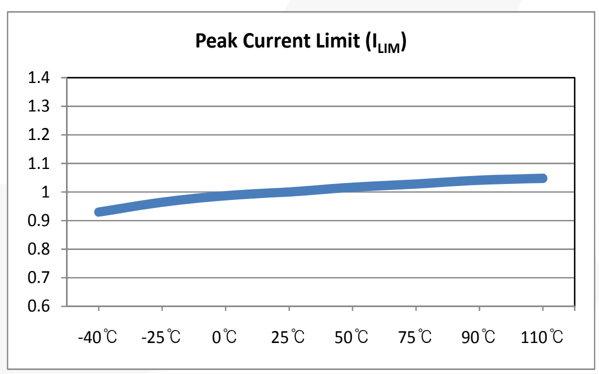


Figure 9. Peak Current Limit vs. Temperature

Typical Performance Characteristics (Continued)

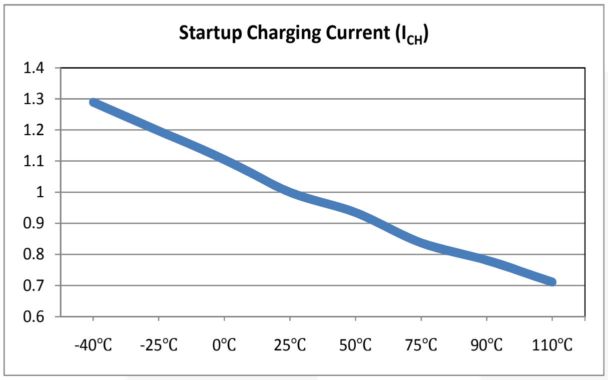


Figure 10. Startup Charging Current vs. Temperature

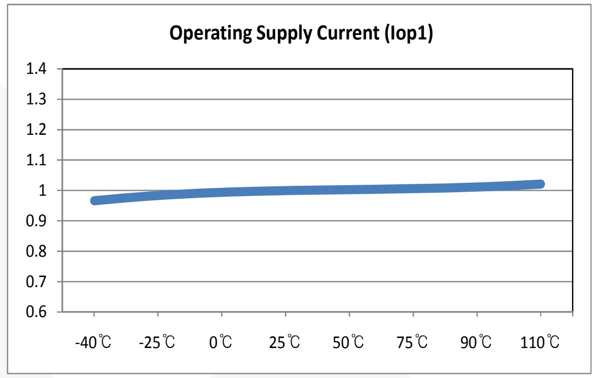


Figure 11. Operating Supply Current 1 vs. Temperature

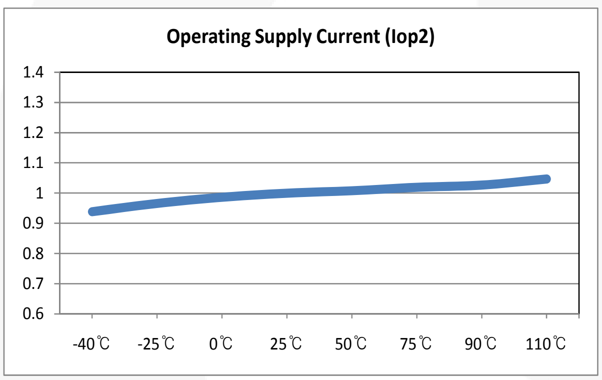


Figure 12. Operating Supply Current 2 vs. Temperature

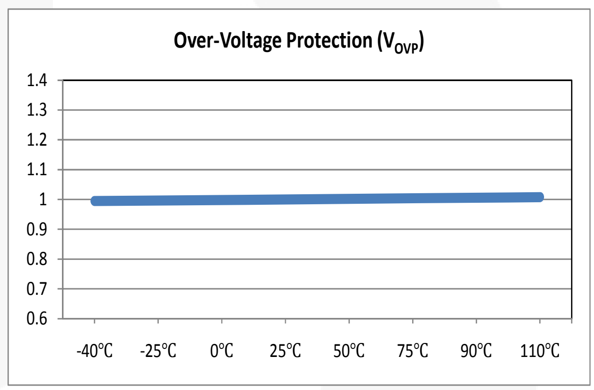


Figure 13. Over-Voltage Protection Voltage vs. Temperature

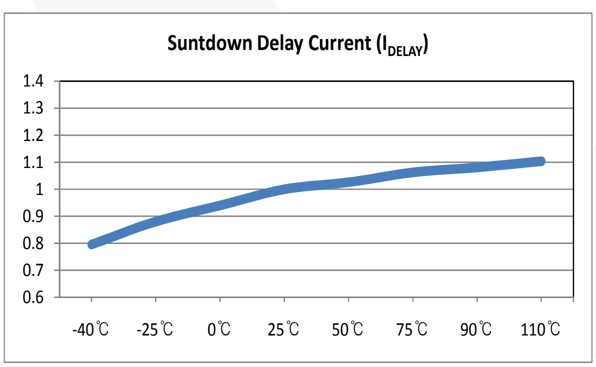


Figure 14. Shutdown Delay Current vs. Temperature

Functional Description

Startup

At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_A) connected to the V_{CC} pin, as illustrated in Figure 15. An internal high-voltage regulator (HV REG) located between the V_{STR} and V_{CC} pins regulates the V_{CC} to 7.8V and supplies operating current. Therefore, FSL206MR needs no auxiliary bias winding.

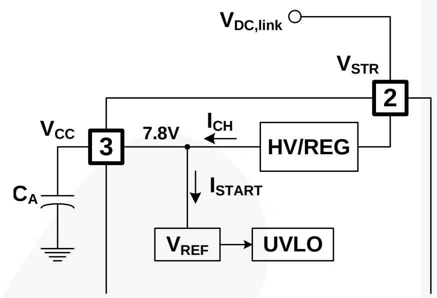


Figure 15. Startup Block

Oscillator Block

The oscillator frequency is set internally and the FPS™ has a random frequency fluctuation function.

Fluctuation of the switching frequency can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the range of the frequency variation. The range of frequency variation is fixed internally; however, its selection is randomly chosen by the combination of an external feedback voltage and internal free-running oscillator. This randomly chosen switching frequency effectively spreads the EMI noise near switching frequency and allows the use of a cost-effective inductor instead of an AC input line filter to satisfy world-wide EMI requirements.

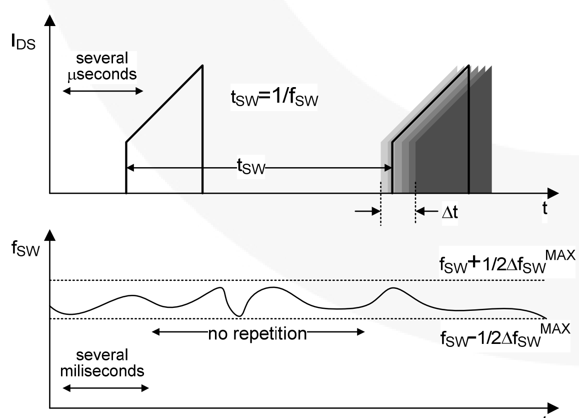


Figure 16. Frequency Fluctuation Waveform

Feedback Control

FSL206MR employs Current-Mode control, as shown in Figure 17. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V; the opto-coupler LED current increases, feedback voltage V_{FB} is pulled down, and the duty cycle is reduced. This typically occurs when input voltage is increased or output load is decreased.

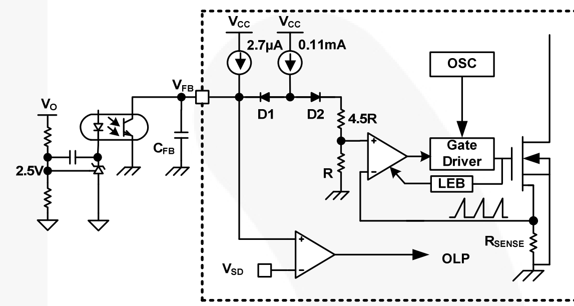


Figure 17. Pulse-Width-Modulation (PWM) Circuit

Leading-Edge Blanking (LEB)

At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the Current-Mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit (*see Figure 17*). This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

Protection Circuits

The protective functions include Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), Line Under-Voltage Protection (LUVP), Abnormal Over-Current Protection (AOCP), and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{STR} pin. When V_{CC} reaches the UVLO start voltage V_{START} (8V), the FPS resumes normal operation. In this manner, auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

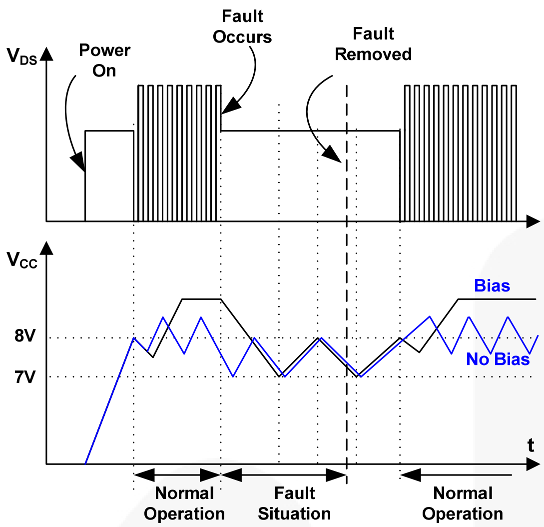


Figure 18. Auto-Restart Protection Waveforms

Overload Protection (OLP)

Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the overload protection (OLP) circuit can be activated during the load transition or startup. To avoid this undesired operation, the OLP circuit is activated after a specified time to determine whether it is a transient situation or a true overload situation. The Current-Mode feedback path limits the current in the SenseFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_O) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4V, the feedback input diode is blocked and the 2.7µA current source (I_{DELAY}) starts to charge C_{FB} slowly up. In this condition, V_{FB} increases until it reaches 5V, when the switching operation is terminated, as shown in Figure 19. The shutdown delay is the time required to charge C_{FB} from 2.4V to 5V with 2.7µA current source.

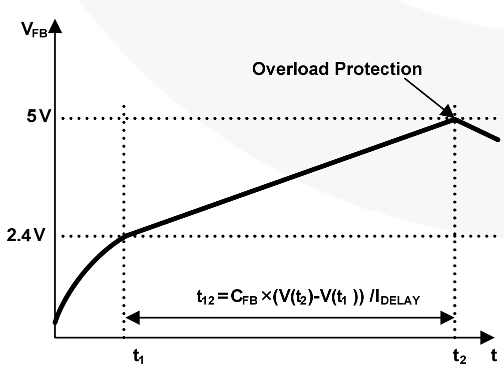


Figure 19. Overload Protection (OLP)

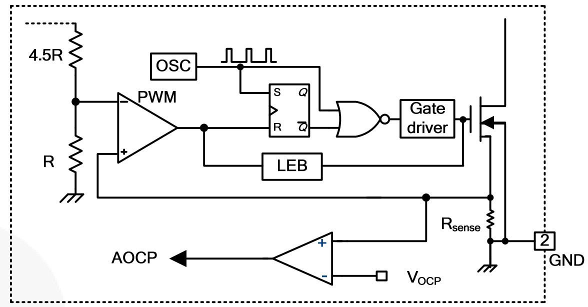


Figure 20. Abnormal Over-Current Protection

Abnormal Over-Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pin are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FPS has overload protection, it is not enough to protect the FPS in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FPS includes the internal AOCP (Abnormal Over-Current Protection) circuit shown in Figure 20. When the gate turn-on signal is applied to the power sense, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing-resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

Thermal Shutdown (TSD)

The SenseFET and control IC being integrated makes it easier to detect the temperature of the SenseFET. When the junction temperature exceeds ~135°C, thermal shutdown is activated and the FPS is restarted after temperature decreases to 60°C.

Over-Voltage Protection (OVP)

In the event of a malfunction in the secondary-side feedback circuit or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (*refer to Figure 17*). Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an over-voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, OVP circuit is activated, resulting in termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

Line Under-Voltage Protection (LUVP)

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing components failure. If the input voltage is low, the converter should be protected. In the FSL206MR, the LUVP circuit senses the input voltage using the LS pin and, if this voltage is lower than 1.5V, the LUVP signal is generated. The comparator has 0.5V hysteresis. If the LUVP signal is generated, the output drive block is shut down and the output voltage feedback loop is saturated.

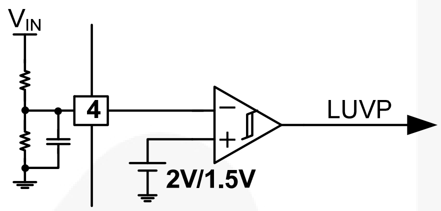


Figure 21. Line UVP Circuit

Soft-Start

The FSL206MR has an internal soft-start circuit that slowly increases the feedback voltage, together with the SenseFET current, after it starts. The typical soft-start time is 15ms, as shown in Figure 22, where progressive increments of the SenseFET current are allowed during the startup phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps prevent transformer saturation and reduce the stress on the secondary diode.

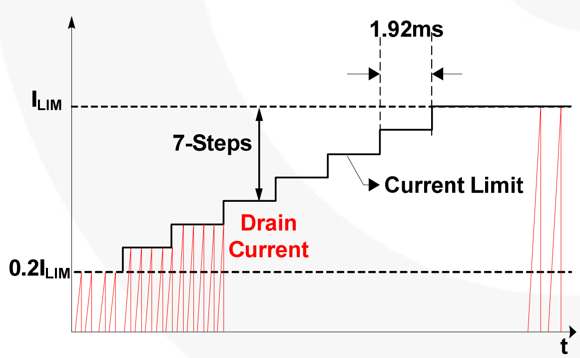


Figure 22. Internal Soft-Start

Burst Operation

To minimize power dissipation in Standby Mode, the FPS enters Burst Mode. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURH}. Switching continues until the feedback voltage drops below V_{BURL}. At this point, switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the SenseFET and reduces switching loss in Standby Mode.

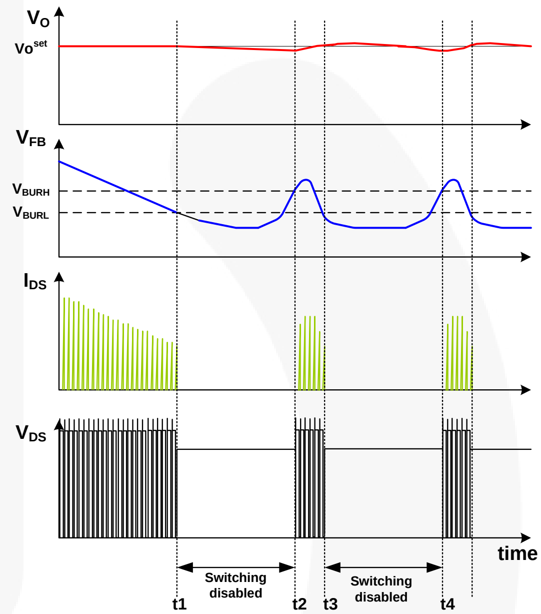
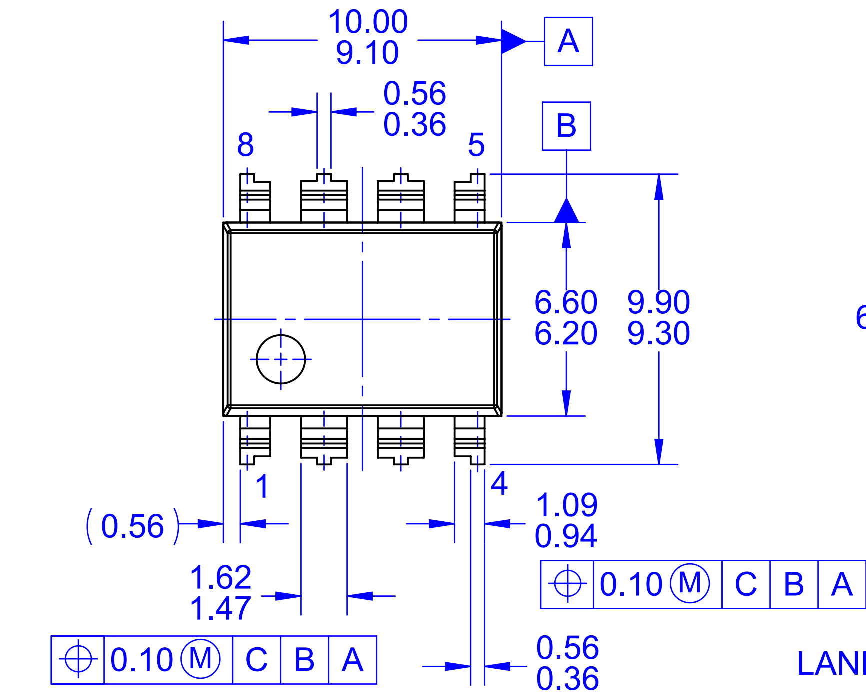
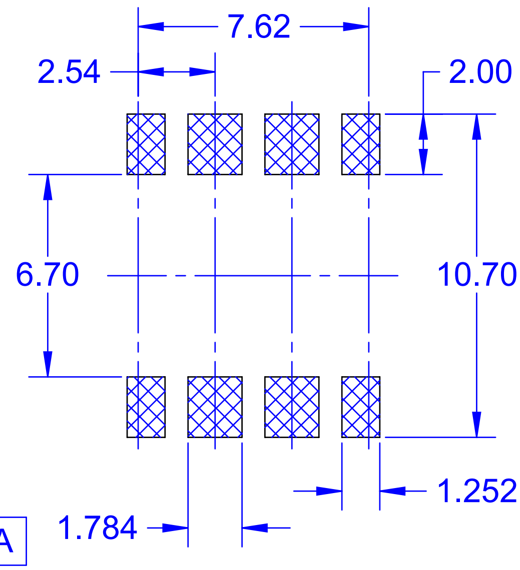


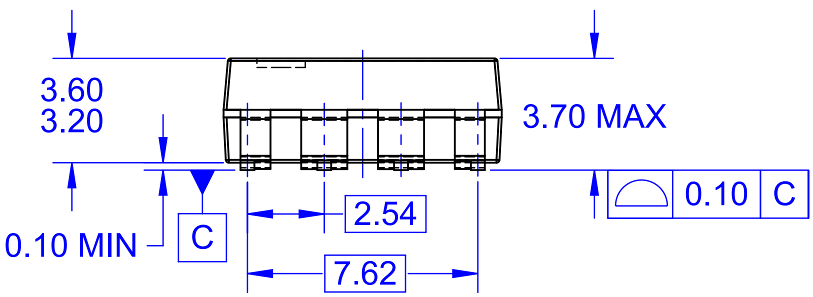
Figure 23. Burst-Mode Operation



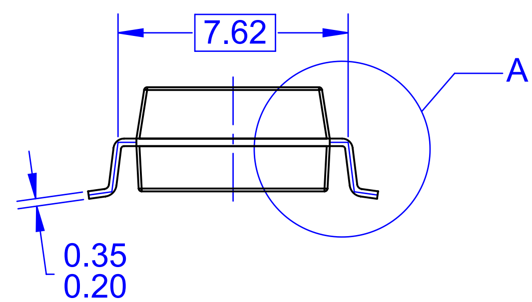
TOP VIEW



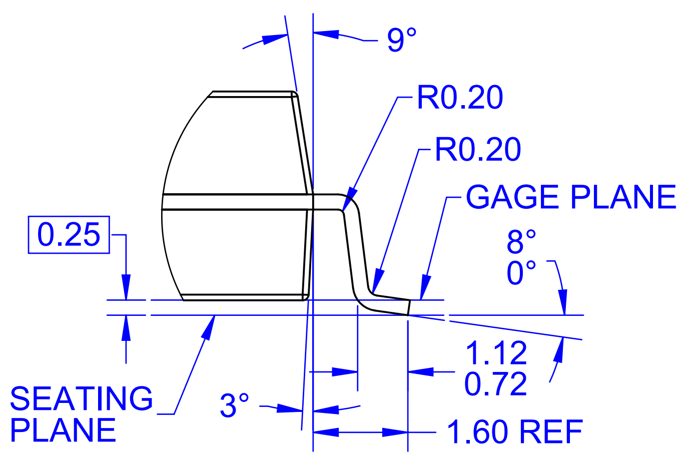
LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW



DETAIL A
SCALE 2:1

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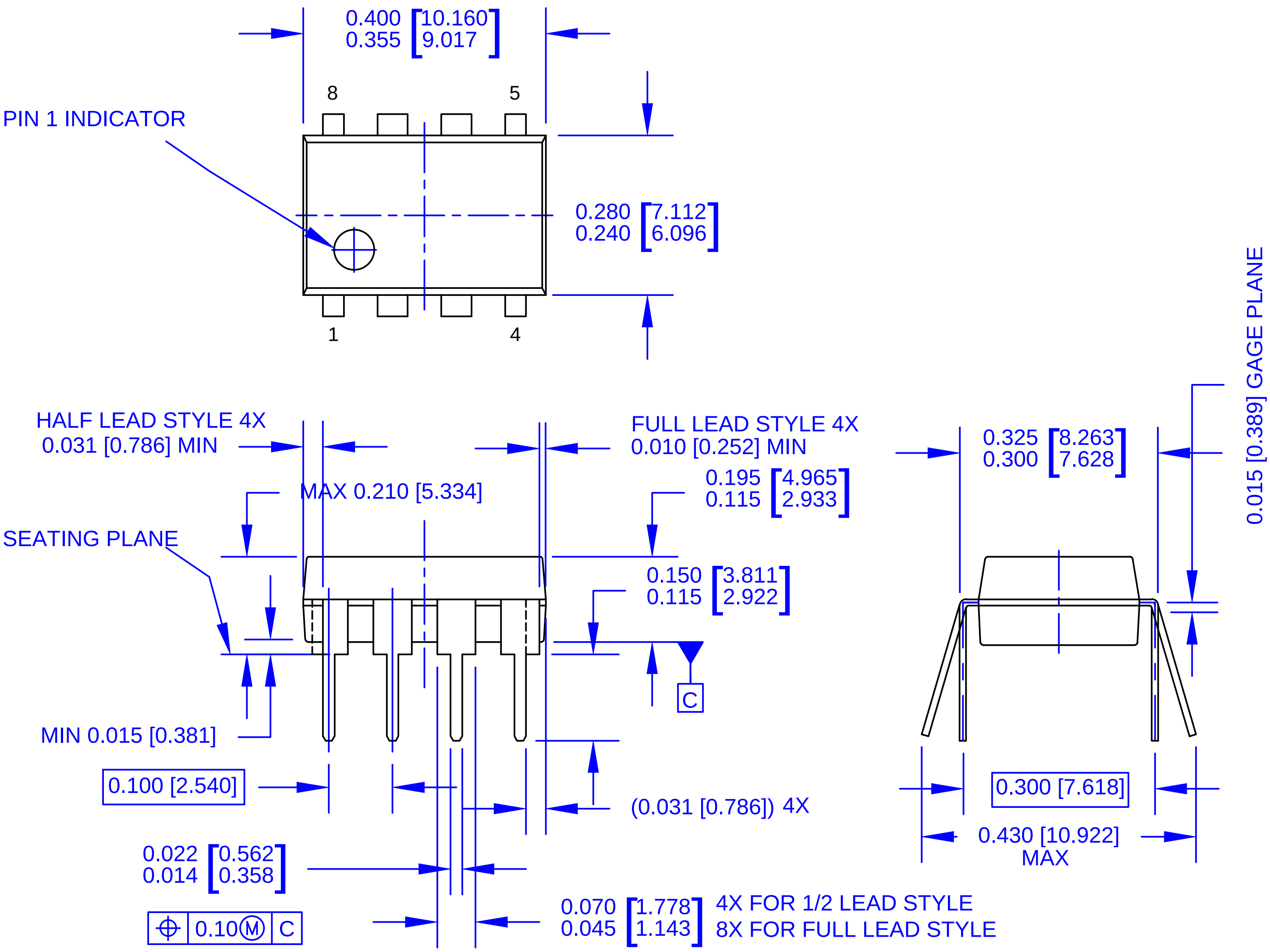

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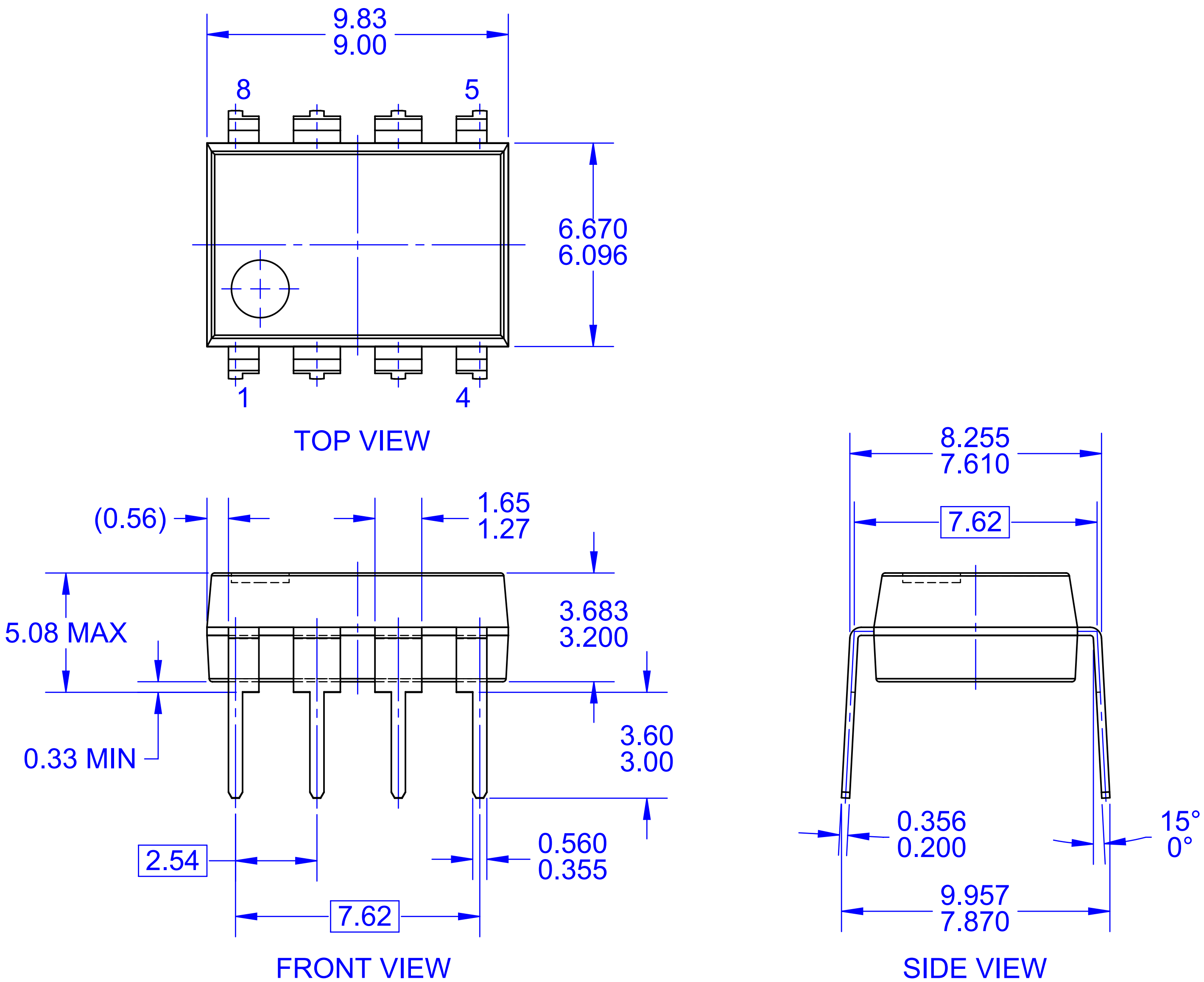

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