

FEATURES

- 1.8 V to 5.5 V single supply**
- Low on resistance (2.5 Ω Typ)**
- Low on resistance flatness**
- 3 dB bandwidth > 200 MHz**
- Rail-to-rail operation**
- 16-lead TSSOP and SOIC packages**
- Fast switching times: $t_{ON} = 16$ ns, $t_{OFF} = 10$ ns**
- Typical power consumption (< 0.01 μ W)**
- TTL/CMOS compatible**
- Qualified for automotive applications**

APPLICATIONS

- USB 1.1 signal switching circuits**
- Cell phones**
- PDA's**
- Battery-powered systems**
- Communication systems**
- Sample hold systems**
- Audio signal routing**
- Video switching**
- Mechanical reed relay replacement**

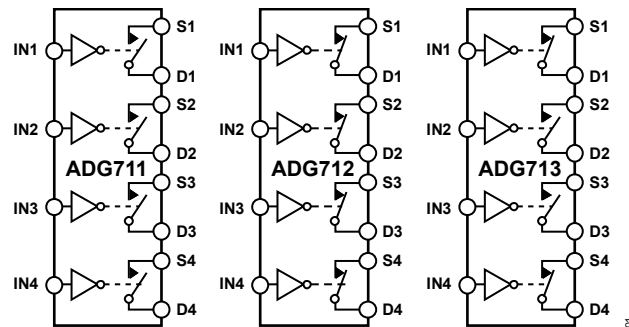
GENERAL DESCRIPTION

The [ADG711](#), [ADG712](#), and [ADG713](#) are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and high bandwidth.

They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc. Fast switching times and high bandwidth make the parts suitable for switching USB 1.1 data signals and video signals.

The [ADG711](#), [ADG712](#), and [ADG713](#) contain four independent single-pole/single-throw (SPST) switches. The [ADG711](#) and [ADG712](#) differ only in that the digital control logic is inverted. The [ADG711](#) switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the [ADG712](#). The [ADG713](#) contains two switches whose digital control logic is similar to the [ADG711](#), while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when On. The [ADG713](#) exhibits break-before-make switching action.

FUNCTIONAL BLOCK DIAGRAM


SWITCHES SHOWN FOR A LOGIC "1" INPUT

Figure 1.

00042-010

The [ADG711/ADG712/ADG713](#) are available in 16-lead TSSOP and 16-lead SOIC packages.

PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation.
The [ADG711](#), [ADG712](#), and [ADG713](#) offer high performance and are fully specified and guaranteed with 3 V and 5 V supply rails.
2. Very Low R_{ON} (4.5 Ω maximum at 5 V, 8 Ω maximum at 3 V).
At supply voltage of 1.8 V, R_{ON} is typically 35 Ω over the temperature range.
3. Low On Resistance Flatness.
4. -3 dB Bandwidth >200 MHz.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF} .
7. Break-Before-Make Switching.
This prevents channel shorting when the switches are configured as a multiplexer ([ADG713](#) only).
8. 16-Lead TSSOP and 16-Lead SOIC Packages.

Rev. B

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REVISION HISTORY

6/11—Rev. A to Rev. B

| | |
|--|-----------|
| Updated Format..... | Universal |
| Changes to Features Section..... | 1 |
| Changes to Absolute Maximum Ratings Table..... | 5 |
| Changes to Ordering Guide | 14 |
| Added Automotive Products Section | 14 |

3/04—Rev. 0 to Rev. A

| | |
|----------------------------------|----|
| Added Applications..... | 1 |
| Changes to Ordering Guide | 4 |
| Updated Outline Dimensions | 10 |

SPECIFICATIONS

$V_{DD} = +5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | Unit | Test Conditions/Comments |
|--|------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 2.5 | | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$; See Figure 11 |
| | 4 | 4.5 | Ω max | |
| On Resistance Match Between Channels (ΔR_{ON}) | | 0.05 | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| | | 0.3 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| | | 1.0 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = +5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$ |
| | ± 0.1 | ± 0.2 | nA max | See Figure 12 |
| Drain Off Leakage I_D (Off) | ± 0.01 | | nA typ | $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$ |
| | ± 0.1 | ± 0.2 | nA max | See Figure 12 |
| Channel On Leakage I_D, I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = 1\text{ V}$, or 4.5 V |
| | ± 0.1 | ± 0.2 | nA max | See Figure 13 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| t_{ON} | 11 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 16 | ns max | $V_S = 3\text{ V}$; see Figure 14 |
| t_{OFF} | 6 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 10 | ns max | $V_S = 3\text{ V}$; see Figure 14 |
| Break-Before-Make Time Delay, t_D (ADG713 Only) | 6 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 1 | ns min | $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 15 |
| Charge Injection | 3 | | pC typ | $V_S = 2\text{ V}$; $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 16 |
| Off Isolation | -58 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ |
| | -78 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 17 |
| Channel-to-Channel Crosstalk | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 18 |
| Bandwidth -3 dB | 200 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 19 |
| C_S | 10 | | pF typ | |
| C_D | 10 | | pF typ | |
| C_D, C_S (On) | 22 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +5.5\text{ V}$ Digital inputs = 0 V or 5 V |
| | | 1.0 | μA max | |

¹ Guaranteed by design, not subject to production test.

ADG711/ADG712/ADG713

$V_{DD} = +3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | -40°C to +85°C | Unit | Test Conditions/Comments |
|--|------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 5 | 5.5 | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$; See Figure 11 |
| | | 8 | Ω max | |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.1 | 0.3 | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| | | 2.5 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | | | Ω typ | $V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$ |
| | ± 0.1 | ± 0.2 | nA max | See Figure 12 |
| Drain Off Leakage I_D (Off) | ± 0.01 | | nA typ | $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$ |
| | ± 0.1 | ± 0.2 | nA max | See Figure 12 |
| Channel On Leakage I_D , I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = 1\text{ V}$, or 3 V |
| | ± 0.1 | ± 0.2 | nA max | See Figure 13 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | 0.4 | V max | |
| Input Current I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| t_{ON} | 13 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 20 | ns max | $V_S = 2\text{ V}$; see Figure 14 |
| t_{OFF} | 7 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 12 | ns max | $V_S = 2\text{ V}$; see Figure 14 |
| Break-Before-Make Time Delay, t_D (ADG713 Only) | 7 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | 1 | ns min | $V_{S1} = V_{S2} = 2\text{ V}$; see Figure 15 |
| Charge Injection | 3 | | pC typ | $V_S = 1.5\text{ V}$; $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 16 |
| Off Isolation | -58 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ |
| | -78 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 17 |
| Channel-to-Channel Crosstalk | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 18 |
| Bandwidth -3 dB | 200 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 19 |
| C_S | 10 | | pF typ | |
| C_D | 10 | | pF typ | |
| C_D , C_S (On) | 22 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +3.3\text{ V}$ Digital inputs = 0 V or 3 V |
| | | 1.0 | μA max | |

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|-------------------------------------|---|
| V_{DD} to GND | -0.3 V to +6 V |
| Analog, Digital Inputs ¹ | -0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first |
| Continuous Current, S or D | 30 mA |
| Peak Current, S or D | 100 mA (Pulsed at 1 ms, 10% duty cycle maximum) |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| TSSOP Package, Power Dissipation | 430 mW |
| θ_{JA} Thermal Impedance | 150°C/W |
| θ_{JC} Thermal Impedance | 27°C/W |
| SOIC Package, Power Dissipation | 520 mW |
| θ_{JA} Thermal Impedance | 125°C/W |
| θ_{JC} Thermal Impedance | 42°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| Soldering (Pb-Free) | |
| Reflow, Peak Temperature | 260(+0/-5)°C |
| Time at Peak Temperature | 20 sec to 40 sec |
| ESD | 2 kV |

¹ Overvoltages at IN, S or D will be clamped by internal diodes. Currents should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

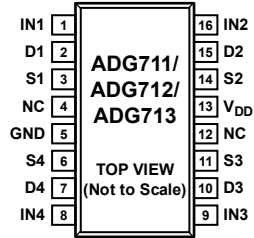
ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG711/ADG712/ADG713

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

00042-904

Figure 2. Pin Configuration

Table 4.

| Pin Number | Mnemonic | Description |
|------------|-----------------|---|
| 1 | IN1 | Digital Control Input. Its logic state controls the status of the Switch S1-D1. |
| 2 | D1 | Drain Pin. Can be used as input or output. |
| 3 | S1 | Source Pin. Can be used as input or output. |
| 4 | NC | Not internally connected. |
| 5 | GND | The most negative power supply pin. |
| 6 | S4 | Source Pin. Can be used as input or output. |
| 7 | D4 | Drain Pin. Can be used as input or output. |
| 8 | IN4 | Digital Control Input. Its logic state controls the status of the Switch S4-D4. |
| 9 | IN3 | Digital Control Input. Its logic state controls the status of the Switch S3-D3. |
| 10 | D3 | Drain Pin. Can be used as input or output. |
| 11 | S3 | Source Pin. Can be used as input or output. |
| 12 | NC | Not internally connected. |
| 13 | V _{DD} | The most positive power supply pin. |
| 14 | S2 | Source Pin. Can be used as input or output. |
| 15 | D2 | Drain Pin. Can be used as input or output. |
| 16 | IN2 | Digital Control Input. Its logic state controls the status of the Switch S3-D3. |

Table 5. Truth Table (ADG711/ADG712)

| ADG711 In | ADG712 In | Switch Condition |
|-----------|-----------|------------------|
| 0 | 1 | On |
| 1 | 0 | Off |

Table 6. Truth Table (ADG713)

| Logic | Switch 1, 4 | Switch 2, 3 |
|-------|-------------|-------------|
| 0 | Off | On |
| 1 | On | Off |

TYPICAL PERFORMANCE CHARACTERISTICS

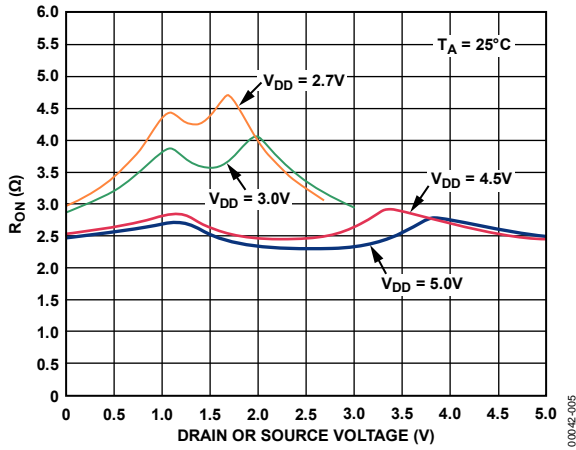


Figure 3. On Resistance as a Function of V_D (V_S)

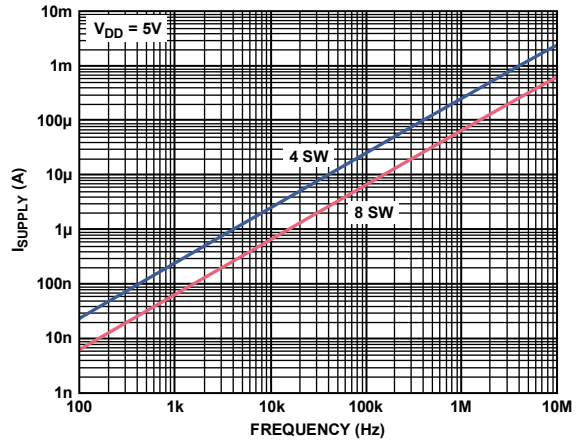


Figure 6. Supply Current vs. Input Switching Frequency

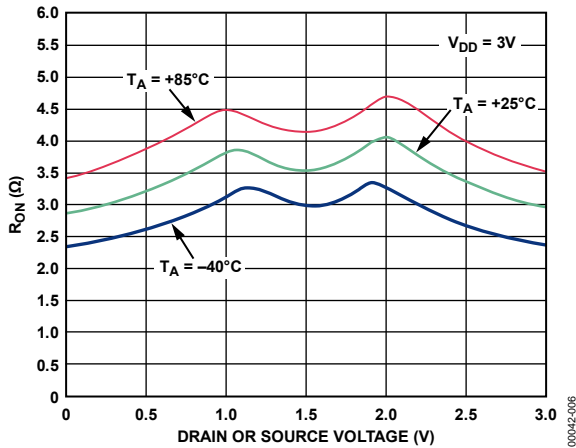


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures
 $V_{DD} = 3V$

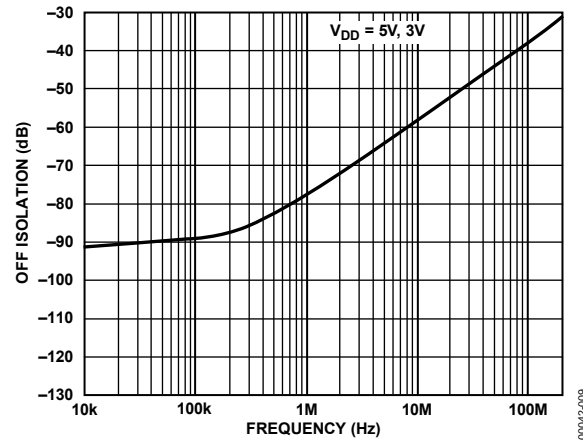


Figure 7. Off Isolation vs. Frequency

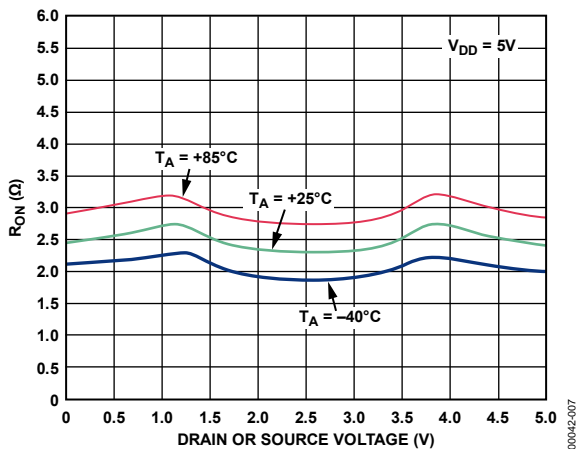


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures
 $V_{DD} = 5V$

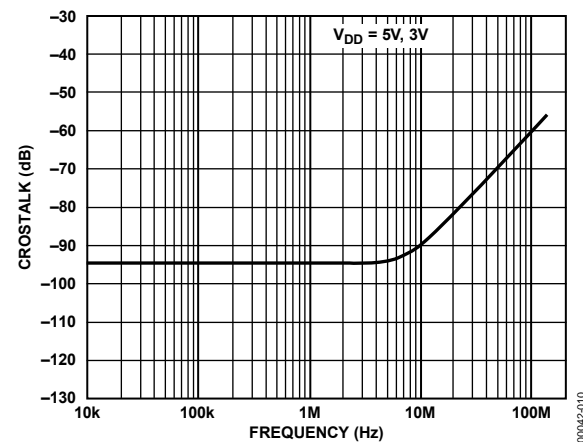


Figure 8. Crosstalk vs. Frequency

ADG711/ADG712/ADG713

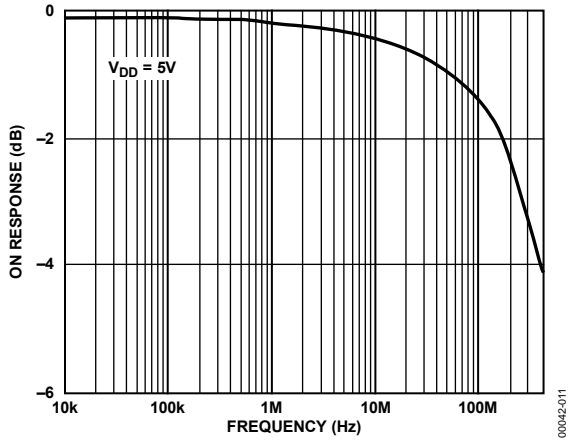


Figure 9. On Response vs. Frequency

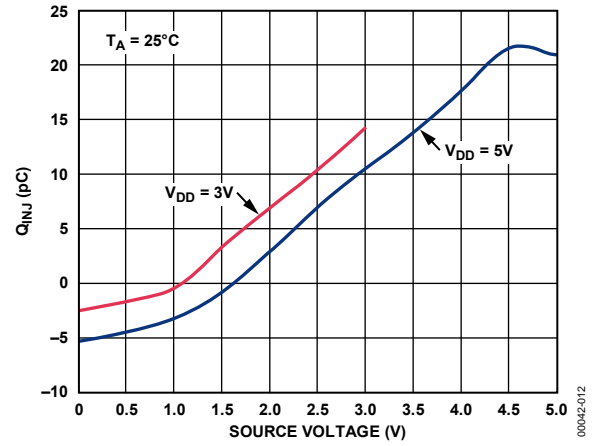


Figure 10. Charge Injection vs. Source Voltage

TEST CIRCUITS

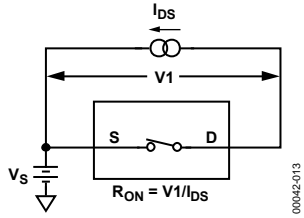


Figure 11. On Resistance

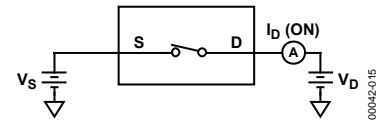


Figure 13. On Leakage

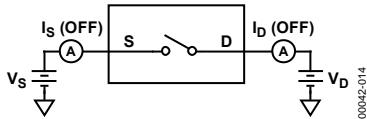


Figure 12. Off Leakage

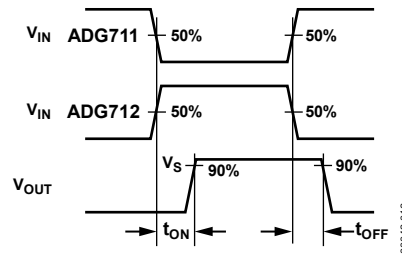
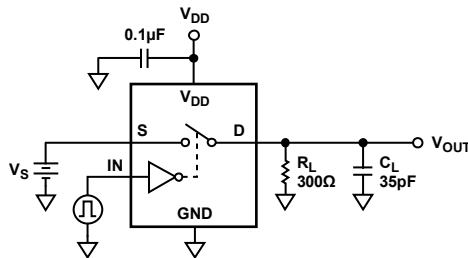


Figure 14. Switching Times

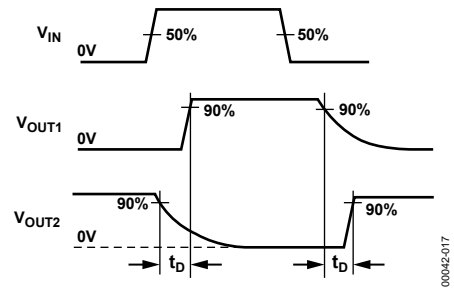
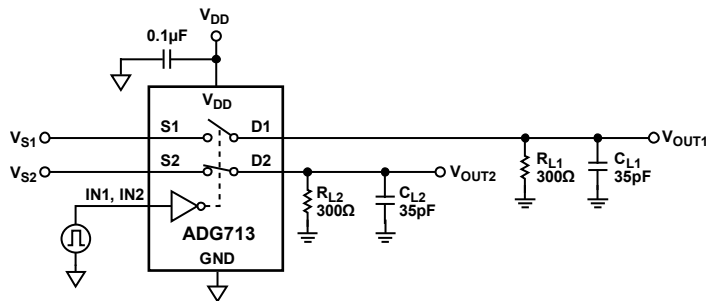


Figure 15. Break-Before-Make Time Delay, t_D

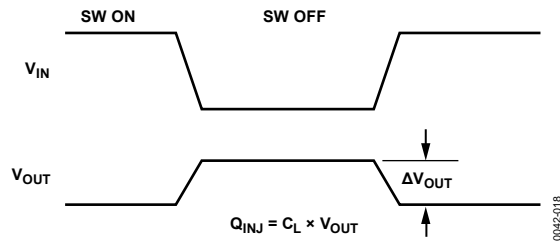
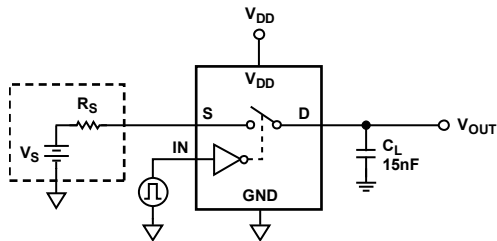
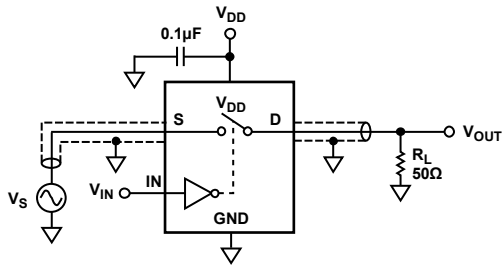


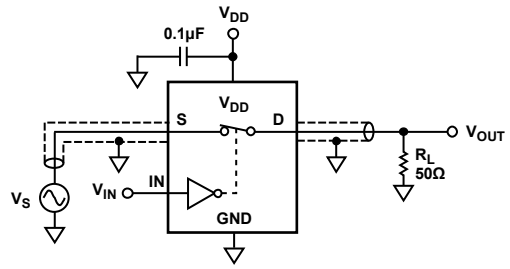
Figure 16. Charge Injection

ADG711/ADG712/ADG713



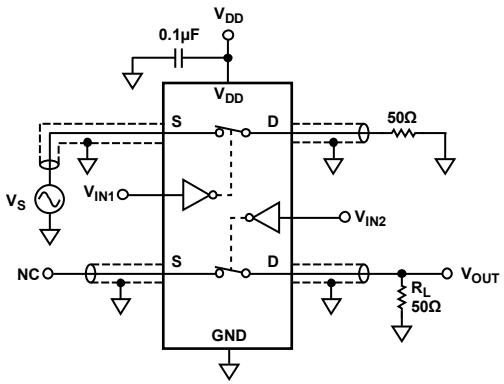
00042-019

Figure 17. Off Isolation



00042-021

Figure 19. Bandwidth



00042-020

$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \log |V_S/V_{OUT}|$$

Figure 18. Channel-to-Channel Crosstalk

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

On resistance match between any two channels, ie., $R_{ONmax} - R_{ONmin}$.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (OFF)

Source leakage current with the switch off.

I_D (OFF)

Drain leakage current with the switch off.

I_D, I_S (ON)

Channel leakage current with the switch on.

V_D (Vs)

Analog voltage on Terminals D, S.

C_S (OFF)

Off switch source capacitance.

C_D (OFF)

Off switch drain capacitance.

C_D, C_S (ON)

On switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_D

Off time or on time measured between the 90% points of both switches, when switching from one address state to another (ADG713 only).

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

APPLICATIONS INFORMATION

Figure 20 illustrates a photodetector circuit with programmable gain. An AD820 is used as the output operational amplifier. With the resistor values shown in the circuit, and using different combinations of the switches, gain in the range of 2 to 16 can be achieved.

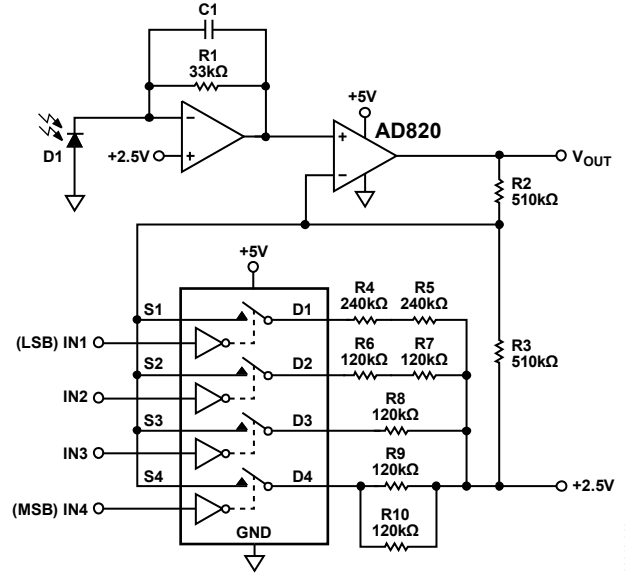
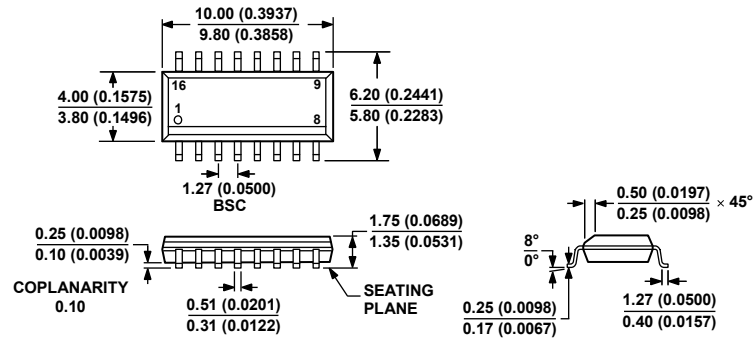


Figure 20. Photodetector Circuit with Programmable Gain

00042-022

OUTLINE DIMENSIONS

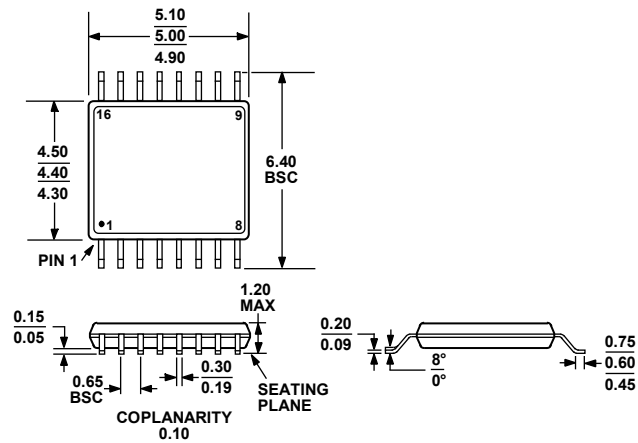


COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 16-Lead Standard Small Outline Package [SOIC]
 Narrow Body
 (R-16)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-16)

Dimensions shown in millimeters

ADG711/ADG712/ADG713

ORDERING GUIDE

| Model ^{1, 2} | Temperature range | Package Description | Package Option |
|-----------------------|-------------------|----------------------------------|----------------|
| ADG711BR | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BR-REEL | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BR-REEL7 | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BRZ | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BRZ-REEL | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BRZ-REEL7 | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG711BRU | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711BRU-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711BRU-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711BRUZ | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711BRUZ-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711BRUZ-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG711WBRUZ-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BR | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BR-REEL | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BR-REEL7 | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BRZ | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BRZ-REEL | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BRZ-REEL7 | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG712BRU | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BRU-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BRU-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BRUZ | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BRUZ-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG712BRUZ-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BR | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG713BRZ | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG713BRZ-REEL | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG713BRZ-REEL7 | -40°C to +85°C | Standard Small Outline(SOIC) | R-16 |
| ADG713BRU | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BRU-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BRU-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BRUZ | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BRUZ-REEL | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |
| ADG713BRUZ-REEL7 | -40°C to +85°C | Thin Shrink Small Outline(TSSOP) | RU-16 |

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD711W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

NOTES

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