



# STB5NK50Z/-1 - STD5NK50Z/-1 STP5NK50Z - STP5NK50ZFP

N-CHANNEL 500V - 1.22Ω - 4.4A TO-220/FP-D/IPAK-D<sup>2</sup>/I<sup>2</sup>PAK  
Zener-Protected SuperMESH™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STB5NK50Z	500 V	< 1.5 Ω	4.4 A	70 W
STB5NK50Z-1	500 V	< 1.5 Ω	4.4 A	70 W
STD5NK50Z	500 V	< 1.5 Ω	4.4 A	70 W
STD5NK50Z-1	500 V	< 1.5 Ω	4.4 A	70 W
STP5K50Z	500 V	< 1.5 Ω	4.4 A	70 W
STP5K50ZFP	500 V	< 1.5 Ω	4.4 A	25 W

- TYPICAL R<sub>DS(on)</sub> = 1.22 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

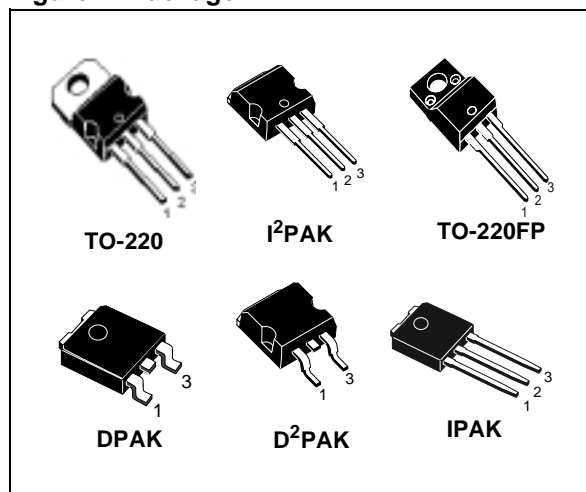
## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

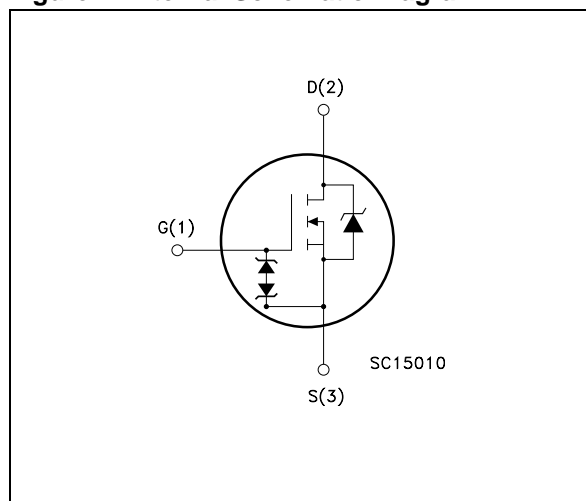
**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB5NK50ZT4	B5NK50Z	D <sup>2</sup> PAK	TAPE & REEL
STB5NK50Z-1	B5NK50Z	I <sup>2</sup> PAK	TUBE
STD5NK50ZT4	D5NK50Z	DPAK	TAPE & REEL
STD5NK50Z-1	D5NK50Z	IPAK	TUBE
STP5NK50Z	P5NK50Z	TO-220	TUBE
STP5NK50ZFP	P5NK50ZFP	TO-220FP	TUBE

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



Rev. 2

## STB5NK50Z/-1 - STD5NK50Z/-1 - STP5NK50Z - STP5NK50ZFP

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value			Unit
		STP5NK50Z STB5NK50Z/-1	STP5NK50ZFP	STD5NK50Z STD5NK50Z-1	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500			V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500			V
V <sub>GS</sub>	Gate- source Voltage	± 30			V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	4.4	4.4 (*)	4.4	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	2.7	2.7 (*)	2.7	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	17.6	17.6 (*)	17.6	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	70	25	70	W
	Derating Factor	0.56	0.2	0.56	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	-	V
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150			°C °C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 4.4A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

**Table 4: Thermal Data**

		TO-220 I <sup>2</sup> PAK/D <sup>2</sup> PAK	TO-220FP	DPAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.78	5	1.78	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5			°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300			°C

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	4.4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	130	mJ

**Table 6: Gate-Source Zener Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>GS</sub> =± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}\text{C}$  UNLESS OTHERWISE SPECIFIED)

**Table 7: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 50 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 2.2 \text{ A}$		1.22	1.5	$\Omega$

**Table 8: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 2.2 \text{ A}$		3.1		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		535 75 17		pF pF pF
$C_{OSS \text{ eq}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 0 \text{ to } 400 \text{ V}$		45		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 250 \text{ V}$ , $I_D = 2.2 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 19)		15 10 32 15		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 \text{ V}$ , $I_D = 4.4 \text{ A}$ , $V_{GS} = 10 \text{ V}$ (see Figure 22)		20 4 10	28	nC nC nC

**Table 9: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				4.4 17.6	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 4.4 \text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4.4 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30\text{V}$ , $T_j = 150^{\circ}\text{C}$ (see Figure 20)		310 1425 9.2		ns nC A

(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3)  $C_{OSS \text{ eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Figure 3: Safe Operating Area For DPAK/IPAK/  
D<sup>2</sup>PAK/I<sup>2</sup>PAK/TO-220

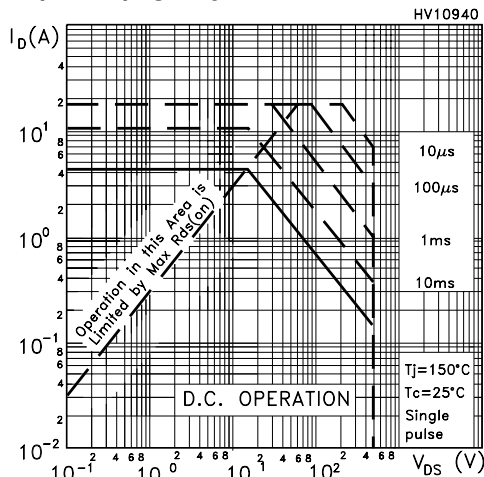


Figure 4: Thermal Impedance For DPAK/IPAK/  
D<sup>2</sup>PAK/I<sup>2</sup>PAK/TO-220

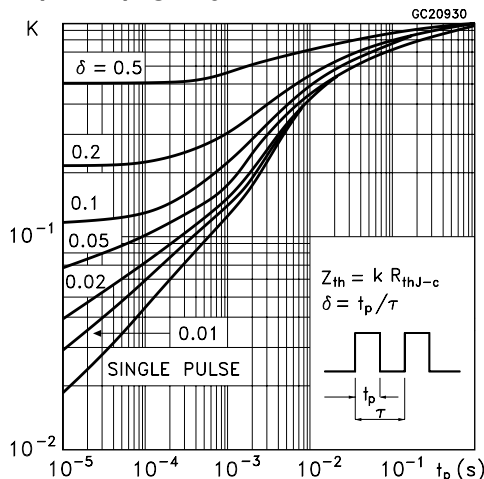


Figure 5: Output Characteristics

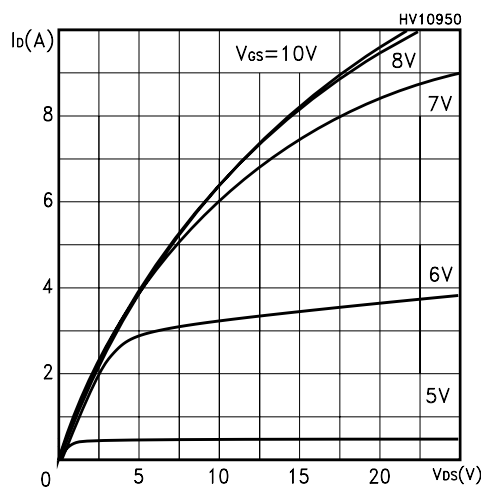


Figure 6: Safe Operating Area For TO-220FP

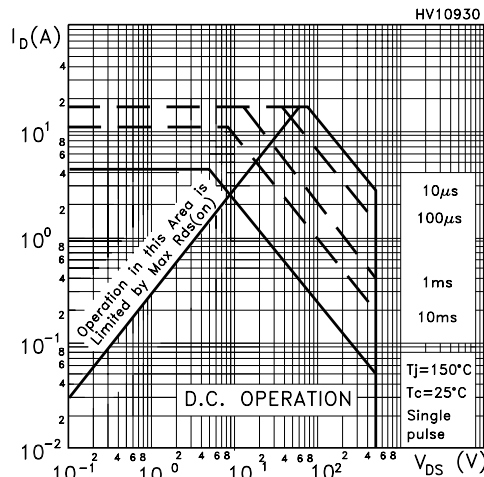


Figure 7: Thermal Impedance For TO-220FP

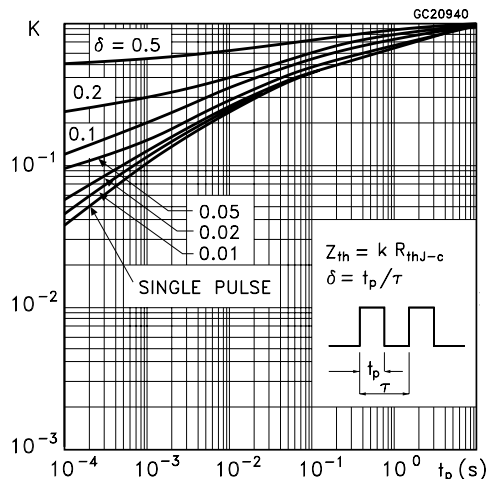


Figure 8: Transfer Characteristics

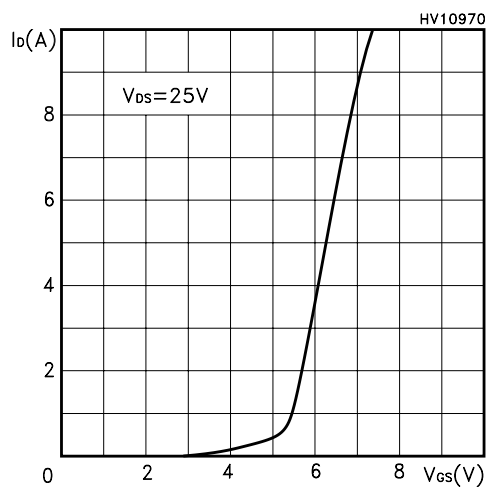


Figure 9: Transconductance

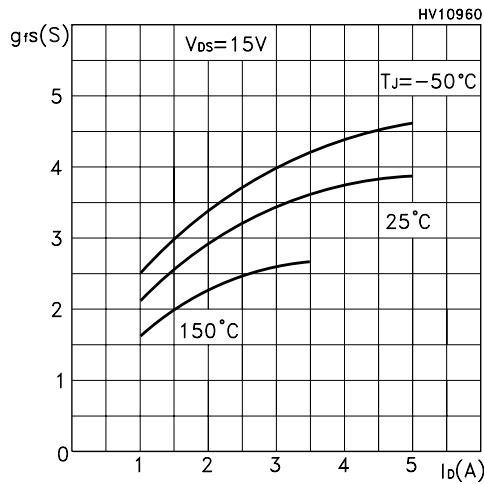


Figure 10: Gate Charge vs Gate-source Voltage

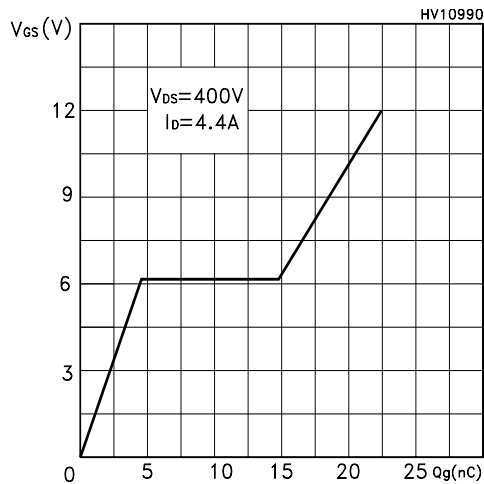


Figure 11: Normalized Gate Threshold Voltage vs Temperature

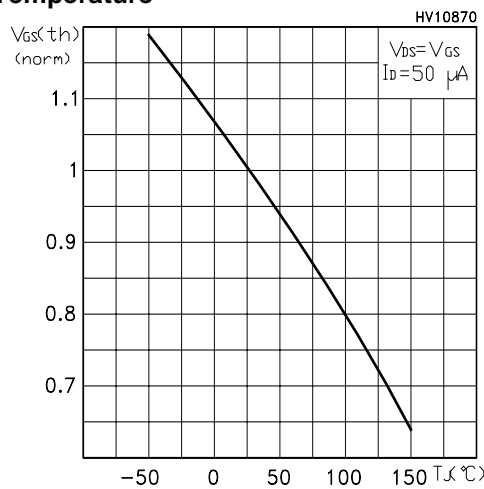


Figure 12: Static Drain-Source On Resistance

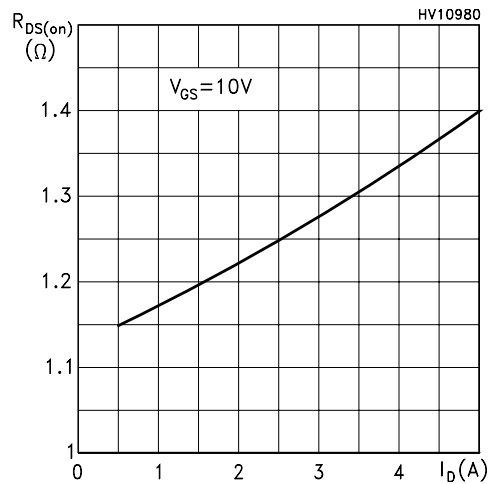


Figure 13: Capacitance Variations

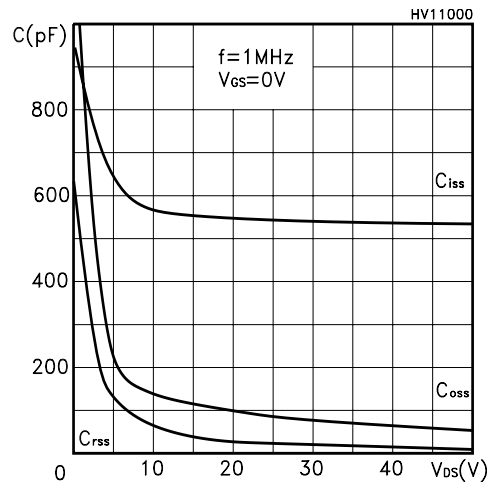


Figure 14: Normalized On Resistance vs Temperature

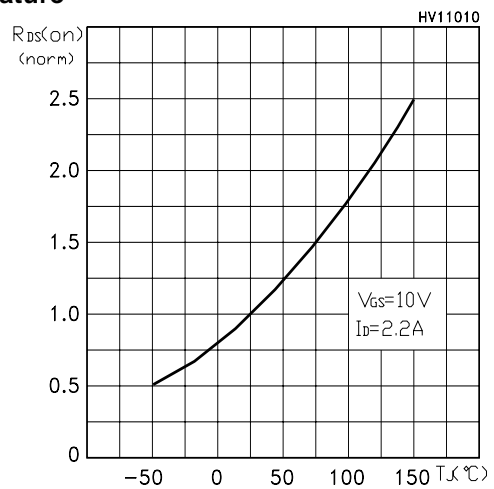


Figure 15: Source-Drain Forward Characteristics

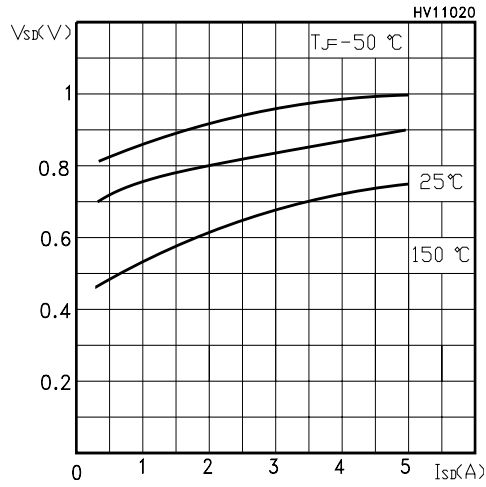


Figure 16: Maximum Avalanche Energy vs Temperature

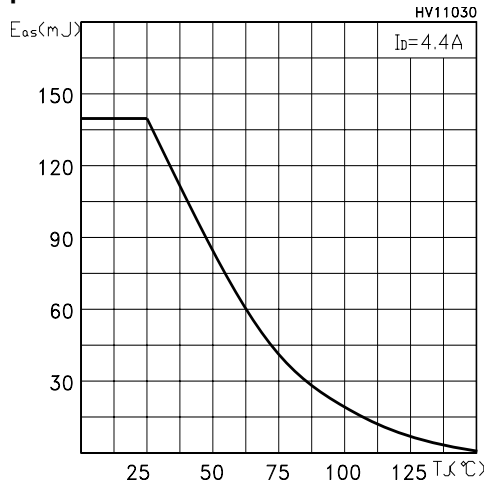


Figure 17: Normalized  $BV_{DSS}$  vs Temperature

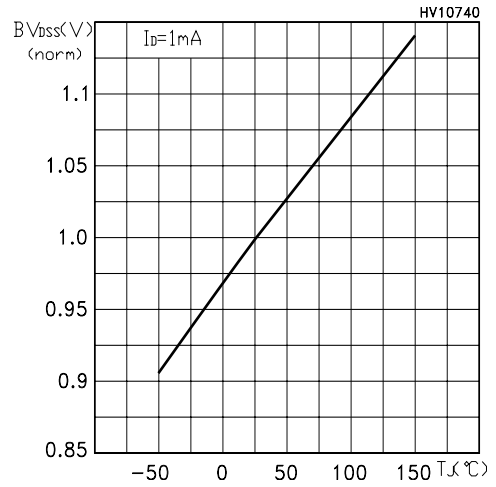


Figure 18: Unclamped Inductive Load Test Circuit

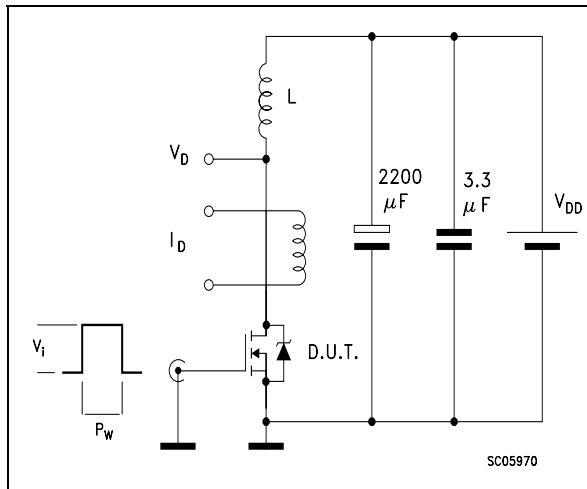


Figure 19: Switching Times Test Circuit For Resistive Load

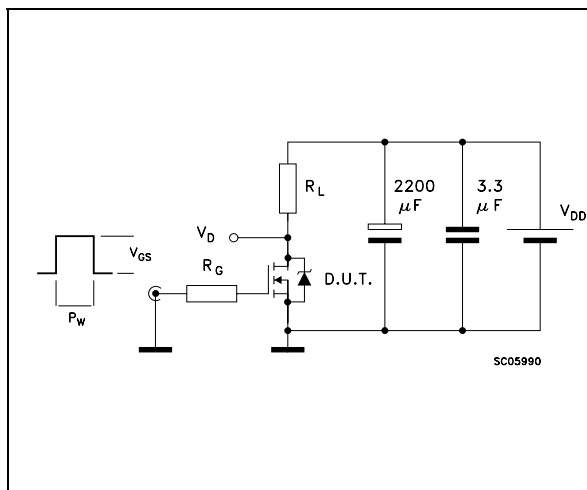


Figure 20: Test Circuit For Inductive Load Switching and Diode Recovery Times

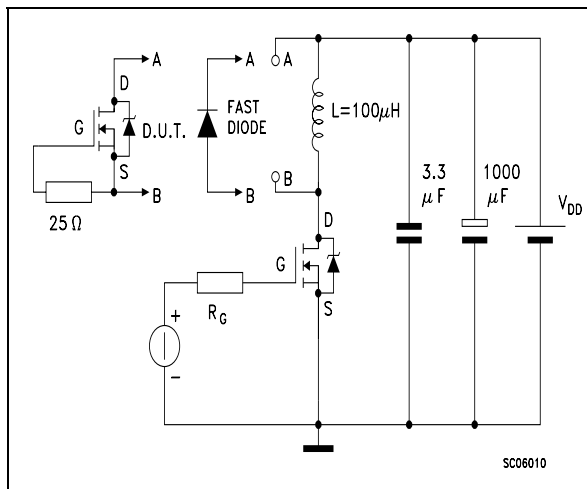


Figure 21: Unclamped Inductive Wafeform

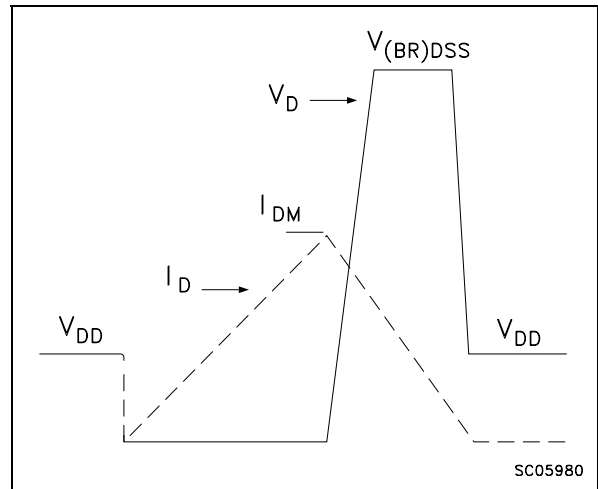
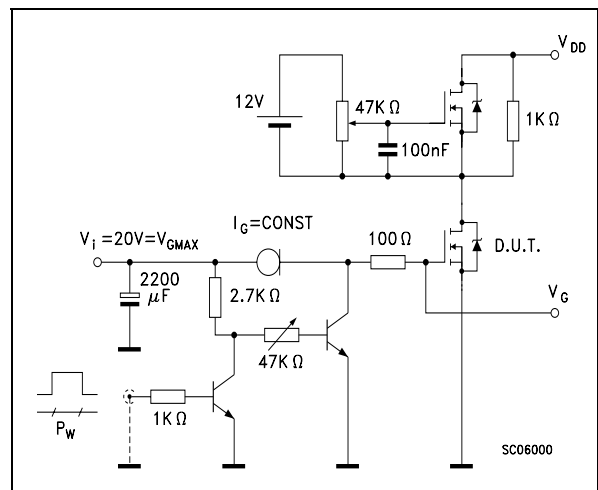


Figure 22: Gate Charge Test Circuit



## **STB5NK50Z/-1 - STD5NK50Z/-1 - STP5NK50Z - STP5NK50ZFP**

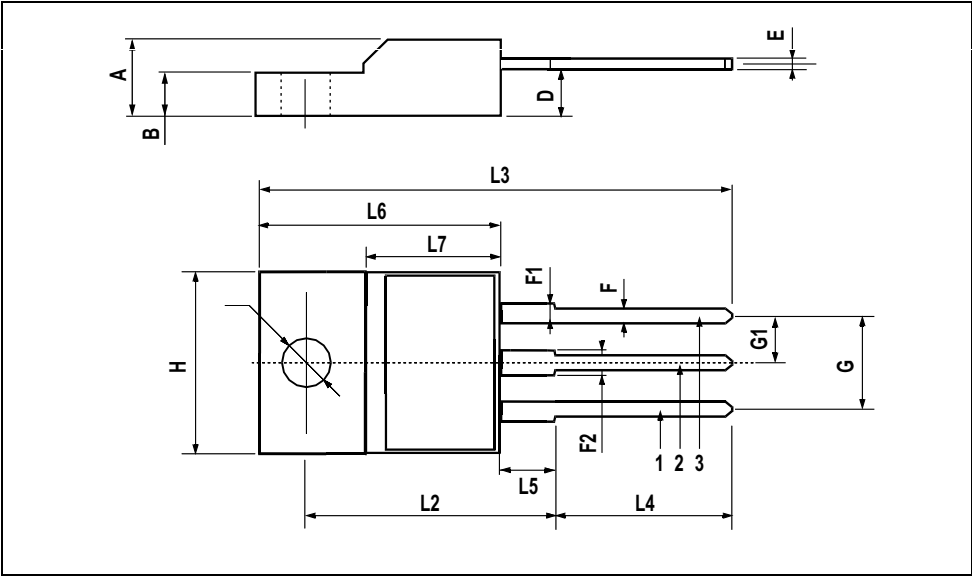
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In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



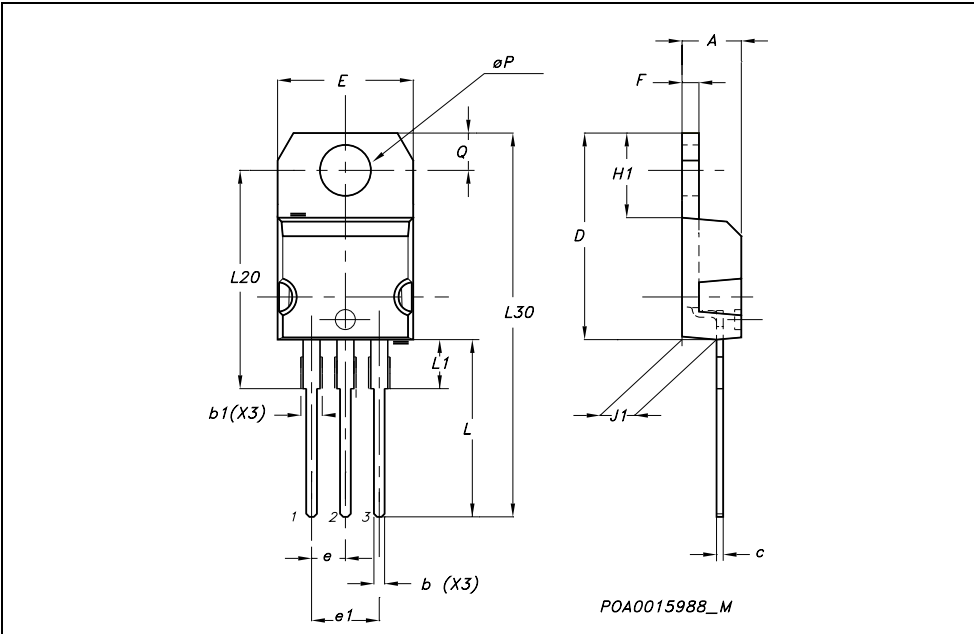
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



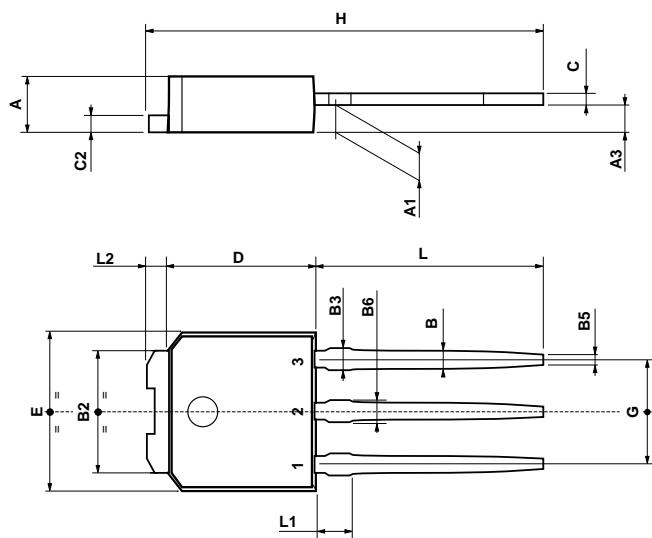
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## TO-251 (IPAK) MECHANICAL DATA

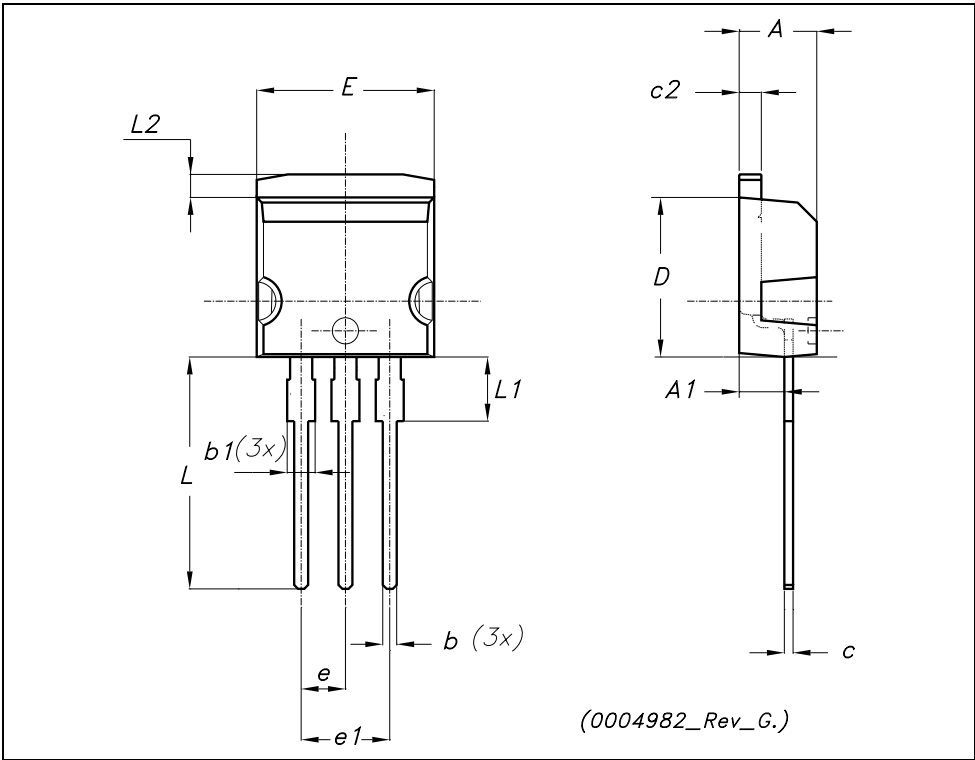
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



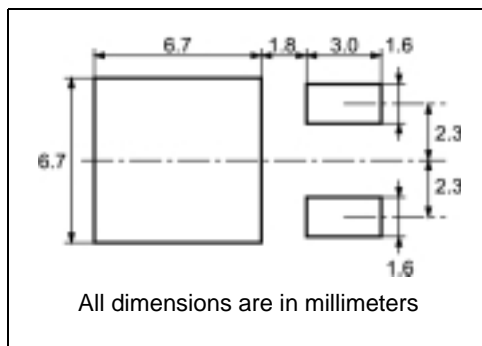
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TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA

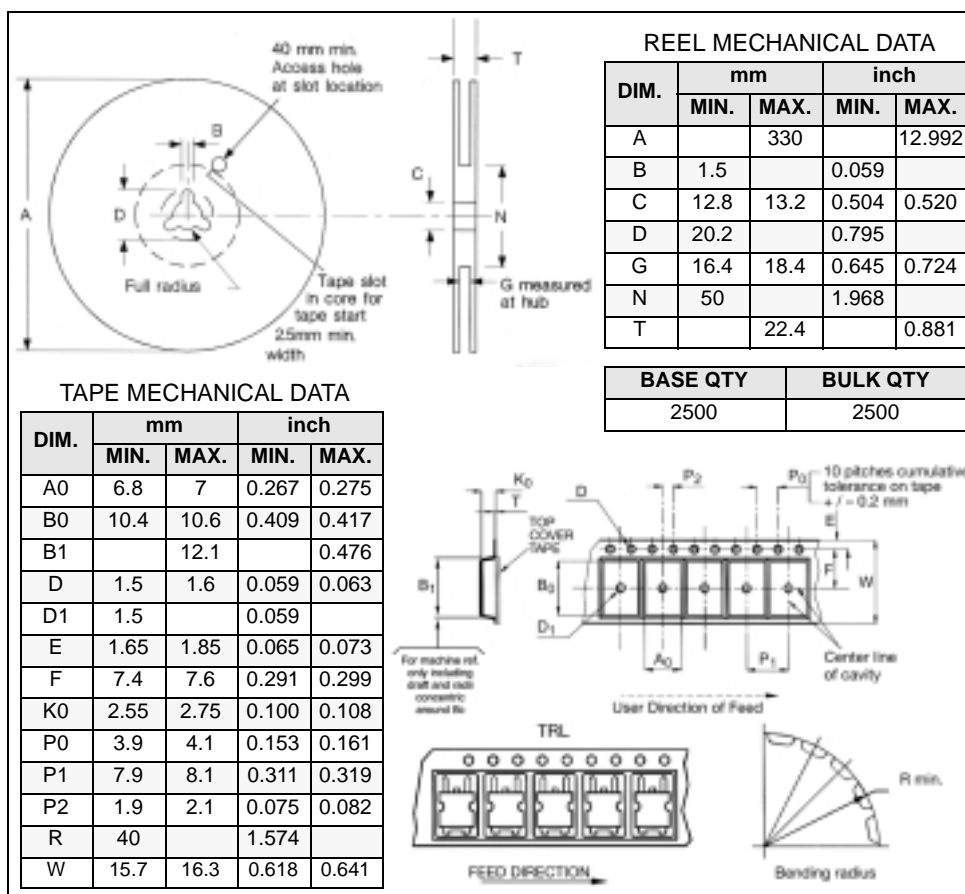
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



## DPAK FOOTPRINT

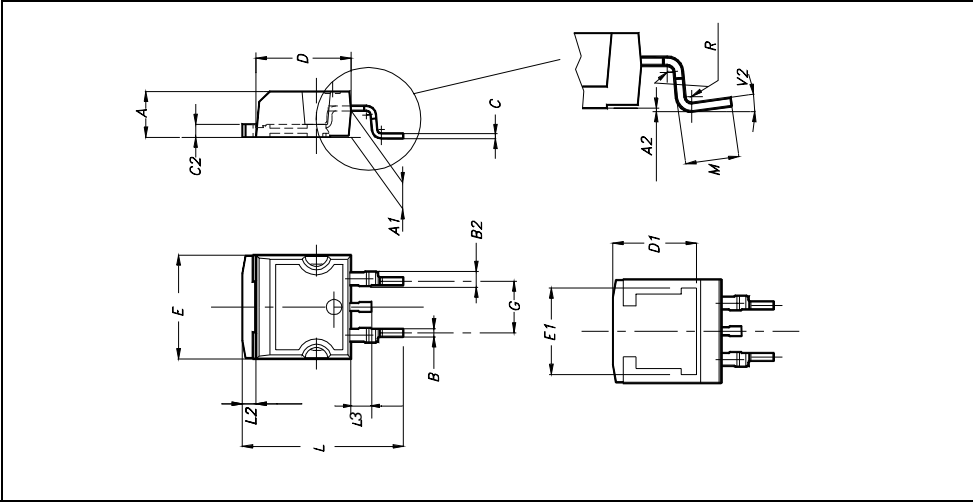


## TAPE AND REEL SHIPMENT



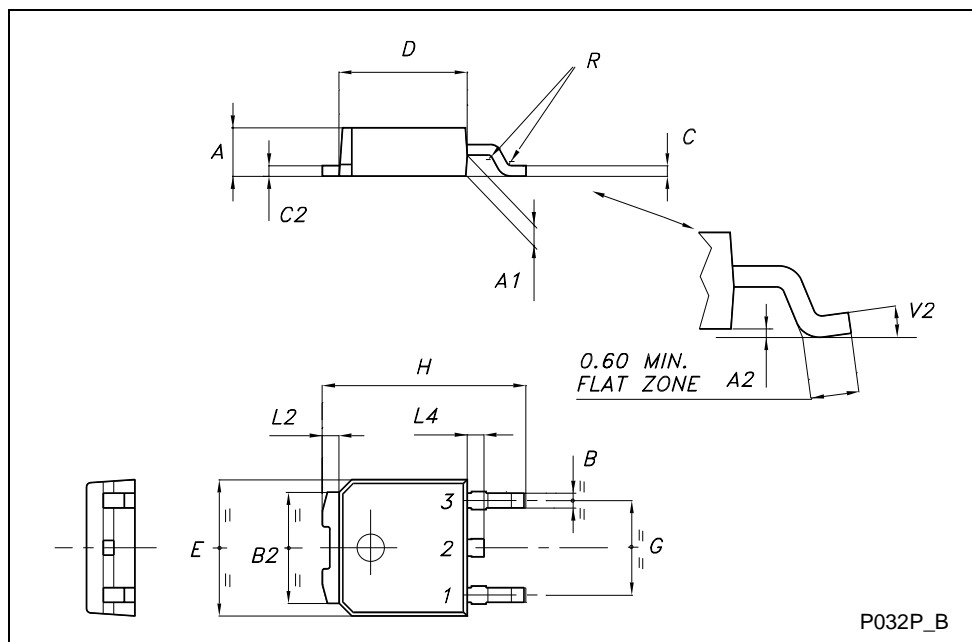
D<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



## STB5NK50Z/-1 - STD5NK50Z/-1 - STP5NK50Z - STP5NK50ZFP

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**Table 10: Revision History**

Date	Revision	Description of Changes
16-Jun-2004	1	D <sup>2</sup> PAK Included. New Stylesheet.
06-Sep-2005	2	Inserted Ecopack indication



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