5 Output PMIC Controller/ IRPS5401

User guide with DB295 and DB296 demo boards

About this document

Scope and purpose

Note: The following information is given as a description of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This application note is intended to provide a description of the operation of IRPS5401 and the performance of the DB295 (orderable as EVAL_PS5401-25 or EVAL_PS5401-40) and DB296 (orderable as EVAL_PS5401-INT) demo boards.

It is assumed that the user is already familiar with the datasheet and functions of the IRPS5401 device.

Intended audience

FAEs and customer engineers

Table of contents

1 Introduction

This document will describe the operation of the IRPS5401 PMIC. This document will also cover the details of the DB295 (available as EVAL_PS5401-25 for 25A power stage and EVAL_PS5401-40 for 40A power stage) and DB296 (available as EVAL_PS5401-INT) IRPS5401 demo boards. IRPS5401 is a 56 pin, 7x7 mm PMIC. It has 4 switching outputs and 1 LDO output. SW-A and SW-B have a max rated current of 2 A. SW-A can be configured to drive an external power-stage. SW-C and SW-D have a max rating of 4 A. The LDO has a max rating of 0.5 A and can be configured as source only mode or sink-source (tracking) mode.

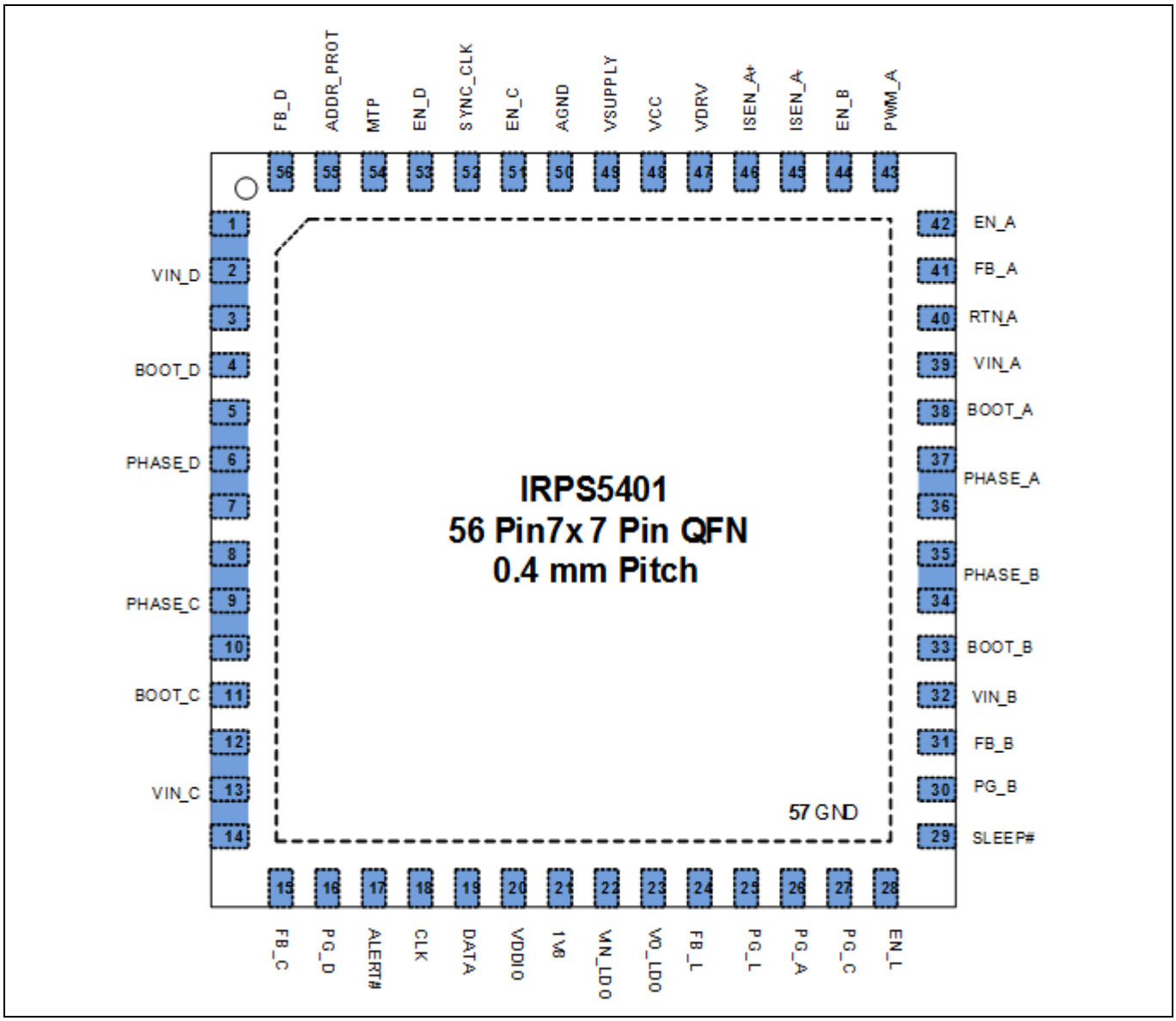


Figure 1 Pinout diagram

For more information see:

- IRPS5401; Data Sheet
- UN0049; Description of PMBus commands in IRPS5401
- UN0065; List of and functional description of I2C Registers (Customer RegMap)
- TB0035; Programming Guide for IRPS5401

2 I2C ADDRESS, PMBUS address, and address offset

The IRPS5401 has 2 addresses; an I2C address for direct register read write access and a PMBus address for sending PMBus commands. With the IRPS5401 powered up and the GUI communicating with the USB dongle (1), you should be able to hit the Auto-populate button (2) and have the GUI recognize and populate the IRPS5401 information (3). You can also use the address scan feature (4) to scan all addresses and see what responds (5).

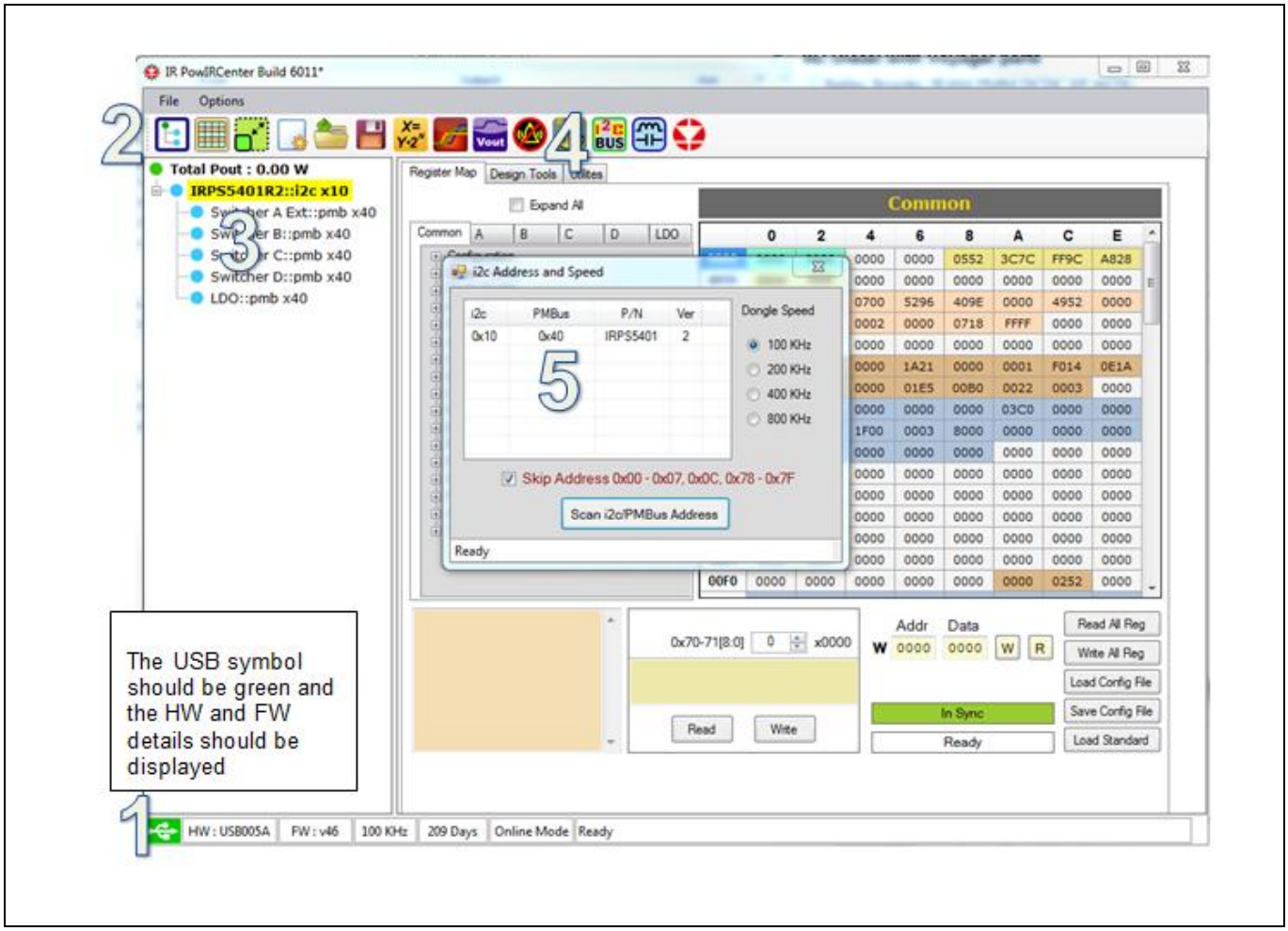


Figure 2 Example figure

The base I2C and PMBus addresses are located in register 0x0020. The PMBus address bits are [6:0] and the I2C address bits are [14:8]. Before these addresses can be updated, the register must be unlocked by setting REG 0x0086 bit [2] to 0. The PAGE command is used so that 1 common PMBus address can be used to access all 5 outputs.

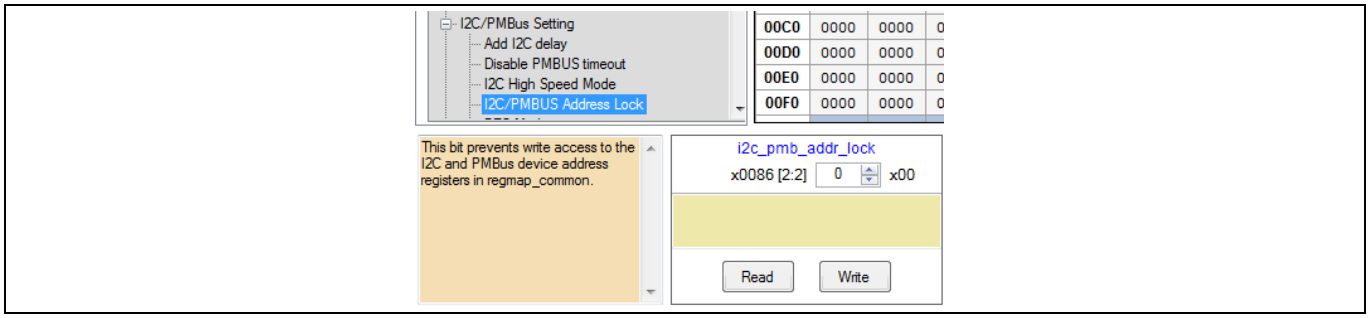


Figure 3 Lock register

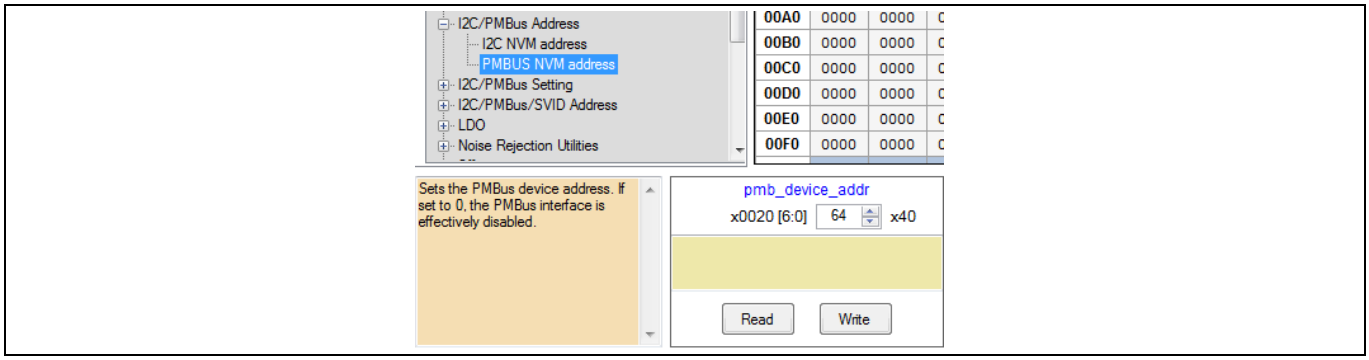


Figure 4 PMBus address

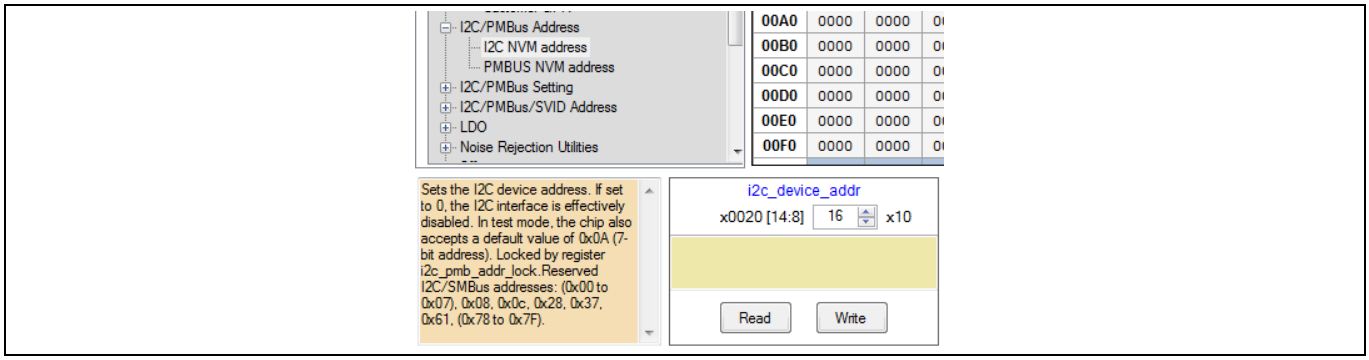


Figure 5 I2C address

After the addresses have been updated in REG 0x0020, you will need to right click on the device (1) to bring up the address editor dialog box (2) to update the addresses (3) that the GUI must use to communicate with the IRPS5401 to the new values that where placed in REG 0x0020.

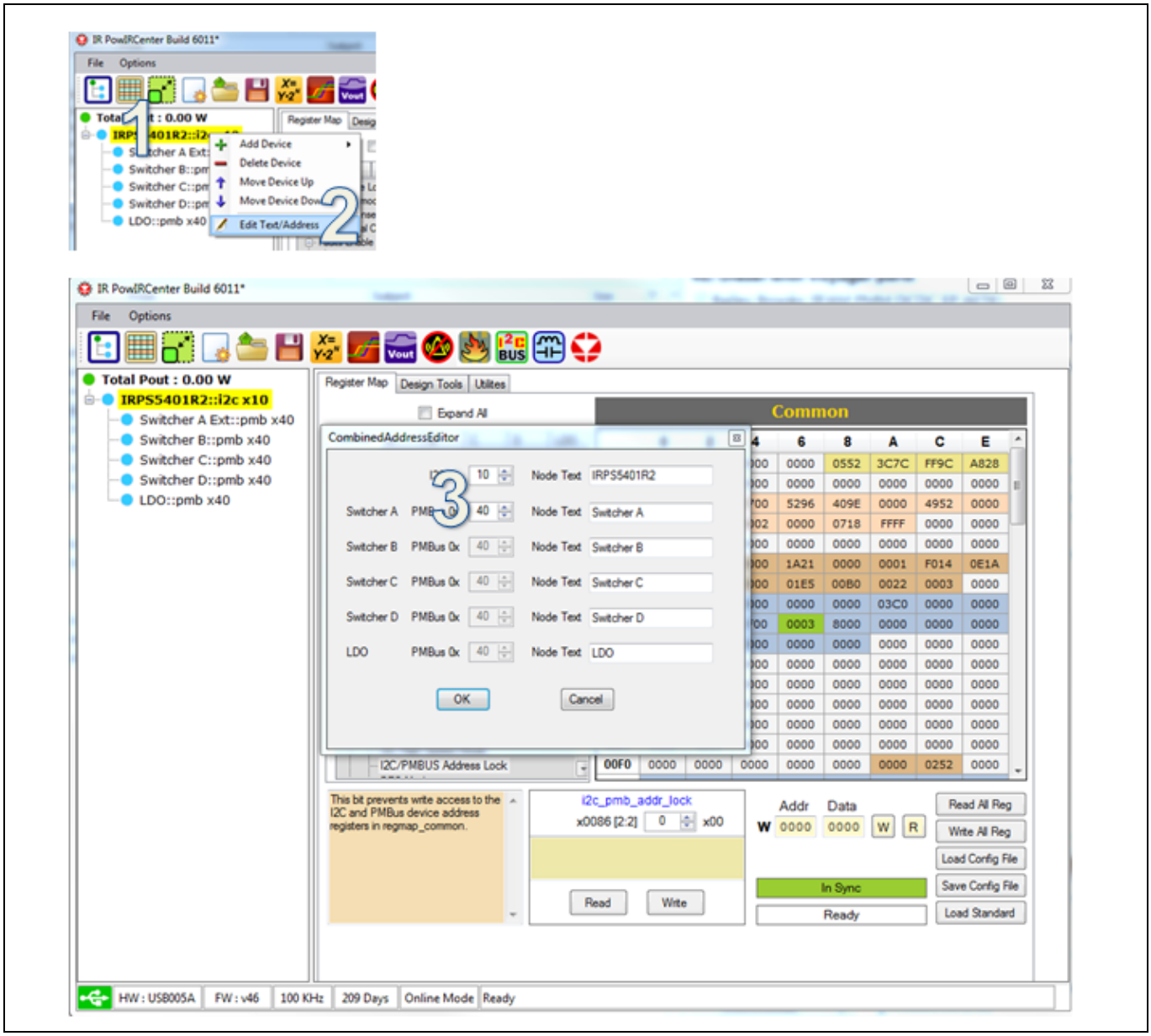


Figure 6 Example figure

2.1 ADDR_PROT Pin

The base I2C and PMBus address that is placed in NVM can be offset by up to fifteen (15) so that up to sixteen (16) IRPS5401 devices with a common NVM address can be placed on a common I2C/PMBus. This feature is activated by setting 0x0028 bit [2], i2c_take_addr_from_ext, to 1. The part will ship from the factory with this bit set to 1.

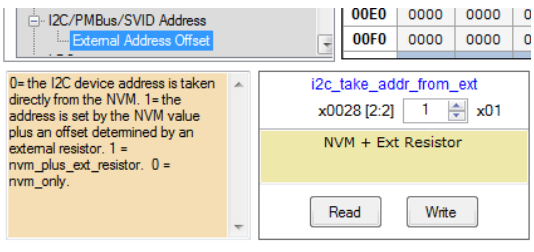


Figure 7 NVM address

With this bit set to 1, the device address will be the NVM address (in REG 0x0020) plus the offset added by the resistor value attached to ADDR_PROT (pin 55).

The resistor must be connected from ADDR_PROT to AGND (pin 50). The resistor must be decoupled with a 10 nF capacitor (X7R type). The IRPS5401 will source 100 µA through the offset resistor for 1 ms immediately after POR, the ADC will measure the voltage drop on the resistor and the value will be latched into the digital core. This happens one time at start up, so updating this resistor after POR will not affect the offset.

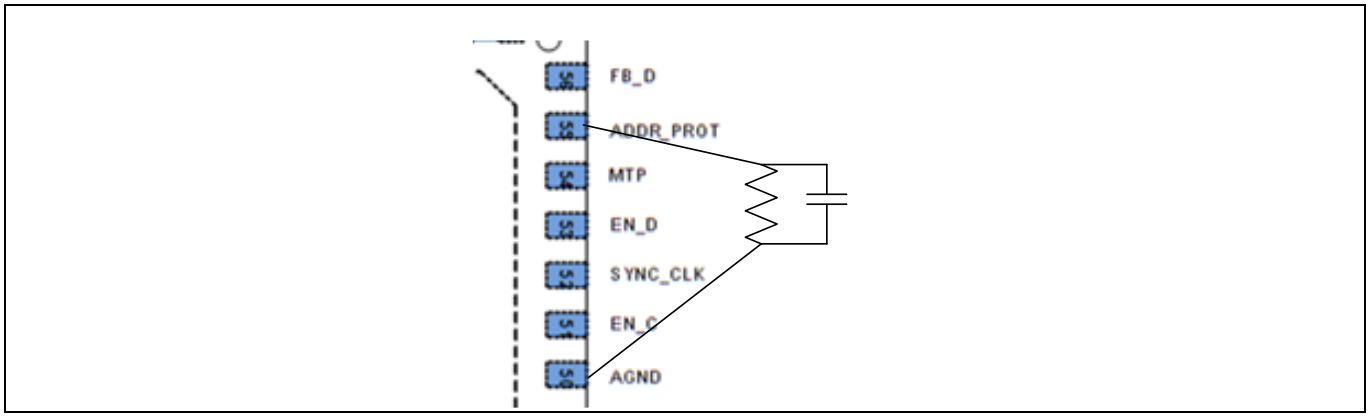


Figure 8 Setting the resistor

This table shows the offset given for a specific resistor value. The I2C and PMBus address will be offset by the same value.

**NOTE: the address can't be offset above 7Fh. So, for instance, if you set the base address in NVM to 77h, the largest offset resistor you can use is 5.49 K, +8 offset.

**NOTE: setting the PMBus address to 0 in NVM will disable PMBus

**NOTE: setting the I2C address to 0 in NVM will disable I2C communication

**NOTE: do not set the NVM (or NVM + offset) to these addresses; 01h to 07h, 0Ah or 0x0Ch

The IRPS5401 will be shipped from the factory with the I2C address defaulted to 10h and the PMBus address defaulted to 40h. The address offset feature will be enabled. In order to see/use the address in NVM, you will need to populate an 845 Ω resistor on pin 55. Do not leave pin 55 floating. Do not short pin 55 to GND. The LSADC does not like trying to sense 0 V

Table 1 Address offset table

ADDR_PROT Resistor	Address Offset
0.845 kΩ	+0
1.30 kΩ	+1
1.78 kΩ	+2
2.32 kΩ	+3
2.87 kΩ	+4
3.48 kΩ	+5
4.12 kΩ	+6
4.75 kΩ	+7
5.49 kΩ	+8
6.19 kΩ	+9
6.98 kΩ	+10
7.87 kΩ	+11
8.87 kΩ	+12
10.00 kΩ	+13
11.00 kΩ	+14
12.10 kΩ	+15

2.2 TEST ADDRESS 0Ah

If the MTP pin (pin 54) is connected to VCC (or any voltage greater than 3.3 V) during POR, NVM will not load into the working registers and the I2C address will be set to 0Ah regardless of the value in REG 0x0020 and the address offset. This would be useful if you had 2 or more devices on the same bus that were responding to the same address. You would be able to communicate with any individual device at address 0Ah by forcing the MTP pin of that device high during POR.

3 LDO Operation

The LDO input is pin 22. The input voltage has a range of 1.2 V to 5.5 V. The LDO output is pin 23.

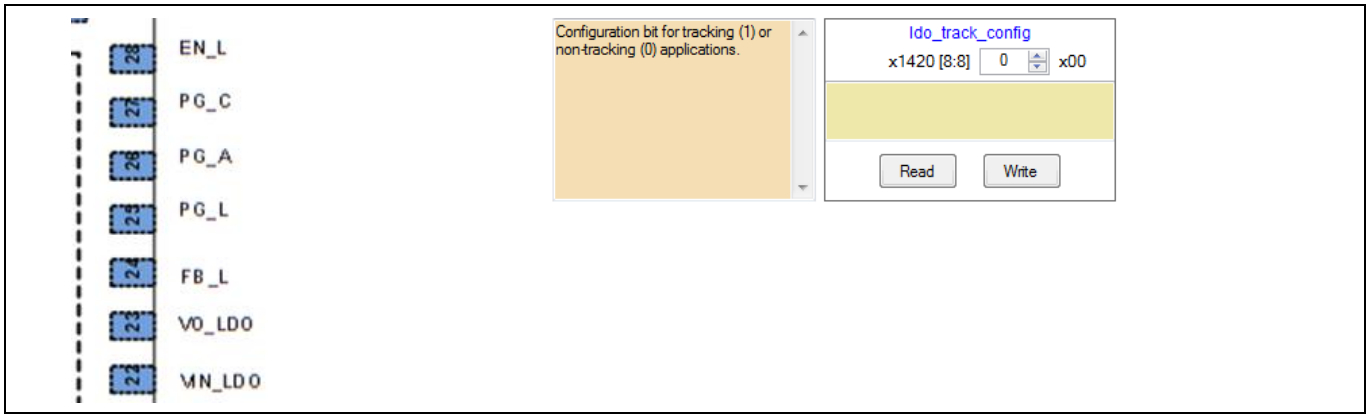


Figure 9 LDO input

3.1 Source only mode

Set REG 0x1420 bit [8] (ldo_track_config) to 0

The LDO output has a range of 0.5 V to 3.6 V. The output is fed back to pin FB_L through a resistor divider network. The output voltage will be set to (1+R_upper/R_lower)*0.5 V. With VOUT tied directly to FB_L, VOUT will be set to 0.5 V…the reference voltage. The output is rated at 0.5 A. The OC_FAULT_LIMIT is read only and is set to 0.72 A. The OV_WARN and FAULT, UV_WARN and FAULT are all read only and are a percentage of the VOUT value set in REG 0x1420 [7:0] (ldo_target_vout). The lsb is 15.625 mV. So a value of 40h (1000/15.625 = 64 dec = 40h) would represent 1 V. Set this register to accurately represent the actual VOUT set by the external components so that the UV and O V circuits trip at the correct value.

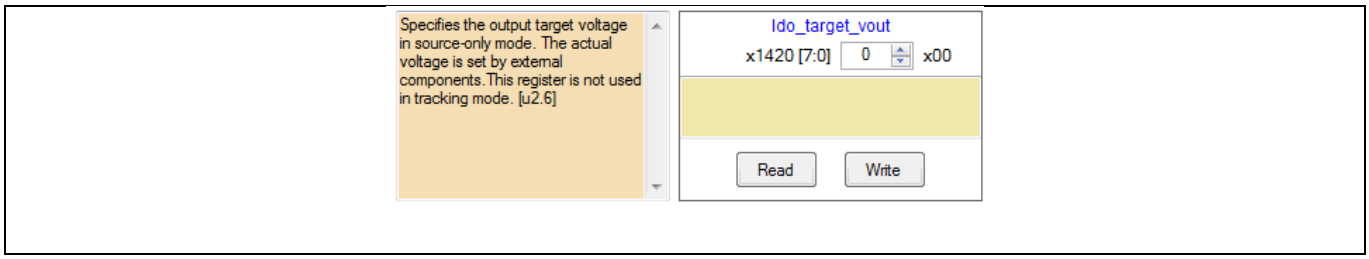


Figure 10 Source only mode

3.2 Sink/Source (Tracking) mode

Set REG 0x1420 bit [8] (ldo_track_config) to 1

In Tracking mode, VO_LDO must be connected directly to FB_L. An internal divider to VIN_LDO sets the reference. The target VOUT is always ½*VIN_LDO so register ldo_target_vout has no function in tracking mode. PMBus commands POWER_GOOD_ON and OFF also have no function in tracking mode. They are a percentage of ½*VIN_LDO.

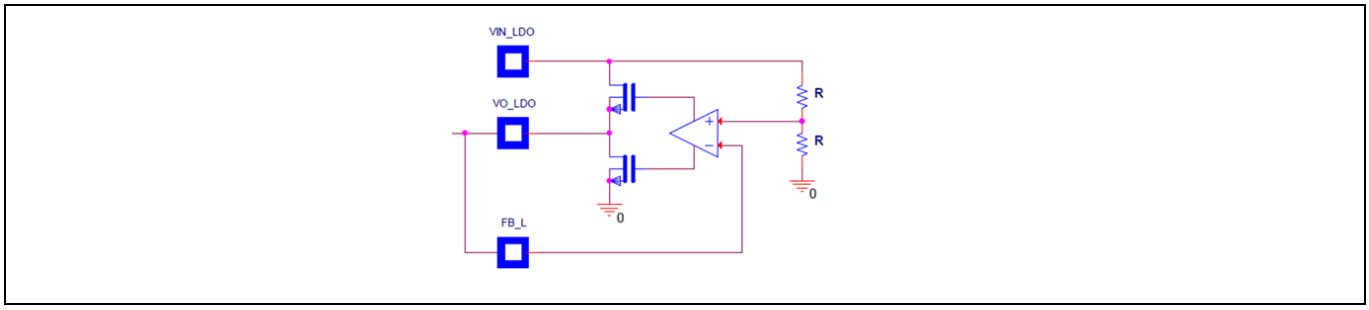


Figure 11 Tracking mode

3.3 Fault settings

All PMBus OV and UV CMD's are READ ONLY for the LDO. A read command will report back the percentage of VOUT shown in the table below. POWER_GOOD_ON and OFF is a read only command in tracking mode.

Table 2 Address offset table

MODE	Source Only	Tracking
Parameter	% of ldo_target_vout	% of ½*VIN_LDO
UV_FAULT	75	75
UV_WARN	87.5	87.5
OV_WARN	112.5	112.5
OV_FAULT	125	125
PG_ON	POWER_GOOD_ON	87.5
PG_OFF	POWER_GOOD_OFF	81.25

4 Switcher Operation

The IRPS5401 consists of 4 internal switching regulators (Switchers). SW-A and B are 2 A regulators. SW-C and D are 4A regulators. SW-A can be configured to drive an external power stage such as the TDA21240 PowerStage or a discrete FET driver with power FET. This output can be designed to deliver up to 50 A. The DB295 is configured such that SW-A is driving an external TDA21240 PowerStage.

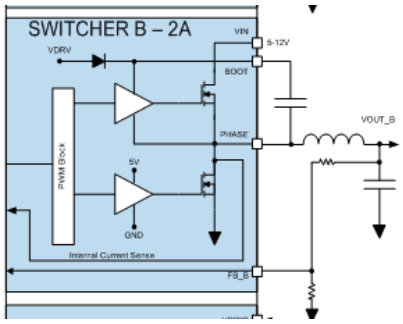


Figure 12 Internal switching regulators

One of the most important considerations for the layout is the path length and loop area for the current path from the input capacitors to the FET switches. C85 in the figure to the left is a 1 µF, 0402 multi-layer ceramic capacitor (MLCC). It is one of the VIN decoupling caps for SW-D. It is placed adjacent to the VIN pins for SW-D and is returned to GND through a via. On the bottom of the PCB, C70 and C71 are 10 µF MLCC caps that provide additional decoupling for SW-D. They are arranged at 45° to provide the shortest path length to the GND RTN vias under the IC.

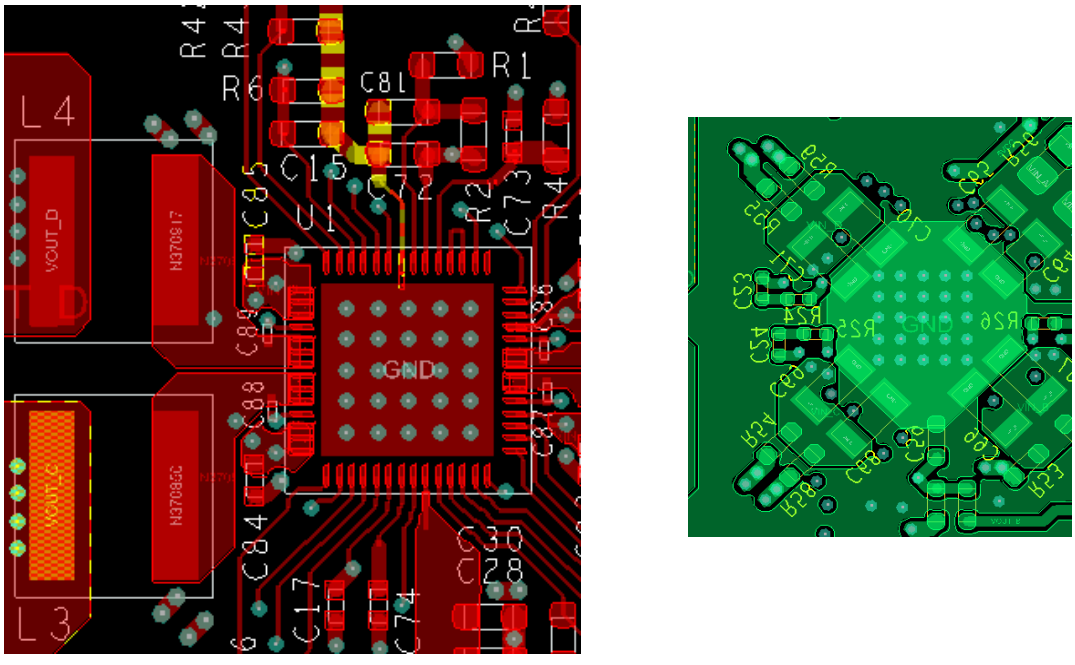


Figure 13 Layout details

Other important considerations are:

- The length and width of the copper connecting the SW Nodes to the inductors. They must be as short as possible and as wide as possible, and be located only on the top layer

- The 5x5 via pattern under the IRPS5401; these help transfer heat from the IC to the copper GND planes on the PCB
- Decouple VCC, MTP, and ADDR_PROT pins directly to AGND (pin 50) and tie AGND to GND with a single point connection (see arrow above)
- SW-A in external mode requires ISENSE and VSENSE lines to be routed back to the IC as differential pairs

4.1 Setting the Switching Frequency

The phase angle between all switchers is maintained at a constant value. SW-A is at 0°, SW-C is at 90°, SW-B is at 180° and SW-D is at 270°. A and B are 180° out of phase and C and D are 180° out of phase. In order to accomplish this, all Switchers must operate at the same switching frequency (fsw). To that end, the fsw for all switchers is controlled by the FREQUENCY_SWITCH PMBus command for SW-C.
SW-C will ACK any FREQUENCY_SWITCH command from 200 kHz to 2 MHz in increments of 1 kHz. Internally the command is decoded and the actual FSW is set to the nearest value that can be supported with the 48 MHz internal clock. For example, 500 kHz can be supported with ninety-six (96) 48 MHz clocks. So if you ask for 500 kHz, you get exactly 500 kHz. But if you wanted 450 kHz, the number of clocks required is 106.6667 (48/0.45). In this case, the frequency would be set to one hundred and seven (107) 48 MHz clocks or 448.6 kHz. Fractional values of 0.5 and above are rounded up to the next whole number.
FREQUENCY_SWITCH write commands to SW-A, B, and D will be ACK'd and ignored. FREQUENCY_SWITCH read commands sent to SW-A, B, and D will read back the value sent in the ignored command.

SW-A FREQUENCY

The user can set the FSW of SW-A to be ½ of SW-C by sending a FREQUENCY_SWITCH command to SW-A that is less than the FSW of SW-C. It does not have to be the value that is ½ of SW-C. Any FSW smaller than SW-C FSW will result in SW-A FSW being set to ½ of SW-C. This 'special' ½ FSW ability only applies to SW-A. Setting FSW for SW-A to ½ FSW of SW-C is usually done when SW-A is used in EXT driver mode.
FSW for SW-B and D will always be the same as SW-C
If the FSW of SW-C is less than 400 kHz, the FSW for SW-A will be the same as SW-C regardless of the FSW setting of SW-A. The FSW of SW-A can't be less than 200 kHz

SUMMARY

The FSW for all 4 switching regulators is controlled by SW-C. The FSW for SW-A may be set to ½ of SW-C
Because SW-C is the master, FREQUENCY_SWITCH 'read' commands to SW-A, B and D may not reflect the actual FSW values for these outputs.

4.2 AOT Mode

Adaptive on-time (AOT) is a means of saving power at low output currents by reducing the switching frequency and shutting off the LS FET before the inductor current goes negative. AOT mode is enabled by sending a MFR specific PMBus command. Sending command D9h with a value 00h will enable AOT mode. AOT is sometimes called discontinuous current mode (DCM) because the inductor current will go to 0 A.

In the GUI, select command D9h (MFR_FCCM), 'Adaptive on-time', then hit 'write' to switch between FCCM (forced continuous conduction mode) and AOT. In AOT mode the switching frequency is a function of the load so the enforced phase angle between outputs does not apply. As the load increases, the FSW will increase. When the load is large enough to cause the FSW to be the same as the FSW set in FCCM, the switcher will automatically switch to FCCM.

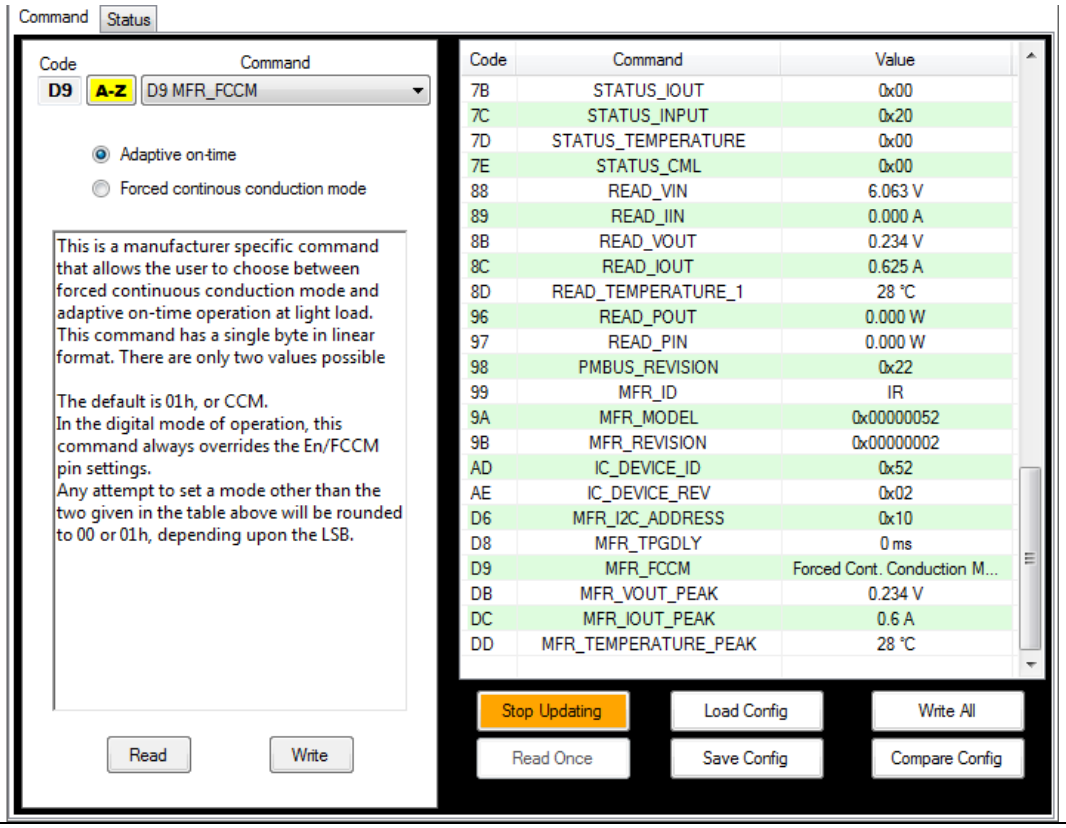


Figure 14 AOT mode

There are 4 configuration registers for each switcher that need to be set so that AOT mode operates correctly.

Diode_emu_threshold is the threshold below the DAC voltage that will cause the AOT pulse to start. This is usually set to 1 ➔ 3 mV:

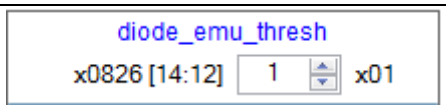


Figure 15 Diode_emu_threshold

diode_emu_pw is the time that the HS FET is on after AOT is activated. It is usually set to 1. The on-time will be a function of VIN. 1 = 180 ns at 12 V and 230 ns at 8 V:

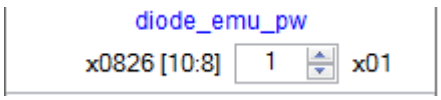


Figure 16 Diode_emu_pw

inductor_ni_thresh is the threshold that IOUT must be below before the output will try to enter into AOT mode. If this is set to 0, the VR will never enter AOT mode even with the PMBUS command. 8 is a 0.25 A limit:

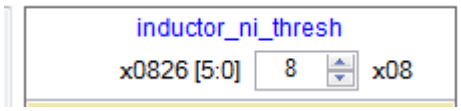


Figure 17 Inductor_ni_thresh

de_off_time_adj is an adjustment to the calculated LS FET on time. This prevents the inductor current from going negative due to delays from the driver entering tri-state. Usually set to 6 ➔ 400 nsec.

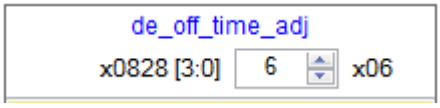


Figure 18 De_off_time_adj

****NOTE: IOUT reporting during AOT is not accurate. Do not send READ_IOUT commands while in AOT Mode**

4.3 External Sync

The IRPS5401 has a sync input (pin 52) that can be used to set the FSW to an external clock. The threshold levels are LVTTL, 0.8V max for low and 2.1V min for high. The FSW setting for the IRPS5401 must be within a +/- 6.5% window of the desired sync frequency. The Sync input signal should be a 3.3V square wave with a 50% duty cycle (+/- 10%)

** NOTE: Using external sync will cause a ~40 nsec 'jitter' on the SW_NODE when compared to no sync input but it is not reflected in the VOUT ripple. See comparison below

Figure 19 TOP→SYNC in, MIDDLE→SW_NODE, BOTTOM→RIPPLE

Figure 20 MIDDLE→SW_NODE, BOTTOM→RIPPLE

4.4 Current Sense and Over Current Settings

The 4 internal switchers sense IOUT by sensing the drop across the Rdson of the LS FET in the middle of the LS FET conduction time. This gives the cleanest (least noisy) measurement because the SW_NODE has had time to settle and stop ringing. Because the current is sensed in the middle of the LS FET on time (also the middle of the inductor current down slope), the IRPS5401 senses the average output current, not the peak inductor current.

The setting of the OC_WARN_LIMIT and OC_FAULT_LIMIT can be set to the DC value the user wants to see and does not have to account for any added peak inductor current.

The OC_WARN_LIMIT is based on the output of the ADC and is filtered to 72 kHz. This digital current sense is trimmed at ATE test to have a gain error of less than 5% and an offset error of less than 1% of the full load capability.

The OC_FAULT_LIMIT is based on the output of a comparator that is looking directly at the Rdson. To ensure OC_FAULT_LIMIT accuracy, the comparator is trimmed during ATE Test to tolerances of +/-10% at 3 A for the 2 A outputs and +/-10% at 6 A for the 4 A outputs.

The PMBus commands OC_WARN_LIMIT and OC_FAULT_LIMIT have a range of 0 A to 15.97 A in increments of 31.25 mA. This means that the user can send a command and the IRPS5401 will ACK the command as valid. However, the OC_FAULT_LIMIT is actually based on the comparator input which can only be set from 0 A to 4 A in 0.25 A increments for the 2 A output and from 0 A to 8 A in 0.5 A increments for the 4 A outputs. (0 A to 16 A for the combined C+D output) The internal logic will take the user's commanded value and round it up to the next real comparator setting. The OC_WARN_LIMIT is based on the ADC output so it really has 31.25 mA increments. But it doesn't make sense to set it above the OC_FAULT_LIMIT so it also has a practical limitation of less than 15.97 A (except for the C+D application).

The user is encouraged to take into account the increase in inductor current that will occur during VOUT increases. This capacitor charging current will have a magnitude of i= C_out*dv/dt and will be added to the DC load current.

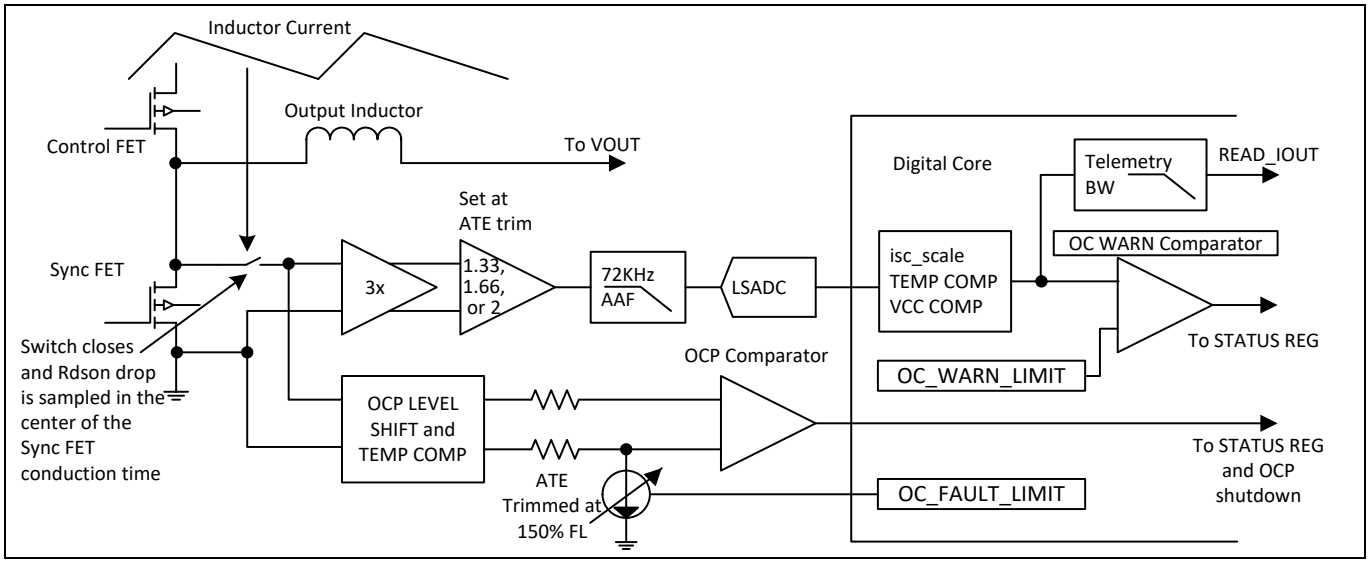


Figure 21 Current settings

4.5 Current Reporting Accuracy

The internal switchers can have up to a 1% (of max rating) offset error in the IOUT sense. The gain error is ≤5%. The chart below shows the % contribution for each source, offset and gain, from 5% load to 100% load for the 4 A outputs.

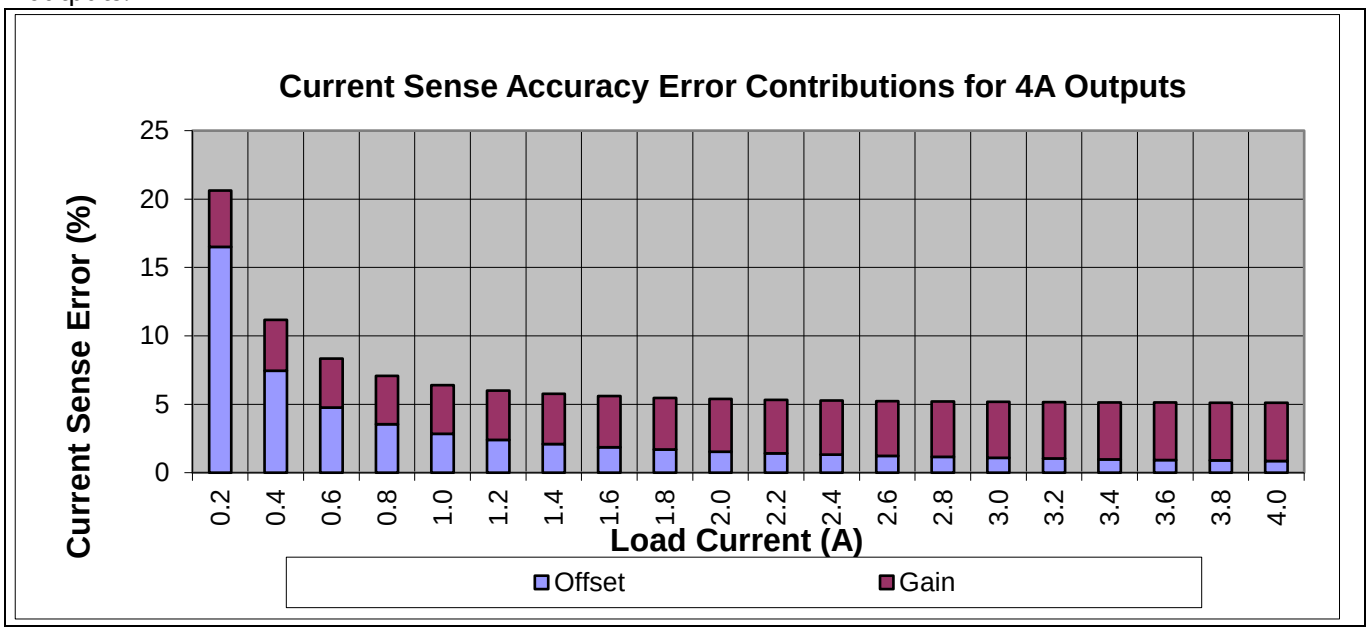


Figure 22 Current reporting

4.6 Over Voltage Settings at Start-up and Shut Down

Before the Switchers are enabled with the Enable pin or OPERATION command and during VOUT ramp up while VOUT is less than 1 V, the output is protected from an OV condition by a fixed OVP threshold. The user can choose between 1.35 V and 2.75 V by setting the fixed_ovp_thresh bit in register xx26h to 1 for 2.75 V, 0 for 1.35 V. If the output is using 2:1 scaling, the fixed thresholds will be 2x the values shown.
This bit is available for each switcher output.

Set the fixed_ovp_thresh greater than the largest VOUT_COMMAND value that will be seen in the application. The logic will switch from relative threshold to the fixed threshold when the Enable goes low, (or OPERATION off command). If Enable goes low with VOUT > fixed_ovp_thresh, an OVP condition will be declared and VOUT will be clamped low with the LS FET and the TOFF_RAMP down time will not be seen. The SM_ALERT# and the STATUS bit will not assert because they are masked by the Enable pin = low.

Figure 23 PINK=SM_ALERT#, GREEN=VOUT, After Enable is de-asserted, VOUT drops from 1.5 V to 0.27 V in 15 µs TOFF_FALL is 1 ms, Fixed_OVP_Thresh=1.35 V, VOUT=1.5 V

4.7 Over Voltage Settings under Steady State

After VOUT has ramped up past 1V (or after VOUT has reached its final value if it is less than 1 V), the OVP switches to a value that is relative to the voltage set by VOUT_COMMAND. There are eight (8) relative threshold values from 50mV to 400 mV (above VOUT) in 50 mV increments. The user sets the relative threshold by sending a VOUT_OV_FAULT_LIMIT value that is greater than the VOUT_COMMAND by the required threshold. If the VOUT_COMMAND is 1 V, a VOUT_OV_FAULT_LIMIT of 1.4 V (or greater) will cause the relative OVP threshold to be 400 mV. If the VOUT_COMMAND is reduced to 0.9 V, the relative threshold of 400 mV will cause an OV fault at 1.3 V. If the VOUT_COMMAND increases VOUT to 1.2 V, the relative OVP threshold will be reduced to 200 mV (FAULT_LIMIT-COMMAND). If the VOUT_COMMAND increases VOUT to 1.4 V, the new relative threshold will be 50 mV. The user can't cause an OVP fault by setting the VOUT_COMMAND to a value greater than or equal to the VOUT_OV_FAULT_LIMIT.

The relative OVP threshold will always be 50 mV above the VOUT_COMMAND value in the scenario described above with the VOUT_COMMAND being increased to the VOUT_OV_FAULT_LIMIT or above.

The user should set the VOUT_OV_FAULT_LIMIT value such that it is > 400 mV above the largest VOUT_COMMAND value that will be used in the application.

Each loop reports out the relative OVP threshold in Read Only (RO) register xx56h [2:0]. 0 = 50 mV, 1 = 100 mV…up to 7=400 mV. If 2:1 scaling is used, the relative OVP threshold is 2x the value shown.

The OV_WARN_LIMIT is not a relative threshold. It is the absolute value set by the user. The user can cause an OV_WARN flag by sending a VOUT_COMMAND greater than the OV_WARN_LIMIT threshold.

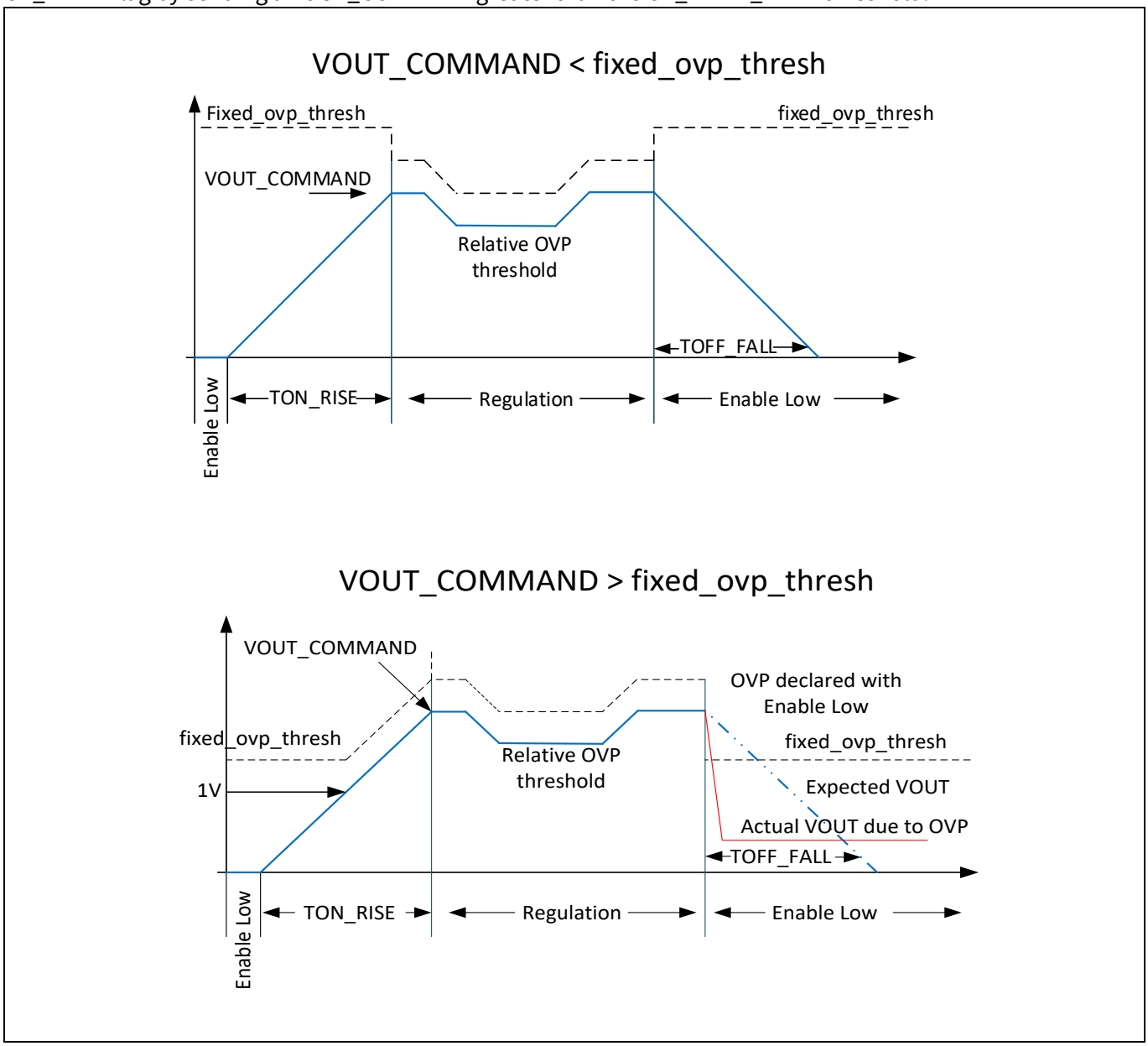


Figure 24 VOUT_COMMAND

If VOUT_COMMAND = 0 V (or any value less than 0.25 V), the relative o V threshold will be used as VOUT transitions down to 0 V. Then the fixed_ovp_thresh is used while waiting for a new VOUT_COMMAND.

4.8 Under Voltage Settings

Similar to OVP, the UV protection is based on thresholds that are relative to the VOUT_COMMAND value. There are eight (8) relative threshold values from 50 mV to 400 mV (below VOUT) in 50 mV increments. The user sets the relative threshold by sending a VOUT_UV_FAULT_LIMIT value that is less than the VOUT_COMMAND by the required threshold. If the VOUT_COMMAND is 1 V, a VOUT_UV_FAULT_LIMIT of 0.6 V (or less) will cause the relative UVP threshold to be 400 mV. If the VOUT_COMMAND is increased to 1.2 V, the relative threshold of 400 mV will cause a UV fault at 0.8 V. If the VOUT_COMMAND decreases VOUT to 0.7 V, the relative UVP threshold will be reduced to 100 mV (COMMAND-FAULT_LIMIT). If the VOUT_COMMAND decreases VOUT to 0.6 V (or

lower), the new relative threshold will be 50 mV. The user can't cause a UVP fault by setting the VOUT_COMMAND to a value less than or equal to the VOUT_UV_FAULT_LIMIT.
The relative UVP threshold will always be 50 mV below the VOUT_COMMAND value in the scenario described above with the VOUT_COMMAND being decreased to the VOUT_UV_FAULT_LIMIT or below.
The user should set the VOUT_UV_FAULT_LIMIT value such that it is < 400 mV below the smallest VOUT_COMMAND value that will be used in the application.
Each loop reports out the relative UVP threshold in Read Only (RO) register xx56h [6:4]. 0 = 50 mV, 1 = 100 mV … up to 7=400 mV. If 1:2 scaling is used, the relative UVP threshold is 2x the value shown.
The UV_WARN_LIMIT is not a relative threshold. It is the absolute value set by the user. The user can cause a UV_WARN flag by sending a VOUT_COMMAND less than the UV_WARN_LIMIT.

4.9 Over Temperature

The IRPS5401 has two (2) on die temp sensors; one for SW-A and B and one for SW-C, D and the LDO.
A READ_TEMPERATURE_1 command to SW-A or SW-B will report the same value. A READ_TEMPERATURE_1 command to SW-C, D or the LDO will report the same value.
The OT_WARN_LIMIT and OT_FAULT_LIMIT can be set to any value from 0°C to 255°C in increments of 1°C. OT_WARN should be set less than OT_FAULT.
The OT_FAULT_RESPONSE can be set to IGNORE, SHUTDOWN and latch off, or SHUTDOWN and auto recover when temp decreases (also known as INHIBIT).

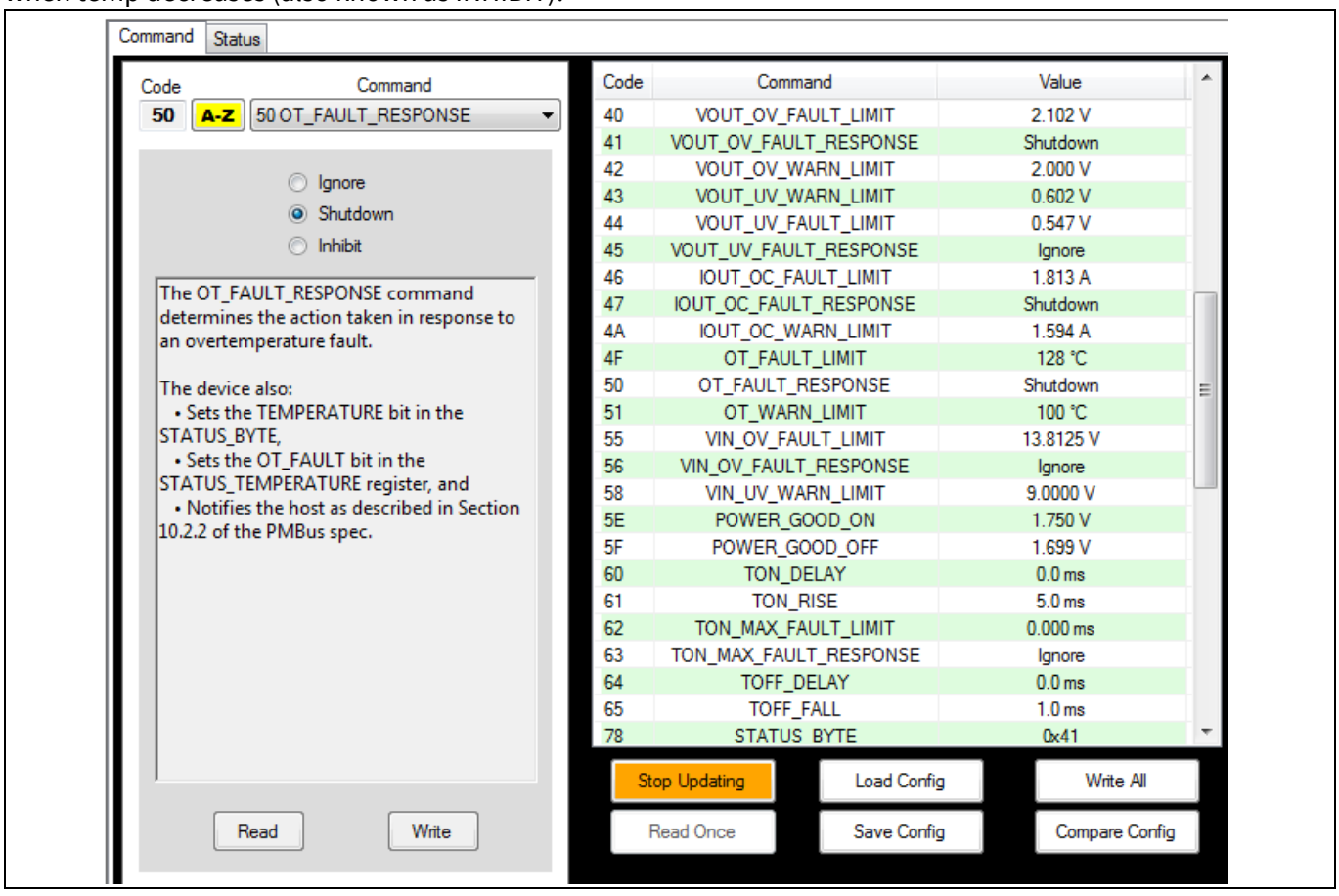


Figure 25 Command set

4.10 ½ Scaling of VOUT

If VOUT is > 2.55 V, VOUT will need to be scaled by 1/2. This means a resistor divider will need to be used to divide the output voltage by 1/2. This has been done with two 1K resistors on SW-C and D on the demo boards. VOUT>2.55 V is not just the VOUT_COMMAND value but also VOUT_COMMAND + OFFSET and MARGIN_HIGH value.

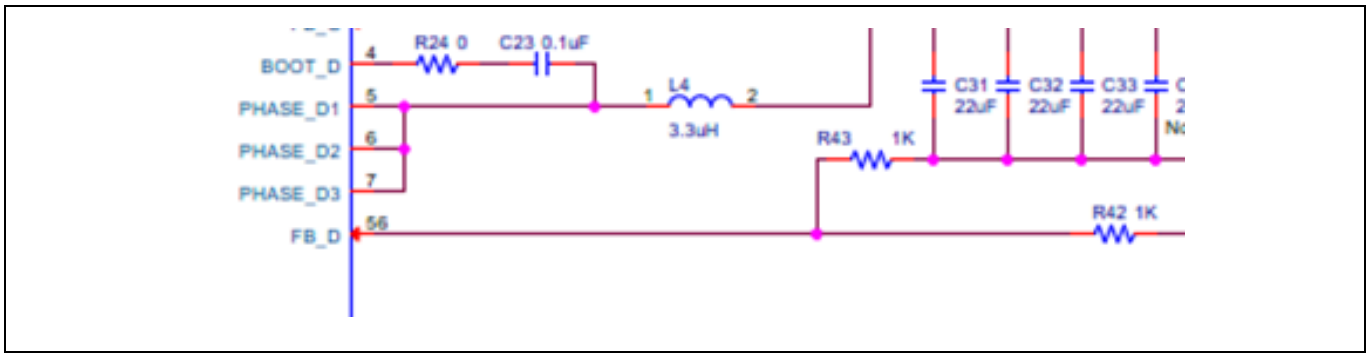


Figure 26 VOUT scaling

FB_x is not a high impedance input so an error may be introduced due to these resistors. This is an error above and beyond the error introduced by the tolerance (usually 1%) of the resistors. All FB_x pins are internally biased up to 1 V with an internal 20 k resistor. So anytime FB_x is not sitting at 1V a bias current will be sourced or sunk by the FB_x pin. The worst case error will be with VOUT = 5 V. Internally the DAC will be set to 2.5 V and the FB_x pin will be at 2.5 V during regulation. This will result in IFB_x = (2.5 V-1 V)/20k = 75 µA. This additional current will flow in the upper resistor of the divider (R42 above) and result in and error of 75 µA*1 k = +75 mV. +1.5% error.

At the expense of added power dissipation, the error can by reduced by using lower value resistors. If two 250 Ω resistors are used instead of 1 k, the 75 mV error would be 18.75 mV (0.37% error). But power dissipation would increase from 12 mW to 50 mW.

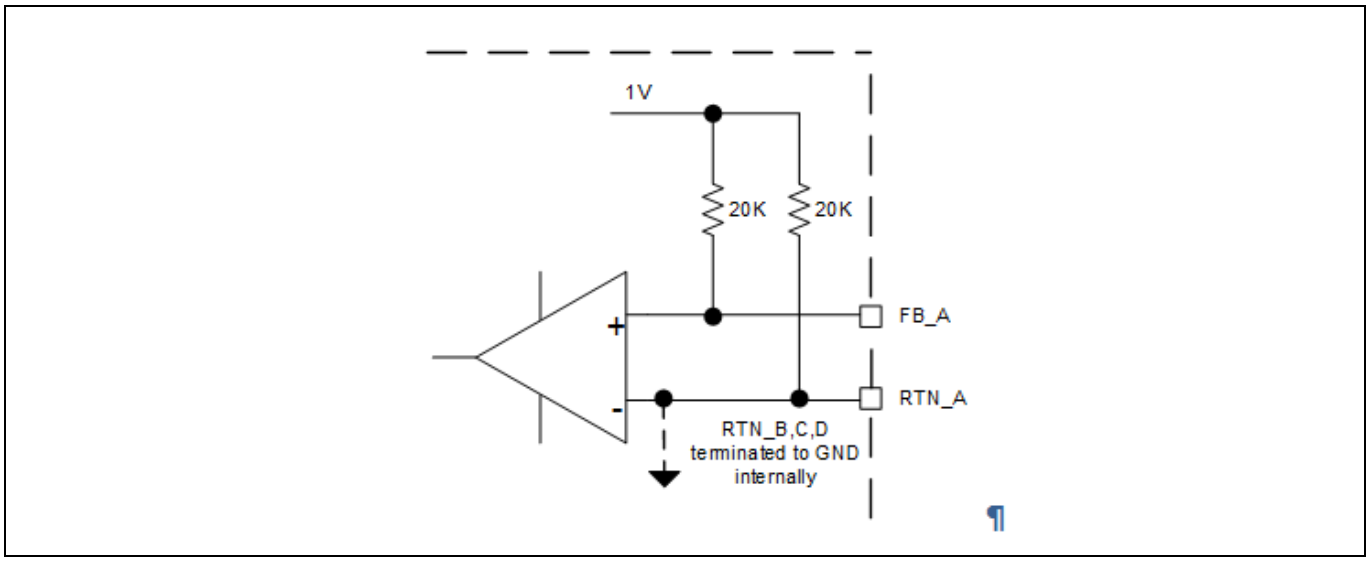


Figure 27 FB_x

Alternatively, the upper resistor can be reduced to account for the added bias current. This is best suited for outputs that would be set and not changed. If R42 was reduced to 976 Ω in the example above and VOUT is set

to 5 V, the additional 75 µA added to the 2.5 mA that is already in the resistor will cause the voltage drop on R42 to be 2.513 V. VOUT will be 5.013 V versus the 5.075 V with R42 = 1 k (assuming all other error sources are 0).

5 External Power Stage

To enable external drive on SW-A, go to 'Design Tools' → 'Device Operating Mode' and choose 'Use External Drive on Switcher A'. The GUI will update Switcher A to Switcher A Ext.

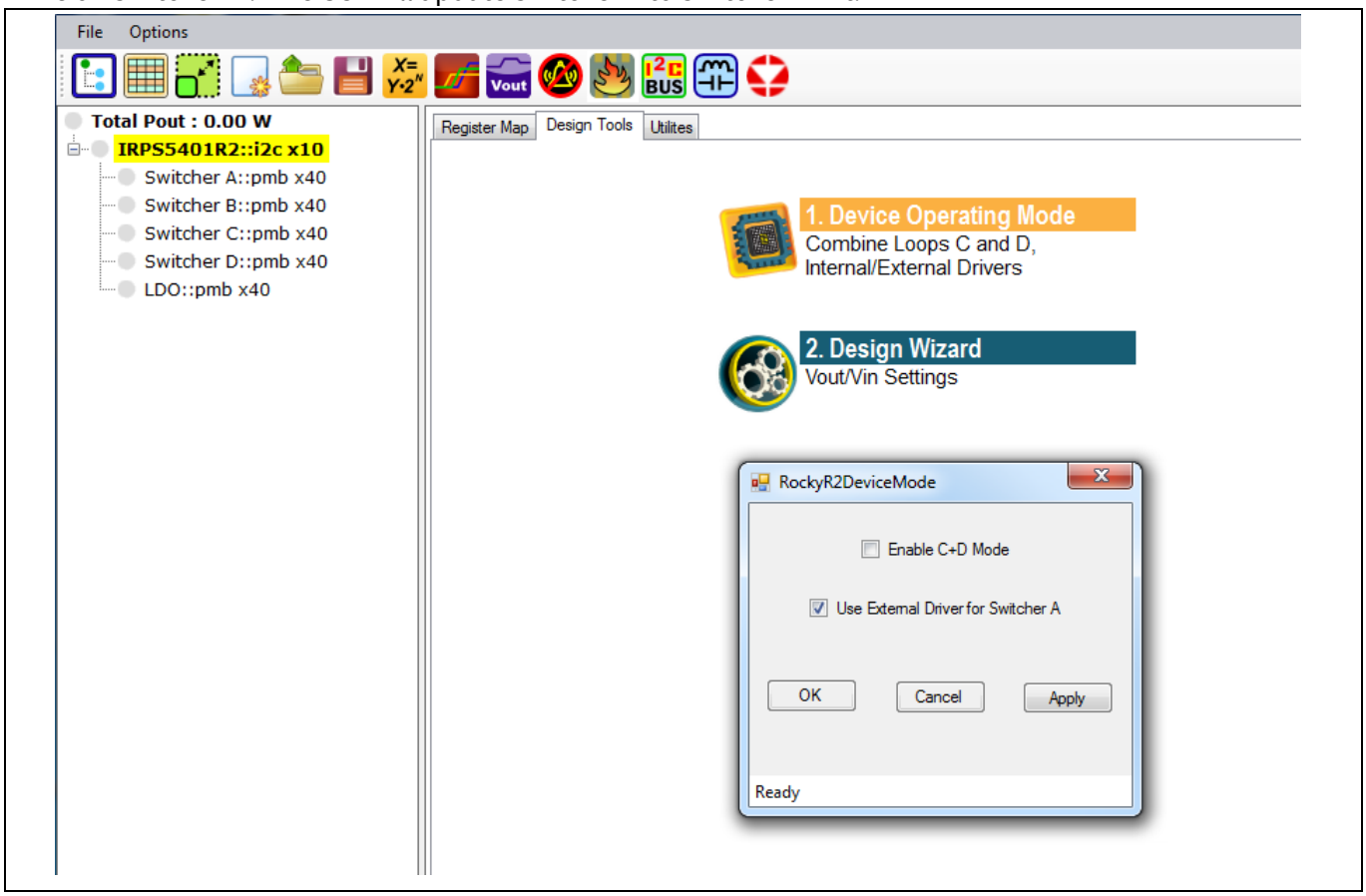


Figure 28 Design tool view

In EXT mode, BOOT_A and PHASE_A are no connects. PWM_A is used to drive the PWM input of an external power stage. The ISEN_A+ and ISEN_A- are differential sense inputs used to sense the DCR drop of an output inductor, the drop across a precision shunt resistor, or as shown here, the IOUT pin of an Infineon power stage. Because it is differential sense, ISEN_A- is connected to a reference voltage above GND.

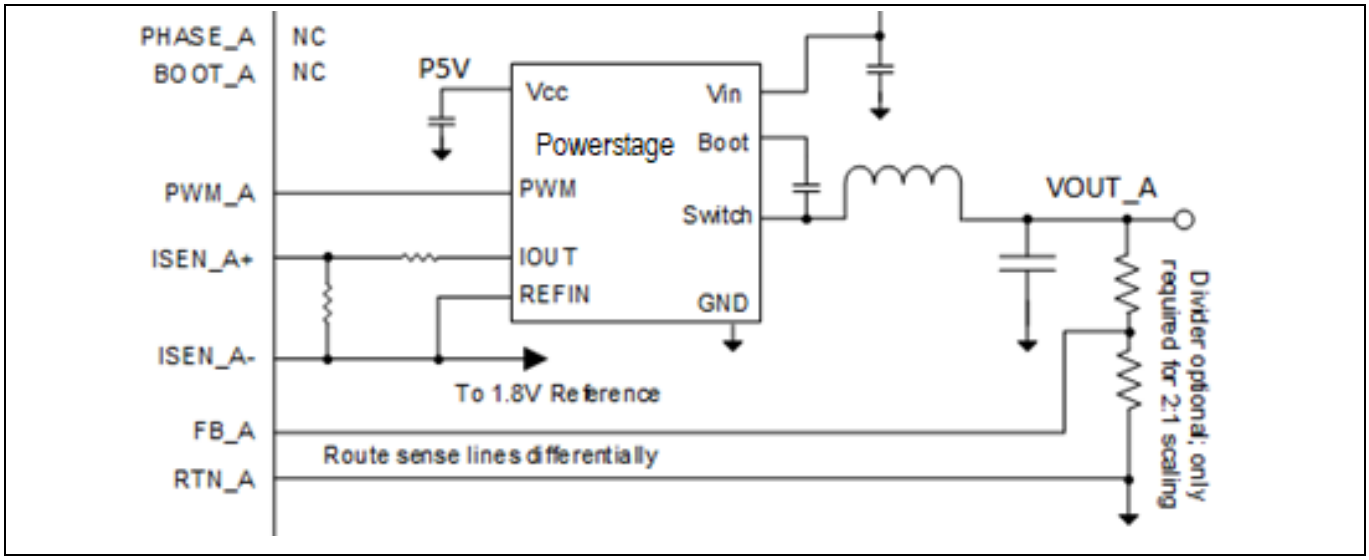


Figure 29 SW_A is the only output with differential VOUT sense to compensate for any GND plane losses due to the high output current

5.1 ISENSE AMP Gain Settings

Unlike the internal current sense, both OC_WARN and OC_FAULT are based on the output of the LSADC. The ISENSE signal coming in is amplified with a user selected gain of 10x to 50x. The gain factor used will be based on the magnitude of the signal coming in.

The IOUT from the power stage is scaled to 1 mV/A on the DB295, so 10x times 1 mV = 10 mV/A at the input to the LSADC. The MAX input to the LSADC is 700 mV, so the user needs to make sure the MAX current required to be sensed does not exceed this limit. 0.7 V/10 mV/A = 70 A. Since the DB295 is rated for 50 A max, the ecs_gain is limited to 10x. 1 mV/A * 10* 50 A = 500 mV at the OCP trip point.

The ecs_scale register needs to be set so that it represents the Q level of the output of the LSADC in mA's. For this example, 50 A = 500 mV = 409 DEC. (10 bit ADC). The Q is 122 mA per code (50 A/409). The LSB of the ecs_scale register is 0.976 mA. So ecs_scale will be populated with 122 mA/0.976 mA = 125 DEC (7Dh) on the DB295 to give accurate IOUT reporting and OCP trip point.

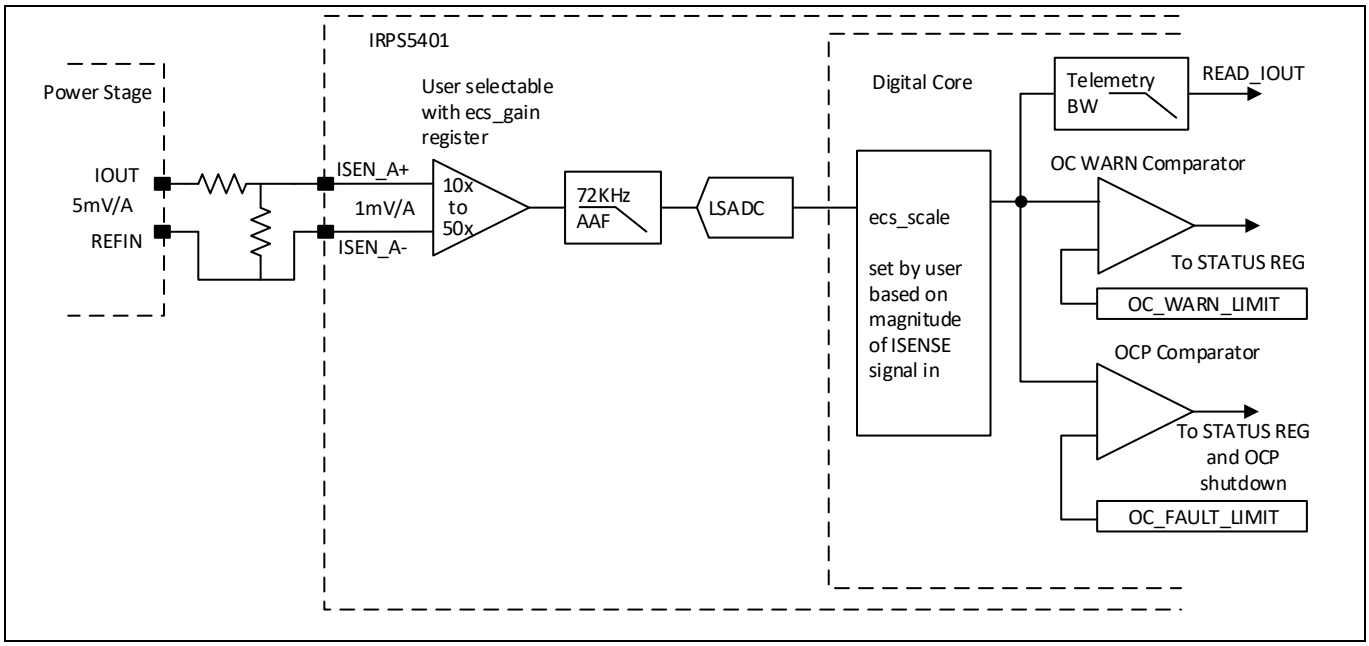


Figure 30 Ecs_scale

5.2 Layout Concerns

ISENSE FEEDBACK
The screen grab below shows the current sense connections for inductior current sensing, on layers 1 and 3, from the output inductor to pins 45 and 46 on the IRPS5401.

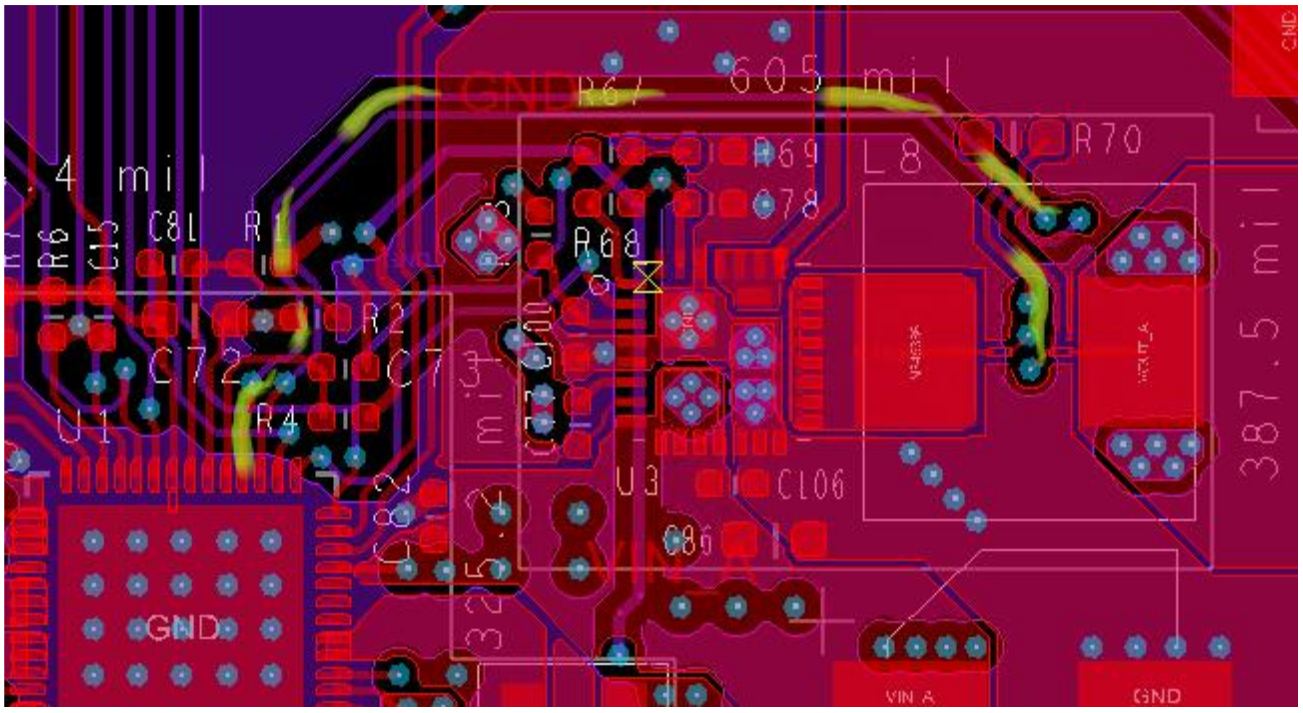


Figure 31 Current Sense Routing

5.3 VSENSE FEEDBACK

In this screen grab the VSENSE lines on layer 3 are highlighted. The DB295 has a divider network and a 10 Ω resistor for small signal injection to do Bode Plots. An actual layout could be simpler if the divider network is not required.

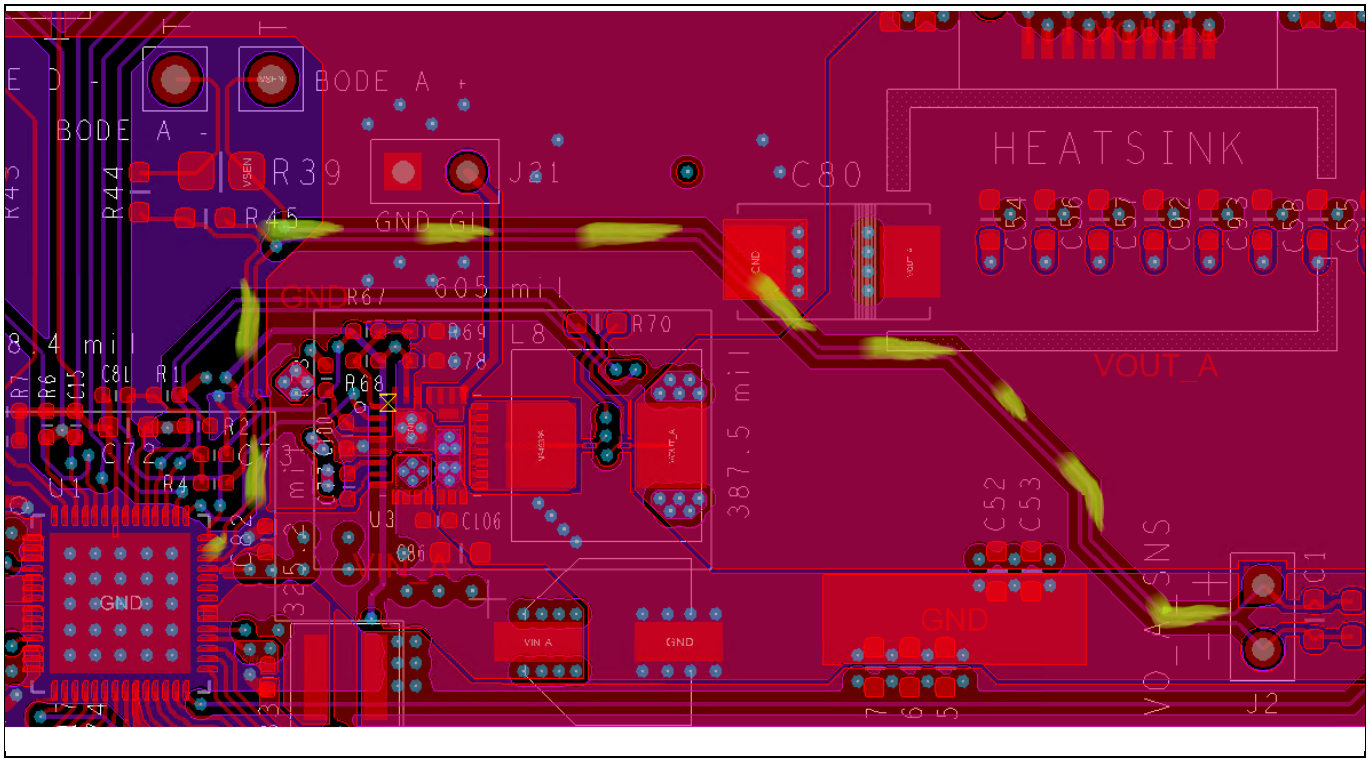


Figure 32 VSENSE on layers 1, 3

5.4 VIN Decoupling

This screen grab shows that MLCC caps are placed directly aside the TDA21240 to create the shortest loop possible for the current path for the FETs in the power stage.

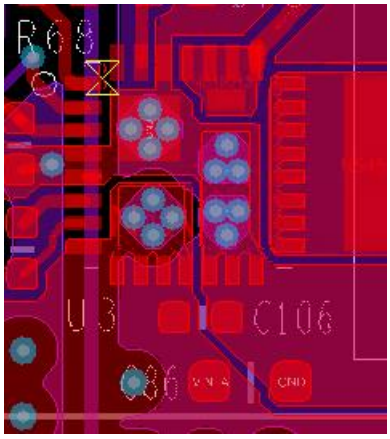


Figure 33 MLCC capacitors aside TDA21240

6 C+D Operation

The IRPS5401 can be configured such that SW-C and D can be operated as a single 2 phase output. This is done by selecting 'Design Tools' → 'Device Operating Mode' checking 'Enable C+D Mode'

- In C+D mode, the GUI will display 'Not Used' for SW-D
- PMBus commands to SW-D will be NAK's and a CML fault will be issued
- VIN_C and VIN_D must be connected to the same INPUT VOLTAGE

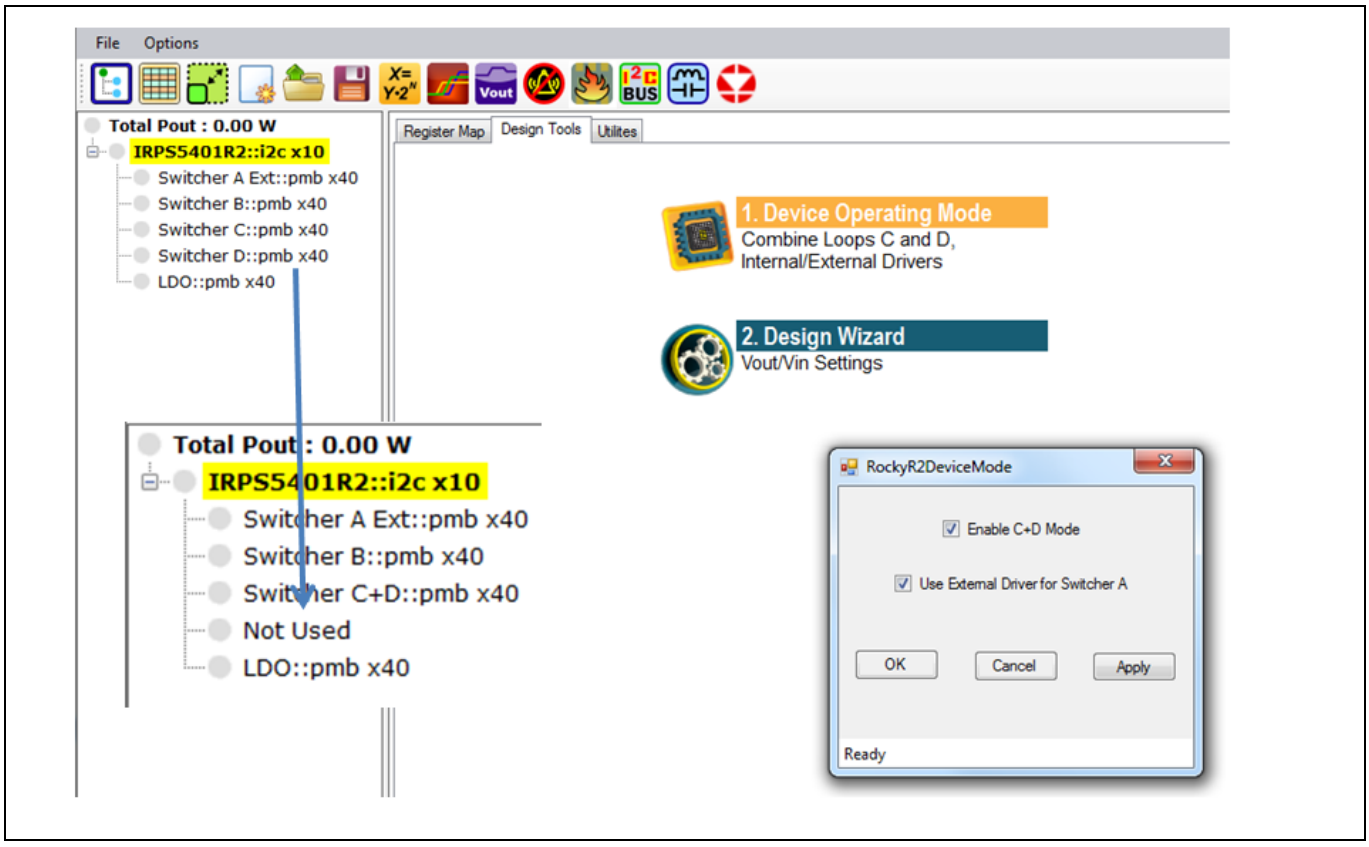


Figure 34 Device operating mode example

6.1 Current Balance

In C+D Mode, a phase balance algorithm has been added to balance SW-D and SW-C phase current. This feature is enabled by setting register 0x0028 [14], low_speed_pbal_en = 1. RO register 0x0050 [13], low_speed_pbal_saturation, will indicate balanced operation when this bit is 0

6.2 Over Current Protection

In C+D Mode, OC_WARN and OC_FAULT commands sent to SW-C will be divided by 2 and applied to SW-C and SW-D individually.

7 MTP Programming

7.1 Programming a Single Config File

Inside the PowIRCenter GUI, choose the 'Utilities' Tab (1) and Click on 'Rocky R2 Device Programmer' (2). The 'RockyR2Programmer' box (3) will pop up and display the number of segments left to be programmed in each section, CNFG, TRIM, USER.

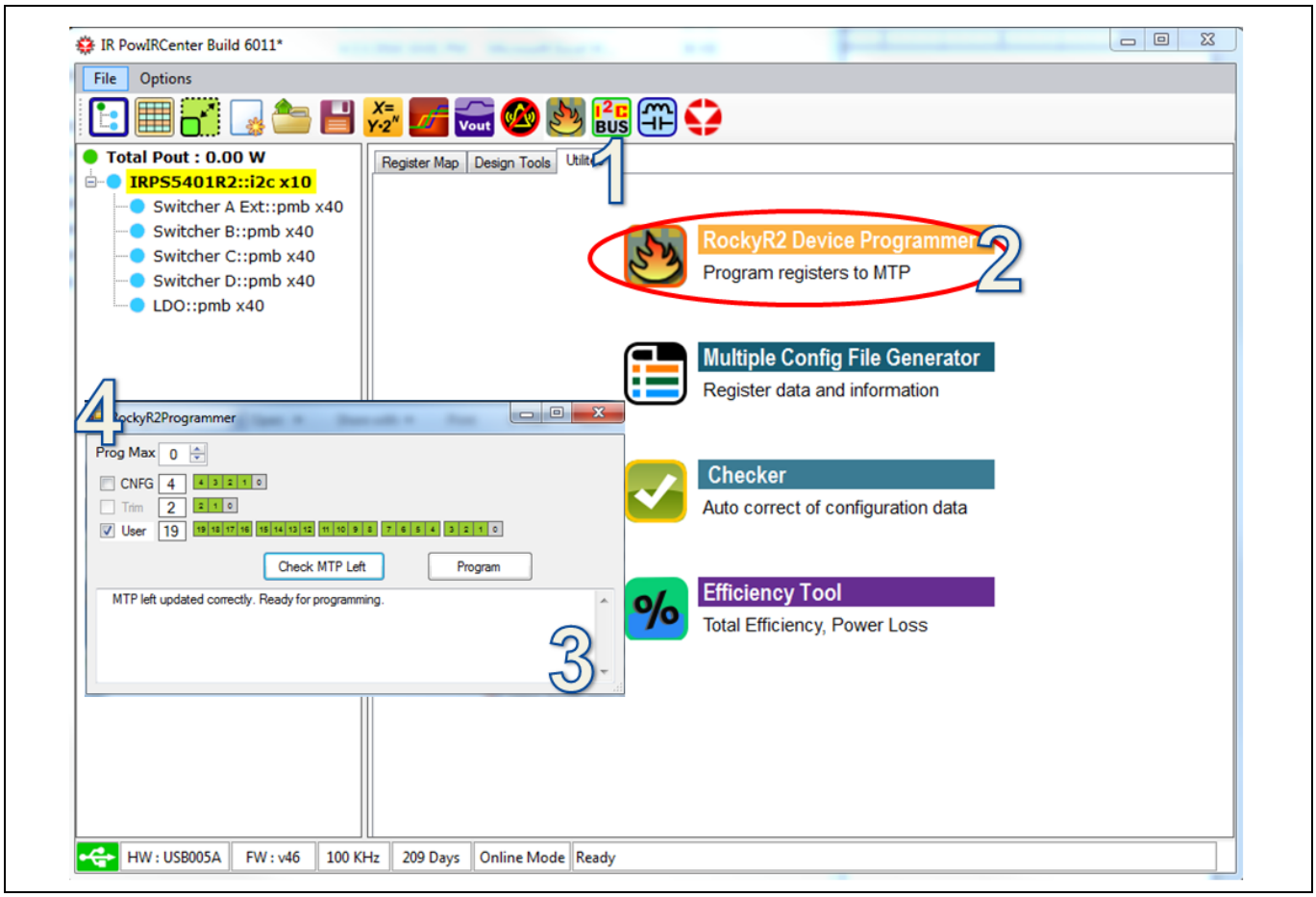


Figure 35 Single config file

For single config file usage (MTP pin offset not used for multiple config file access), the PROGMAX register (4) in CNFG section must be 0 or 1. Both values indicate a single file is programmed. Check 'User', click 'Check MTP Left', and finally click 'Program' button. The device will program another segment of the 20 segments available and the 'RockyR2Programmer' box will show another 'grey' box in the User section.

7.1 Generating Multiple Config Files (*.mic)

Go to 'Utilities'→'Multiple Config file Generator'. In the 'RockyR2MultipleConfigFileGenerator' dialog box set the Prog_Max to the number of files to be programmed. Click on the first 'Click to select a config file' box and select the file to be loaded into the segment to be selected by MTP resistor value 845 Ω. Step and repeat to the n^{th} file.

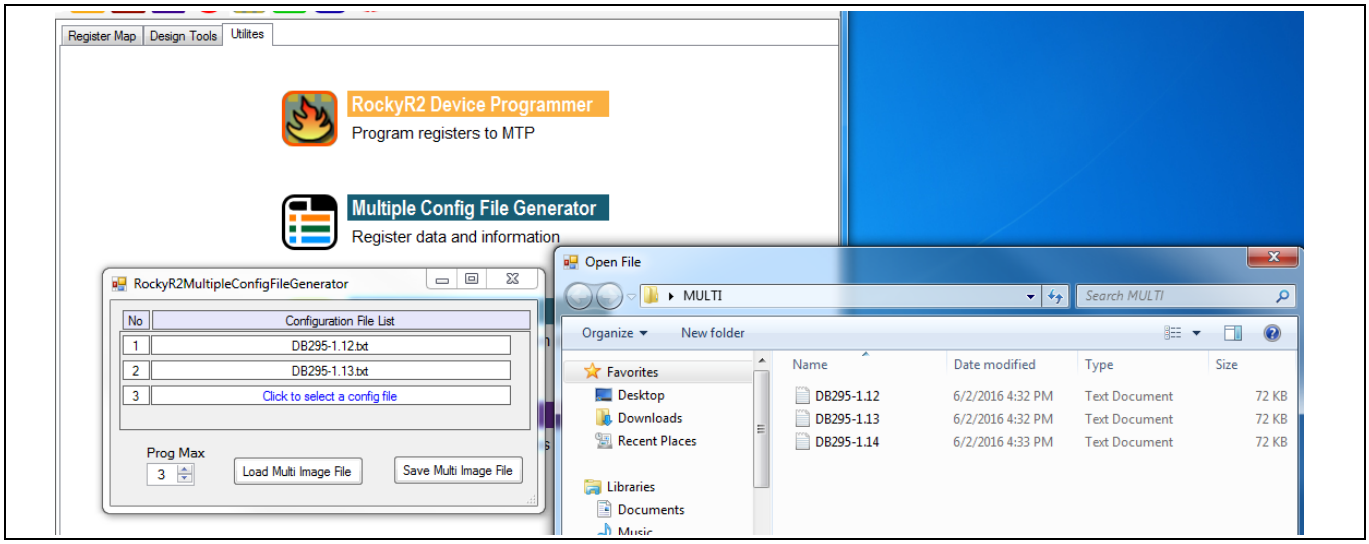


Figure 36 Multiple Config file Generator

When all the files are loaded, click on 'Save Multi Image File' and name the file to be used. Click 'Save'

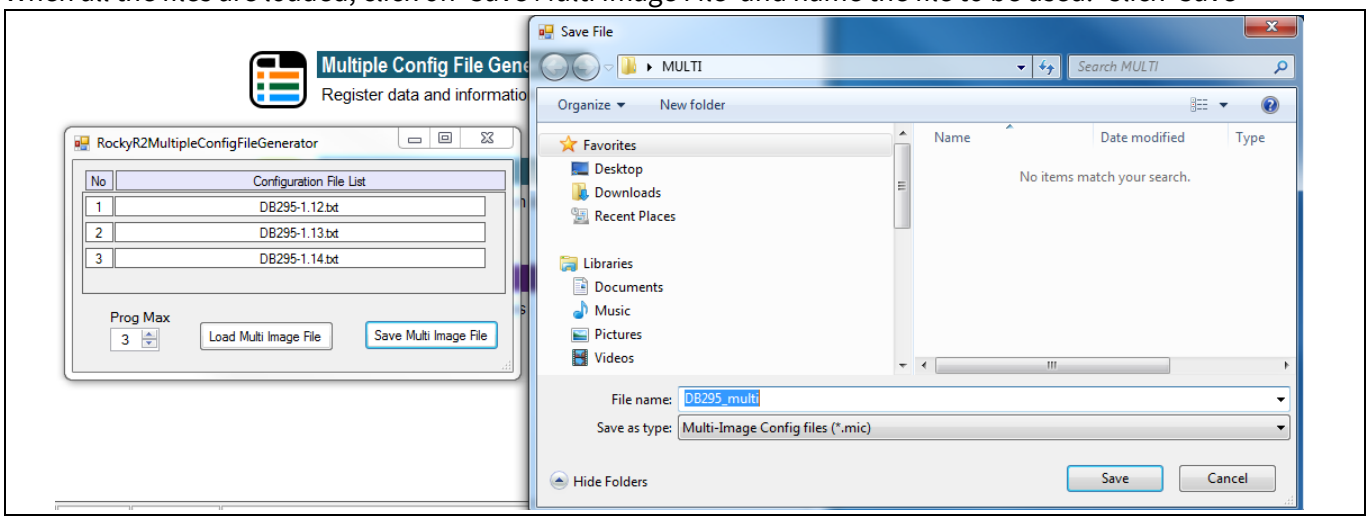


Figure 37 Saving multi image file

The GUI does not support programming of *.mic files. The file will be programmed at ATE test if the volumes are appropriate or by using the gang programmer for smaller sample and production runs.

7.1 Using the Multiple Config File Index Feature

Each separate PMIC configuration stored within the multiple config file can be accessed by a resistor connected to the MTP pin.
The resistor must be connected from MTP to AGND (pin 50). The resistor must be decoupled with a 10 nF capacitor (X7R type). The IRPS5401 will source 100 µA through the offset resistor for 1 ms immediately after POR, the LSADC will measure the voltage drop on the resistor and the value will be latched into the digital core. This happens one time at start up, so updating this resistor after POR will not affect the offset.
The table below shows the resistor value required to give the corresponding config file offset.
An 845 Ω resistor will give access to the config file programmed into the 1st segment, a 1.3 kΩ resistor will select the 2nd segment, etc.

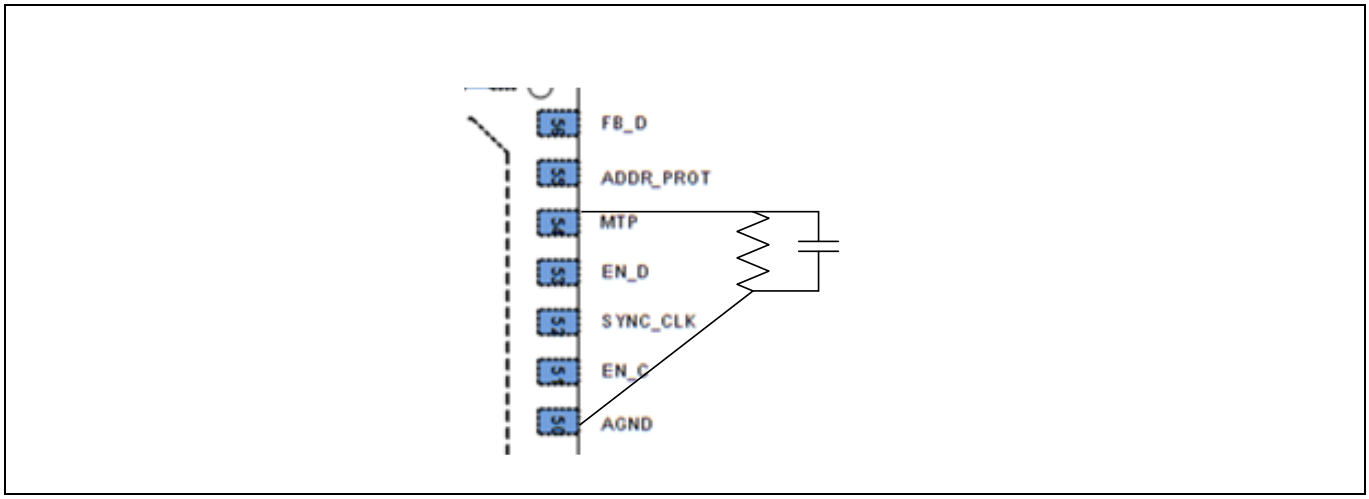


Figure 38 Resistor on MTP pin

The PROGMAX register in the CNFG section has a max value of 15, so the table shows 15 possible selections with an offset of +0 to an offset of +14.
READ ONLY register 0x0052 [11:8], nvm_user_image_sel, shows the value of the offset (given the resistor attached) provided that the PROGMAX is set to the correct value.

Table 3 Config offset table

MTP resistor	Config Offset
0.845 kΩ	+0
1.30 kΩ	+1
1.78 kΩ	+2
2.32 kΩ	+3
2.87 kΩ	+4
3.48 kΩ	+5
4.12 kΩ	+6
4.75 kΩ	+7
5.49 kΩ	+8
6.19 kΩ	+9
6.98 kΩ	+10
7.87 kΩ	+11
8.87 kΩ	+12
10.00 kΩ	+13
11.00 kΩ	+14

FAQ

1. What happens if I program another config file after the .mic file is programmed?
   ANSWER-The PROGMAX and resistor installed will no longer have any effect on the config file read out of NVM. The most recent file written will be the file that is read out and used at POR. However, nvm_user_image_sel, will still display the offset chosen by the resistor installed.

2. What happens if the PROGMAX and resistor value point to an offset (segment) that was not programmed?
   ANSWER – No valid USER image will be loaded and the device will not start. READ ONLY register 0x0052 [12], nvm_read_no_image, will be set to a 1 and READ ONLY register 0x0052 [2], nvm_user_loaded, will be set to a 0. You will need to change the resistor to access a valid (programmed) segment or program an image into the segment being pointed to.

3. What happens if the PROGMAX is smaller than the number of images programmed?
   ANSWER –This is essentially a repeat of #1 above. The last image in the *.mic file is the one that will be loaded and used at start up. The resistor offset will be ignored until the PROGMAX is updated and set equal to the number of programmed segments.

8 Modulator Details

8.1 Emulated Current Mode Control with Digital P and I

IRPS5401 regulates VOUT by modulating the duty cycle (DC) applied to the power stage. The DC needs to vary based on VIN changes and load changes, and to a smaller degree changes in temperature and life. VOUT is compared to Vref (the DAC voltage) by an analog front end that generates an error voltage. The ADC measures this error voltage and converts it to a hex code.

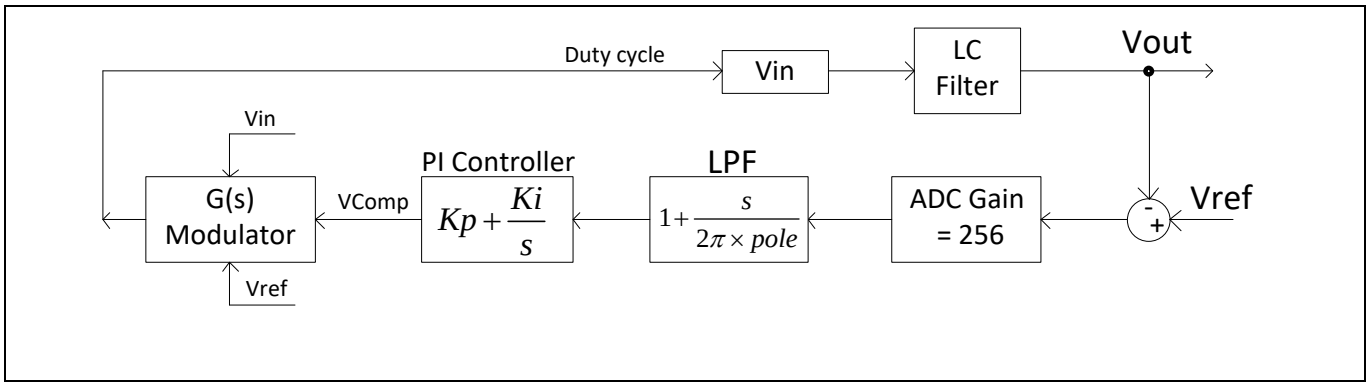


Figure 39 Emulator

The output of the ADC is filtered by the low pass filter (LPF), also called Kpole, and gained up by the Kp (P term) and Ki (I term). The PI controller's sole purpose in life is to maintain Vcomp such that the output of the ADC is 0. If VOUT droops due to load increase or a drop in VIN, the output of the ADC will increase and force the PI controller to increase Vcomp. When Vcomp increases, the emulated current in the G(s) Modulator block forces the DC to increase. An increase in VOUT will have the opposite effect.

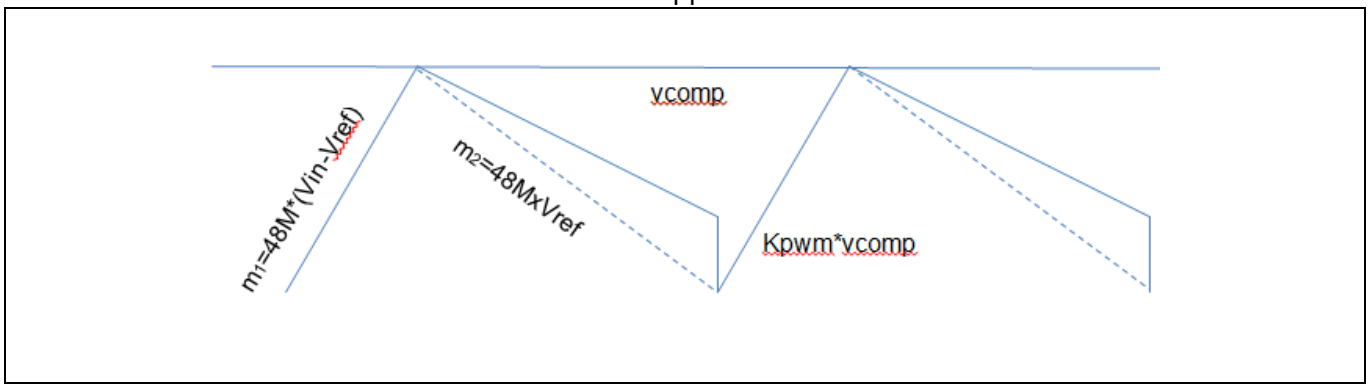


Figure 40 Vcomp

The G(s) transfer function is:

$$\frac{d(s)}{vcomp(s)} \approx \frac{(1 - Kpwm \times D/2).s + Kpwm \times fsw}{48M \times Vin \times (1 + s\frac{Ts}{2})}$$

And the total loop gain is:

$$Loop\_Gain = 256 \times (1 + \frac{s}{2pi * LPF}) \times \frac{Kp.s + Ki}{s} \times \frac{(1 - Kpwm \times D/2).s + Kpwm \times Fsw}{48M \times (1 - \frac{Ts}{2}s)} \times \frac{1}{LC.s^2 + s.\frac{L}{Rload} + 1}$$

8.1 Description of Excel PI Calculator Tool

An Excel tool has been created to help determine the Ki and Kp values that should be used in the config file based on the application L, C and switching frequency. Contact your local FAE to receive a copy.
The Calculator is divided into 2 worksheets, the 'Power Section' tab and the "Compensator" tab
In the Power Section tab, the user describes their application: VIN, VOUT, FSW, Inductor and Capacitor…etc.
The tool will use the design inputs to calculate the minimum L and C.

Shown is a 1 V output at 800 kHz. The calculated L for 33% ripple is 0.87 µH. A standard value of 1 µH has been used.

A 'minimum' bulk capacitor is shown based on the max voltage overshoot and undershoot. This cap value is usually augmented as a safety factor to guarantee meeting the spec.

The Capacitor section shows different banks of capacitors so you can put in different ESR and ESL values. The capacitor value in the worksheet should be the de-rated value after DC and AC coefficients are taken into account. This is typically 55% to 60% of the MFR specified value.

1) Design Inputs:		
Controller Type	Rocky	
Select Operation Mode:Analog or Digital?	Digital	
Input Voltage (PVin):	12.00	V
Use Separate Supply for PVcc? (Y/N)	N	
Biasing Voltage for Drivers? (PVcc)	5.00	V
Output Voltage:	1.00	V
Reference Voltage	1.00	V
Output Voltage Scale Factor	1	
Iout	4.00	A
Free-Running Switching Frequency	800	kHz
Duty Cycle	8.3%	
On Time	104.2	ns
Peak to Peak Output Voltage Ripple	1	%
Peak to Peak Output Voltage Ripple	10	mVp-p

2) Inductor Selection:			
Inductor Ripple Current Percentage		33	%
Inductor		0.87	uH
Select Value of Inductor	L	1.00	uH
	Tolerance (%)	20	%
	DCR	13.0	mOhm
	Inductor Current Ripple at No Load	1.15	A(pk to pk)
	Inductor Saturation Current	6.00	A
	Inductance at Isat (Lsat)	0.70	uH

3) Output Capacitors Selection:		
The minimum Required Bulk Capacitance	24.0	uF
Select Output Capacitors:		
PLEASE ENTER SMALL SIGNAL PARAMETERS for Capacitors)		
Output Capacitor Type 1:		
Cout1	25	uF
ESR1	5	mOhm
ESL1	0.5	nH
The number of Capacitor Type 1 (N1)	1	
Output Capacitor Type 2:		
Cout2	11	uF
ESR2	5	mOhm
ESL2	0.4	nH
The number of Capacitor Type 2 (N2)	6	
Output Capacitor Type 3:		
Cout3	1	uF
ESR3	10	mOhm
ESL3	0.03	nH
The number of Capacitor Type 3 (N3)	1	

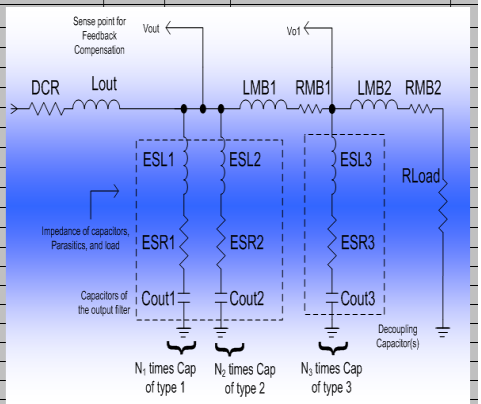


Figure 41 Design Tool

The ‘Compensator’ Tab contains the settings for Kpwm, KPole, and Fo (crossover frequency)

Compensator TYPE					
TYPE II (PI)					
Kpwm	0.25				
Clk	48	MHz			
ADC Gain	256				
Kpole	1084500.00				
Poles and Zeros of the Power Stage:					
Double Pole caused by Output Inductor and Capacitor			Fpo=	16.59	KHz
Half of the Switching Frequency			1/2Fs	400.0	kHz
Selecet Zero Cross Over Frequency between (1/5~1/10) of Fs			Fo	60	kHz
Recommended Compensator TYPE:	PI Controller				

Figure 42 Compensator tab

The bode plot will be displayed when the Kp-reg and Ki-reg values are inserted from the calculated values.

Transfer Functions		
Modulator	0.00568246993779736+0.00643326888947508i	
LC Filter Transfer Function with Current Source	-0.0826987068835445-0.00308791130529924i	
Kp(1+1/4ssqrt(LC))	1-0.06913770771447786i	
High Frequency Pole	0.996948480820248-0.055156209174011i	
Recommended PI Controller		
Kp	5.49	
Kp-Reg (GUI)	37.00	
Ki	143207.52	
Ki-Reg (GUI)	42.00	
Bode Plot		
Use calculated values?	No	
Kp-Reg	37	
Ki-Reg	42	
Kp-Value	5.00	
Ki-Value	140625.00	
Estimated Bandwidth	56.00	KHz
Estimated PhaseMargin	44.14	Degree

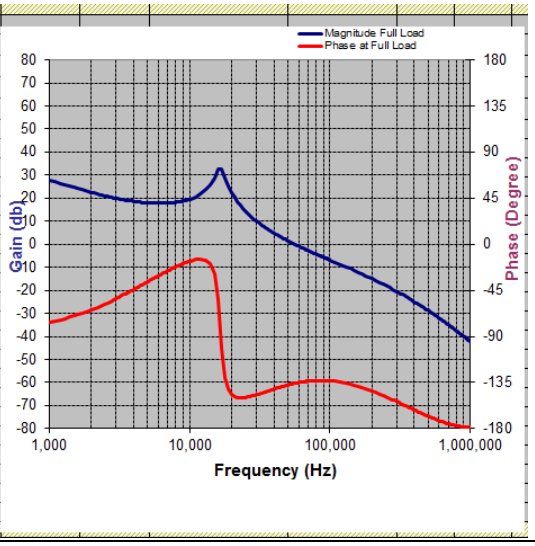


Figure 43 Bode plot

8.2 Recommended Circuit and Operating Parameters for Internal Switchers from the Data Sheet

Input Voltage	Output Voltage	Switching Frequency	Min L_out for 1Ap-p inductor ripple [1]	Min C_out for +/- 3% AC regulation [2]	Kp [3]	Ki [3]
V	V	KHz	µH	µF	Decimal	Decimal
12	0.5 to 1	800	1.1	7 x 22 µF	35	42
	1 to 1.5		1.6	6 x 22 µF	36	43
	1.5 to 2		2	5 x 22 µF	38	43
	2 to 2.5		2.5	4 x 22 µF	40	44
	2.5 to 3.3		3	4 x 22 µF	42	46
	3.3 to 5		3.6	3 x 22 µF	42	50
9	0.5 to 1		1.1	7 x 22 µF	36	43
	1 to 1.5		1.5	6 x 22 µF	37	43
	1.5 to 2		2	5 x 22 µF	38	43
	2 to 2.5		2.2	4 x 22 µF	40	44
	2.5 to 3.3		2.7	4 x 22 µF	42	46
	3.3 to 5		2.7	3 x 22 µF	42	50
5	0.5 to 1		1	7 x 22 µF	38	44
	1 to 1.5		1.3	6 x 22 µF	38	45
	1.5 to 2		1.5	5 x 22 µF	40	48
	2 to 2.5		1.5	4 x 22 µF	41	50
	2.5 to 3.3		1.5	4 x 22 µF	42	53

Figure 44 Bode plot

9 Efficiency, Power Dissipation, and Temp Rise

9.1 GUI Efficiency Tool

The IRPS5401 GUI has a tool that will estimate the power loss and temp rise.

Go to 'Utilities' and choose 'Efficiency Tool'. In the dialog box load in the appropriate VIN, VOUT, L value, L DCR, L core loss, and Switching Frequency. Click on the 'Efficiency Sweep' button.

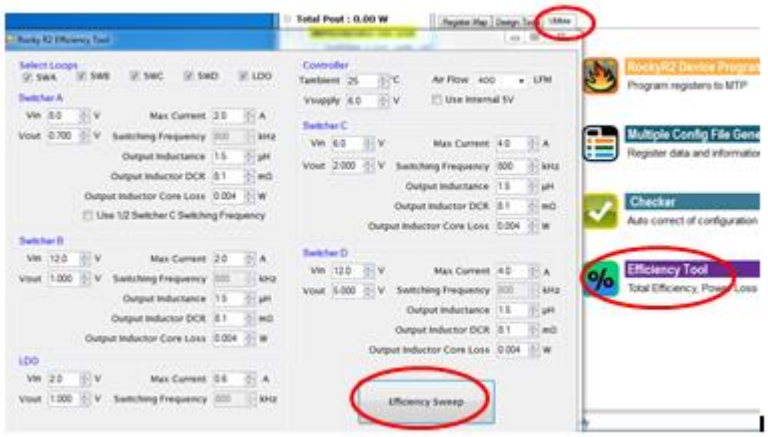


Figure 45 Efficiency tool

The tool will sweep the load from 0 A to the max IOUT specified.

The GUI will display total system efficiency versus load on the left axis (with all outputs increasing from 0 A to maximum at the same rate) and junction temp on the right axis. The calculated junction temp uses the ambient temperature specified by the user and the thermal impedance from junction to ambient is estimated to be 15°C/W at 0LFM.

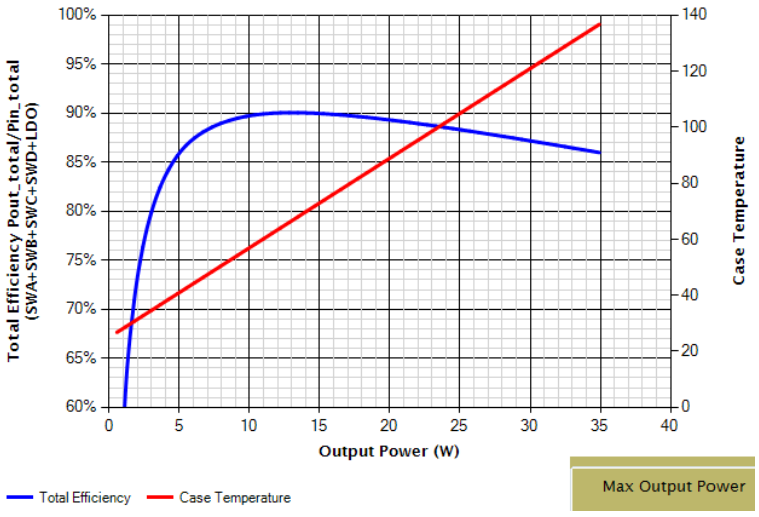


Figure 46 System efficiency vs. load

The GUI will also display:

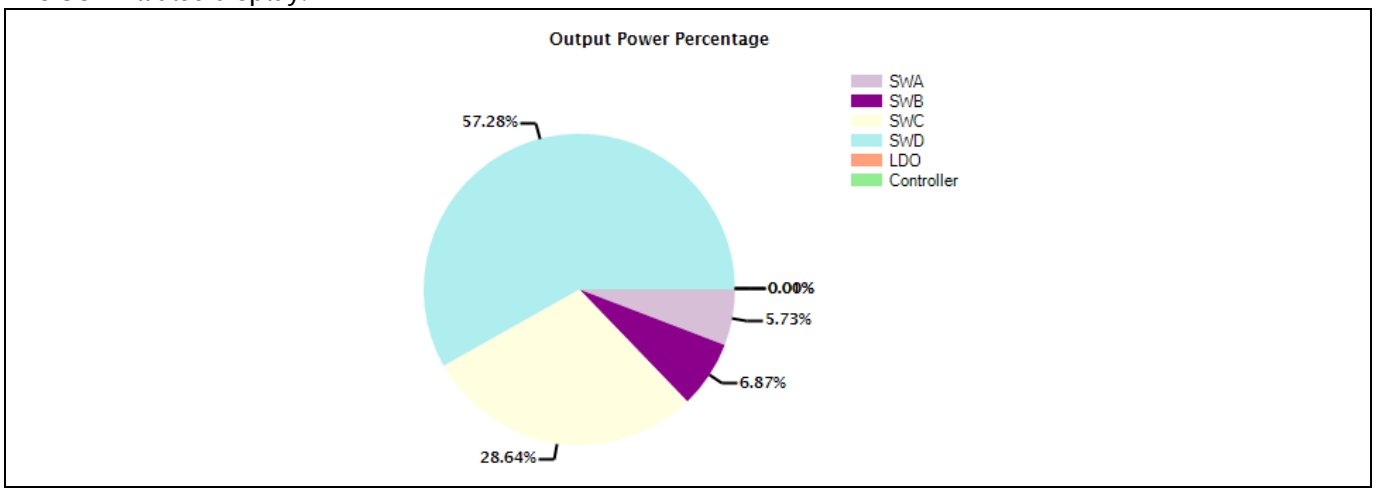


Figure 47 Percentage of output power contributed by each output

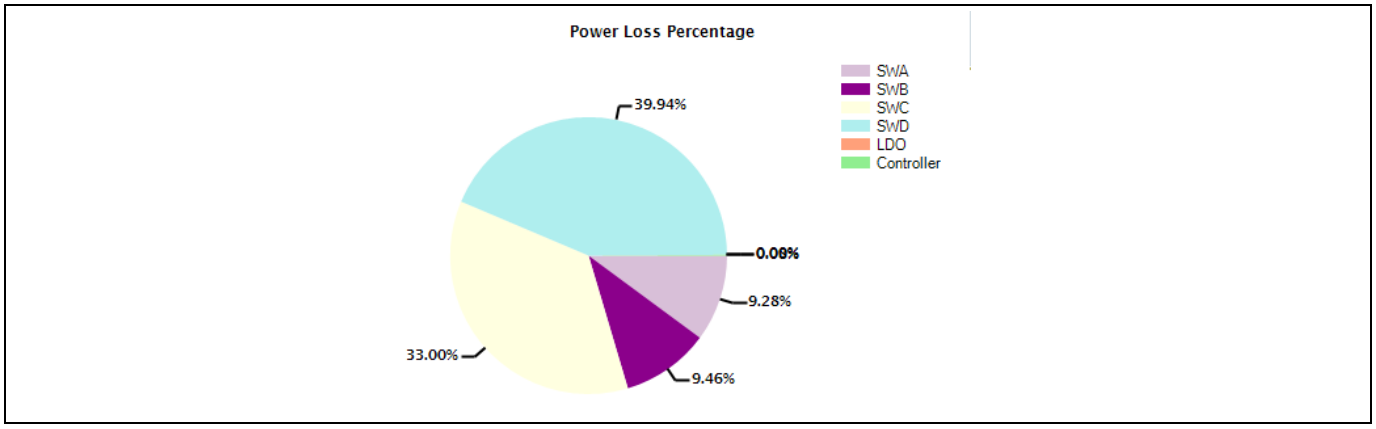


Figure 48 Percentage of the total loss contributed by each output

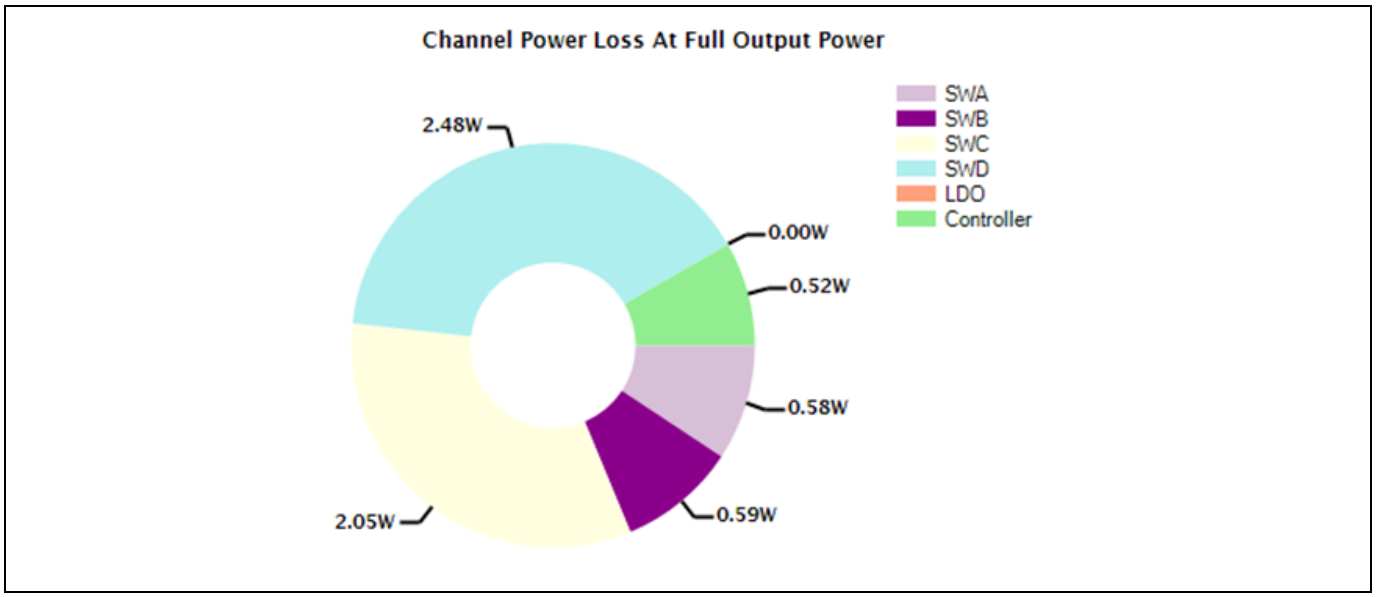


Figure 49 Total loss per channel at full load

9.2 Demo Board Efficiency and Temp Rise

The DB296 was tested at 12 V in with VCC from the internal LDO, All 4 switchers were loaded to the maximum current supported. C+D mode was used to consolidate the number of loads needed. The LDO was not loaded for this test.

TEST SETUP

The DB296 is mounted vertically with no forced airflow. Ambient temperature is 25°C.

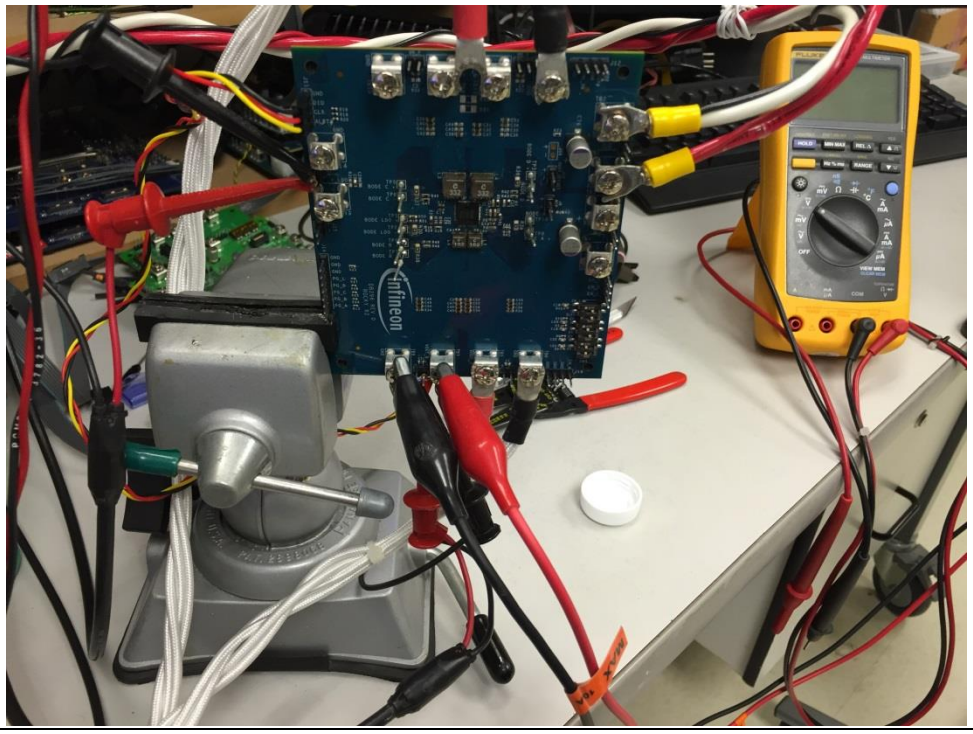


Figure 50 Test set-up

Table 4 Load conditions

Output power			
SW-A	1.997 V	2.00 A	3.994 W
SW-B	1.998 V	2.00 A	3.996 W
SW-C+D	5.06 V	8.02 A	40.58 W
Total			48.57 W
Input power			
Total Power	11.95 V	4.588 A	54.83 W

Total Dissipation (IRPS5401 + inductors)	6.26 W
System Efficiency including loss of VCC LDO	88.6%

The GUI estimates the IRPS5401 efficiency for the same load conditions to be ~88%. The same as the measured efficiency.

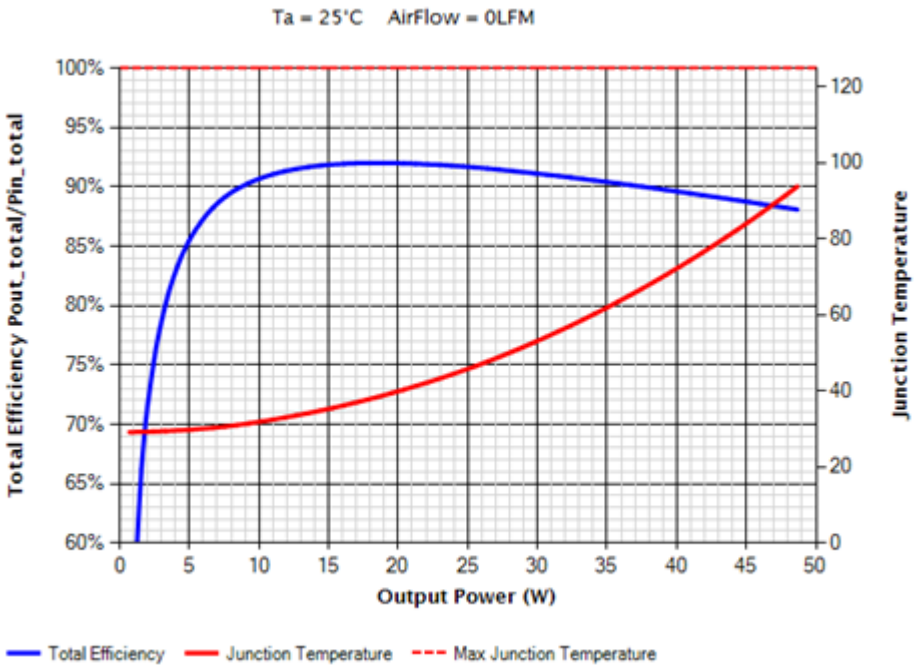


Figure 51 Total efficiency curve

To determine the power loss of the IRPS5401 (for thermal impedance calculation), the inductor core and winding losses need to be removed from the total power dissipation shown above.
Inductor losses calculated from Coiltronic website; http://www.coilcraft.com/xal60xx.cfm and http://www.coilcraft.com/xal4000.cfm

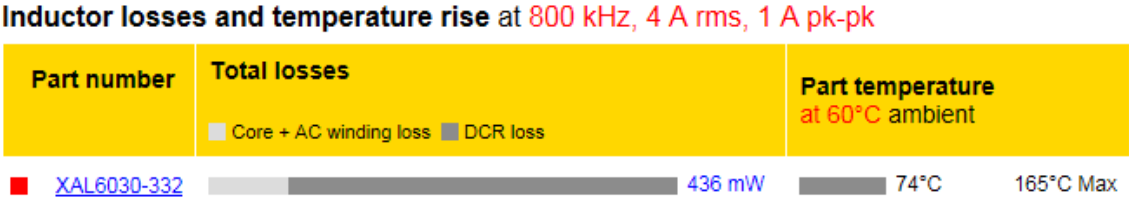


Figure 52 Total inductor losses on SWITCHER C and D

The inductors used in the 5 V C+D output are dissipating 0.436 W.

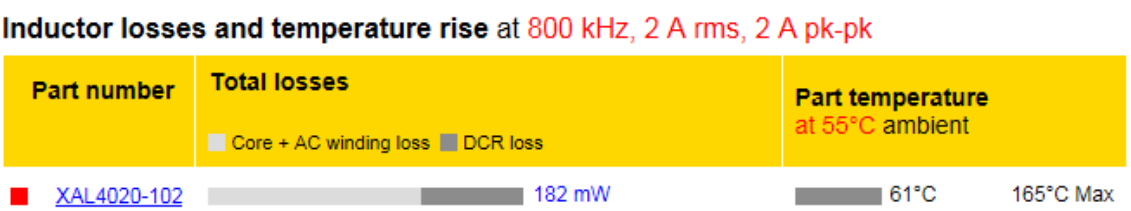


Figure 53 Total inductor losses on SWITCHER A and B

SW-A and B are being over driven for VOUT to get as much power dissipation as possible. The inductors used should only be used up to ~1.2 V for acceptable core loss. The Manufacturer's data shows 0.182 W per inductor for SW-A and B in this test (~66% is core loss).

Given this information, the total power dissipation in the IRPS5401 is (6.26 W-(2*0.436 W)-(2*0.182 W)) 5.024 W. This includes the 0.52 W (12 V*0.043 A) dissipated in the internal LDO + gate drive + controller.

The reported junction temperature for SW-A and SW-B is 77°C. The reported junction temperature for SW-C+D is 81°C. In this application nearly all the heat is being transferred to and dissipated in the copper of the PCB so the junction temperature and case temperature are essentially the same.
The 1st IR image shows that the case in the area of C/D FETs is at 81°C. The temperature rise above ambient is (81°C - 25°C) 56°C. The thermal impedance of the IRPS5401 for this particular thermal solution with no airflow is 56°C/5.024W = 11.1°C/W. The measured case temperature (81°C) is better than the GUI estimate or 93°C.

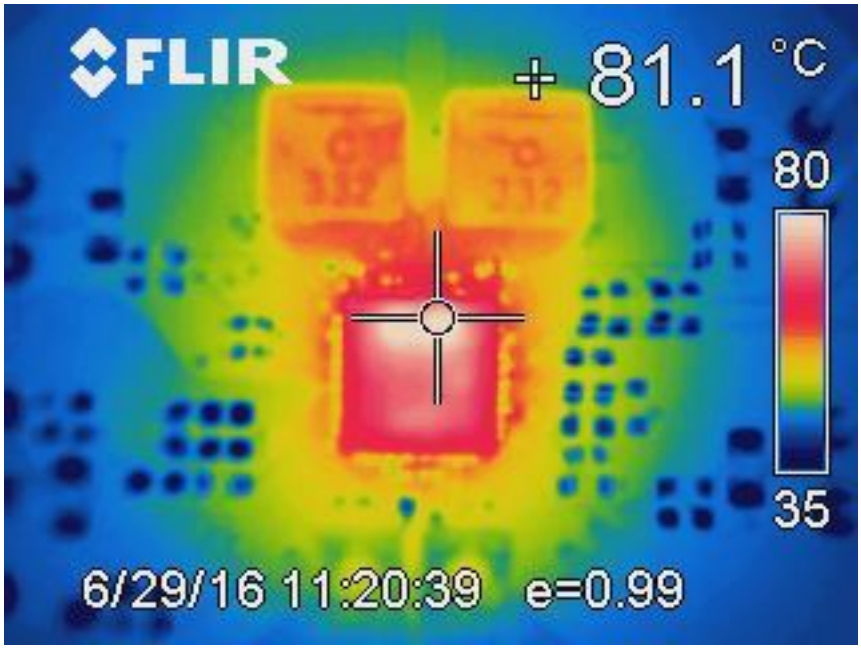


Figure 54 Reported junction temperature

The thermal image of the entire board shows the PCB in the area of the IRPS5401 is ~60˚C. The thermal impedance from case (and junction) to PCB is (81°C - 60°C) 21°C/5.024W ~ 4°C/W.

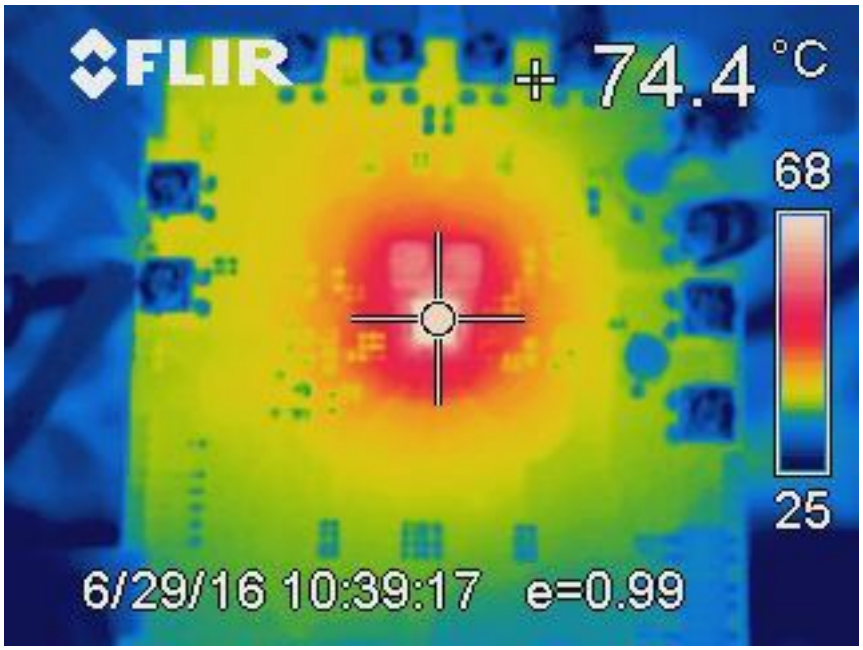


Figure 55 Thermal image of entire board

10 DB295 and DB296 Details

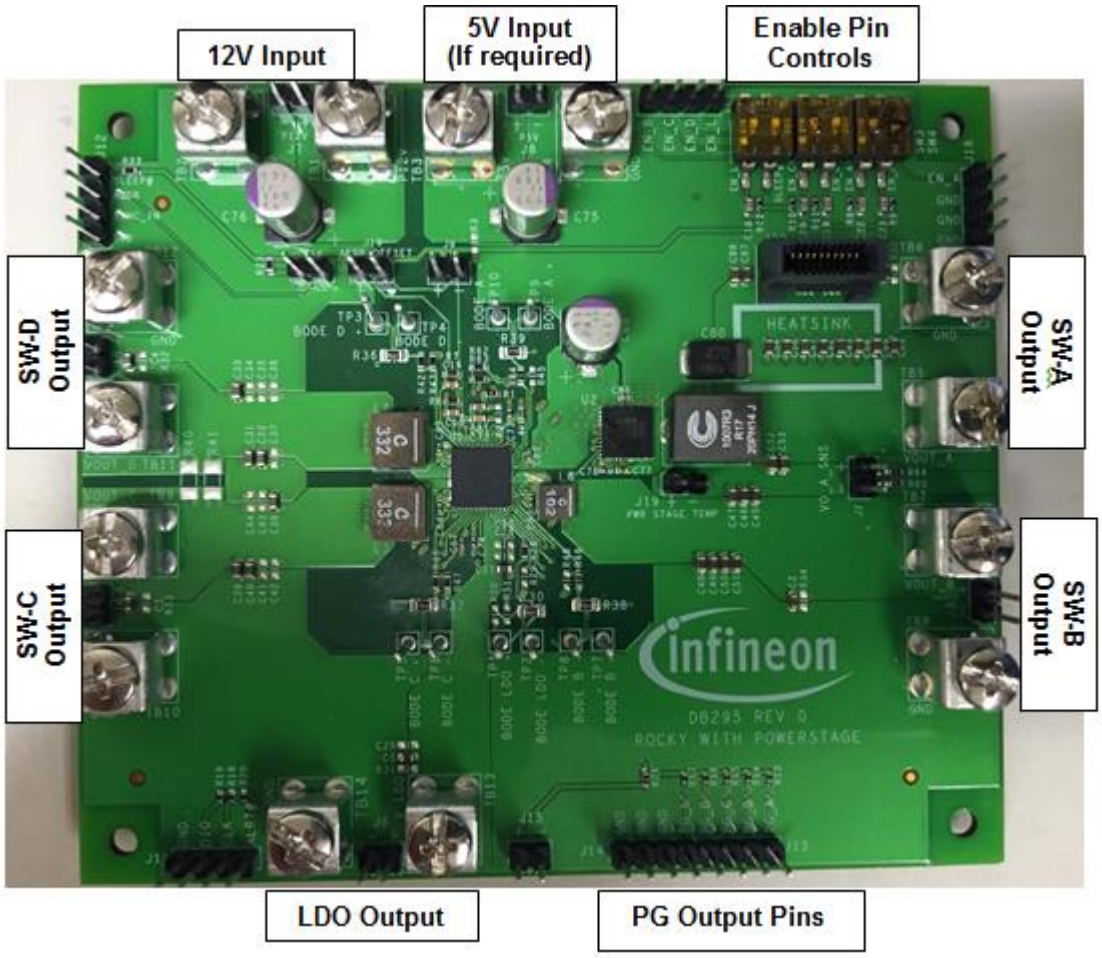
Two demo boards have been developed to show the operation of the IRPS5401. DB295 has SW-A configured with an external power stage and DB296 is configured with SW-A as an internal switcher. Both boards have four switching outputs plus the LDO. Both boards are configured at the factory to operate with just the 12 V input. The internal LDO is utilized to power the VCC for the IRPS5401 and the gate drive voltage VDRV. The LDO is in TRACKING mode running off of SW-B.

So with the application of 12 V (VIN > 6 V) and asserting the enable pins high, the DB295/6 will produce 5 outputs.
There are resistor stuff options that allow VCC to be connected to an external 5 V so the VIN pins can be used down to 1.2 V.

There is a resistor stuffing option at each VIN_x pin that allows VIN to be connected to 12 V or 5 V independently.
There is a resistor stuffing option so the LDO can be tied to 5V external and used in Source Only Mode

Table 5 DB295/6 test points

TB1	12 V input	TB13	VO_LDO	J9	MTP Offset
TB2	GND	TB14	GND	J10	ADDR Offset
TB3	5 V input	TP1,2	LDO Bode	J11	I2C Header
TB4	GND	TP3,4	SW-D Bode	J12	SLEEP#, SYNC
TB5	VO_A	TP5,6	SW-C Bode	J13	PG_A to PG_D
TB6	GND	TP7,8	SW-B Bode	J14	GND + PG_LDO
TB7	VO_B	TP9,10	SW-A Bode	J15	VDDIO Sense (or input)
TB8	GND	J2	VO_A sense	J16	Pull up on ADDR_PROT
TB9	VO_C	J3	VO_B sense	J17	EN_B,C,D,L
TB10	GND	J4	VO_C sense	J18	EN_A + GND
TB11	VO_D	J5	VO_D sense	J19	PS TEMP (DB295 only)
TB12	GND	J6	VO_LDO sense		



The TDA2124x powerstages have only 3.3V compatible EN and PWM inputs. DB295 is designed to tie them to 5V signals. For evaluation purposes this has not been a problem. However, in actual designs the datasheet of TDA2124x parts needs to be obeyed. DB295 can be reworked to accomplish proper signal levels.

R68 needs to be 75kOhm instead of 10kOhm. A 402 Ohm resistor and a 3V Zener diode have to be placed in the PWM path as shown in the schematic.

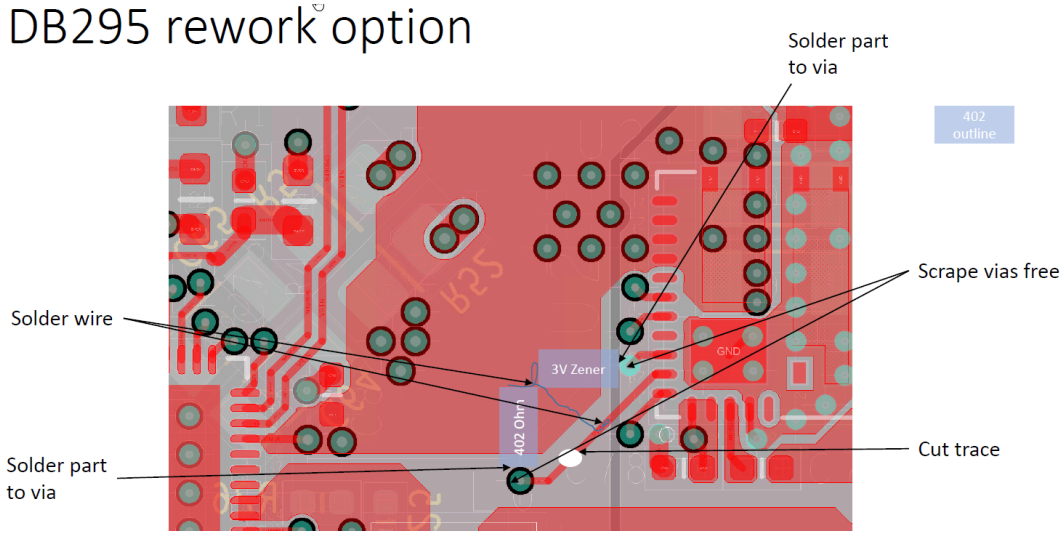


Figure 56 DB295

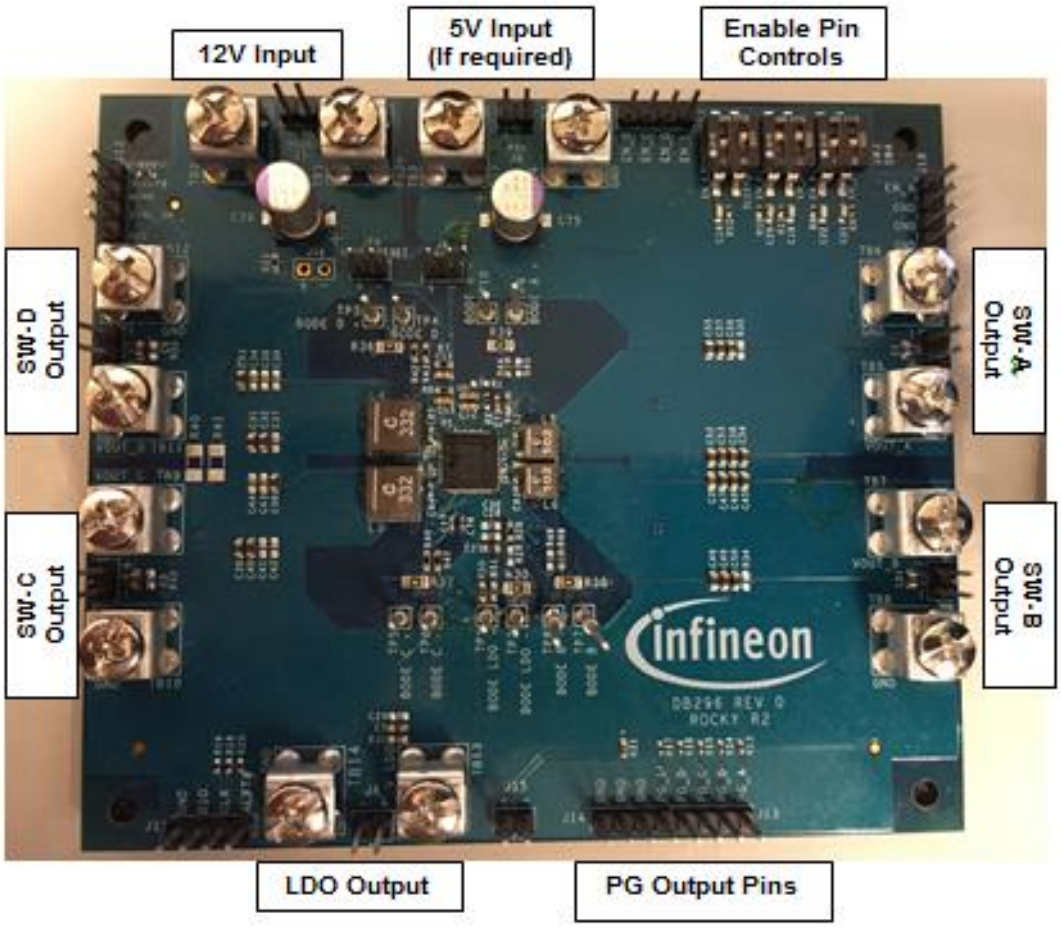


Figure 57 DB296

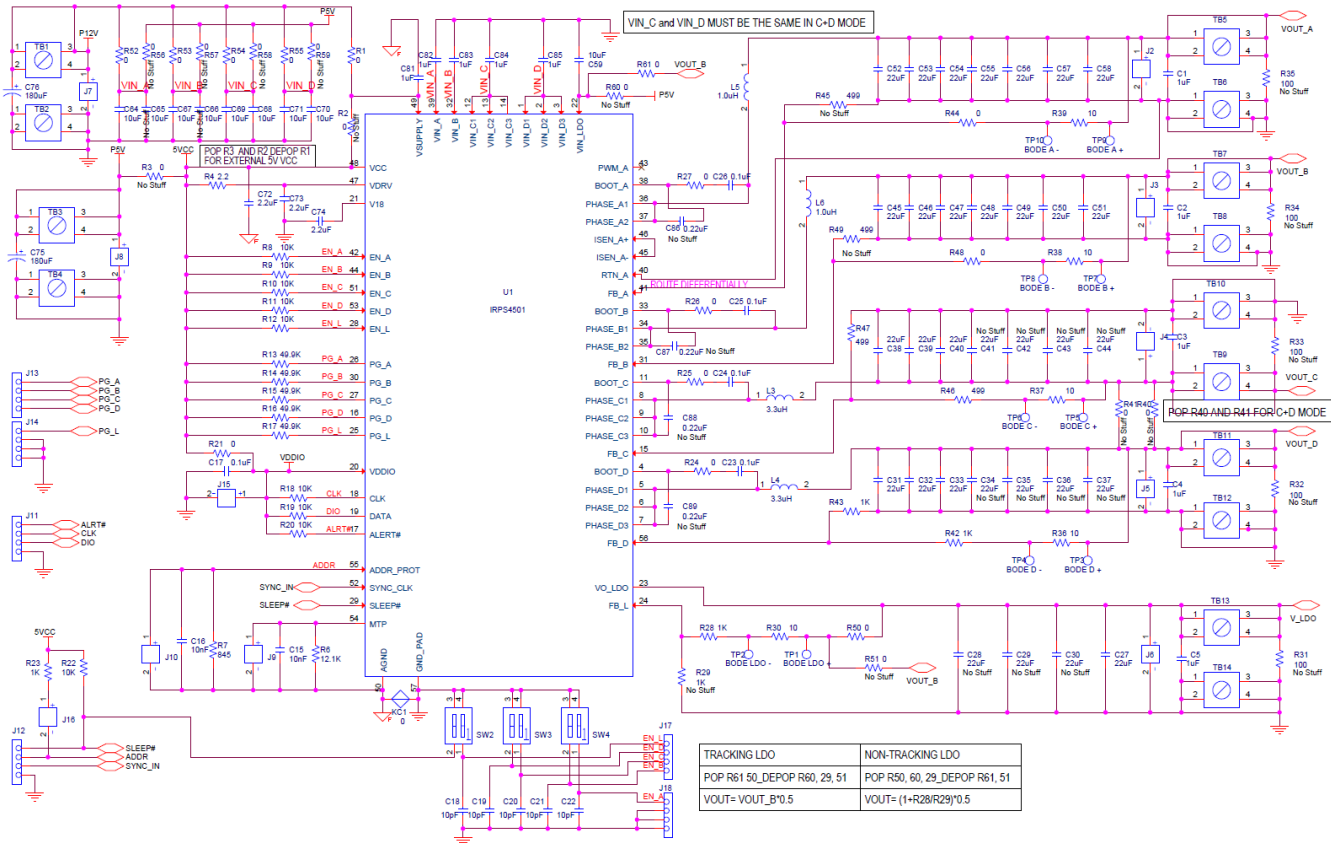


Figure 58 DB296 schematic – SW-A internal FETs

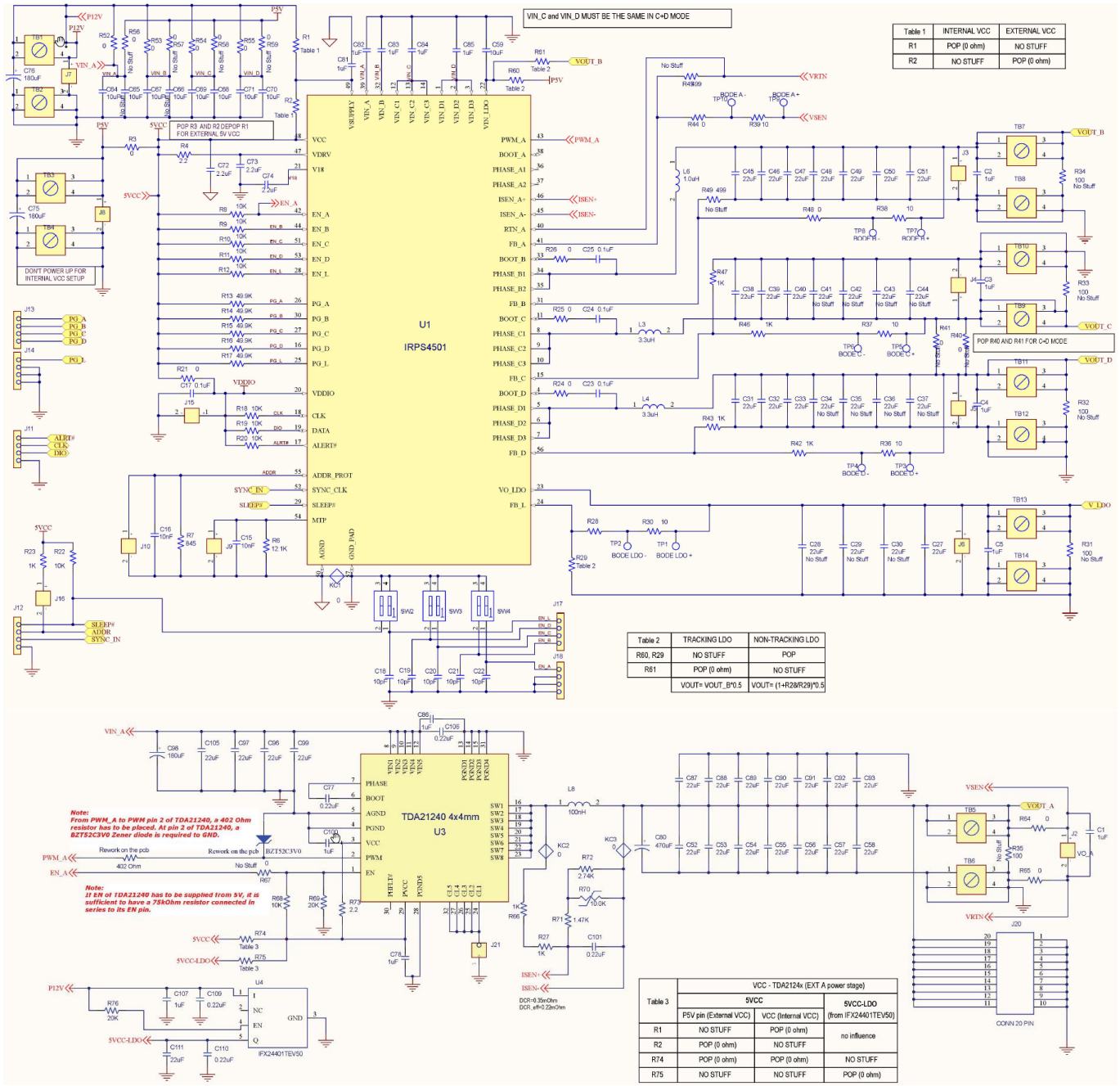


Figure 59 DB295 schematic – SW-A external FETs

11 General Design Recommendations and Advisements

Jitter prevention:

Actual designs are likely not matching the tight layout of the evaluation boards. To prevent noise from entering the EA it is recommended to have a 0402 capacitor footprint located directly at the FB to GND of each respective regulation loop (for SWA it is FB to RTN). Values between 0.1uF and 2.2uF will deliver best results dependent on the board design.

Ground routing:

a. If having more than one IRPS5401 in the system ensure that each IRPS5401 has its own AGND only for the components associated with the particular IC.

b. AGND has to be connected at a single point to GND (ideally directly at the pin). If a 0 Ohm resistor is being used for the purpose of net separation, position it close to the pin.

c. Keep AGND small. There are only a few components tied to it (decoupling of VCC, MTP, ADDR and the resistors for ADDR and MTP).

12 Typical Performance

(Performance data obtained from DB296 and DB295 with IR3555 as PowerStage)

SW-A; 1.0 V @ 100 mA
500mV/div,
TON_RISE = 1 msec
Output Filter ➔1 µH + 7* 22 µF

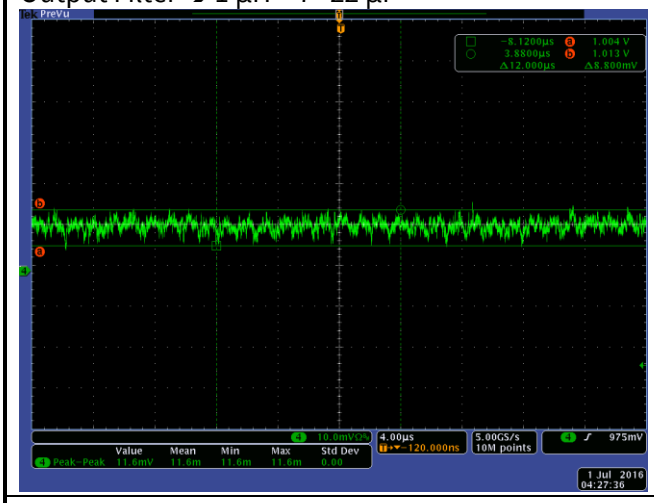
SW-B; 1.2 V @ 100 mA
500 mV/div,
TON_RISE = 1 msec
Output Filter ➔1 µH + 7* 22 µF

SW-C; 2.5 V @ 100 mA
500m V/div,
TON_RISE = 1 msec
Output Filter ➔3.3 µH + 3* 22 µF

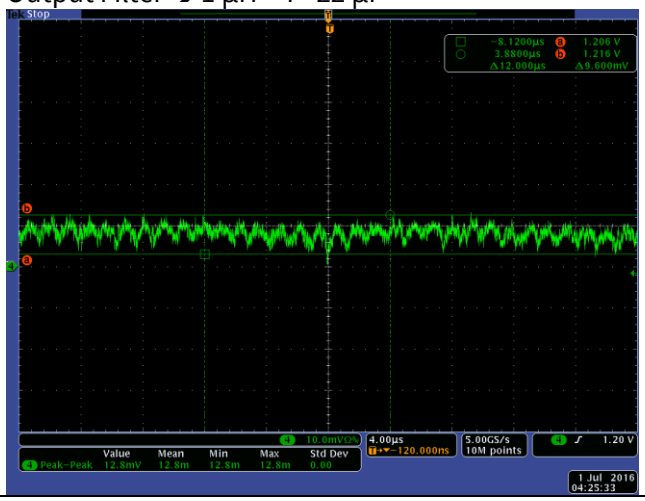
SW-D; 3.3 V @ 100 mA
1 V/div,
TON_RISE = 1 msec
Output Filter ➔3.3 µH + 3* 22 µF

Figure 60 Start-up

SW-A; 1.0 V @ 2 A
10 mV/div, 12 mVp-p
Output Filter ➔1 µH + 7* 22 µF

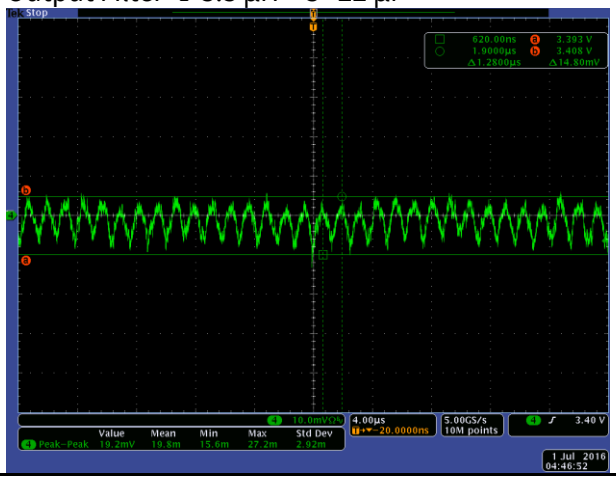


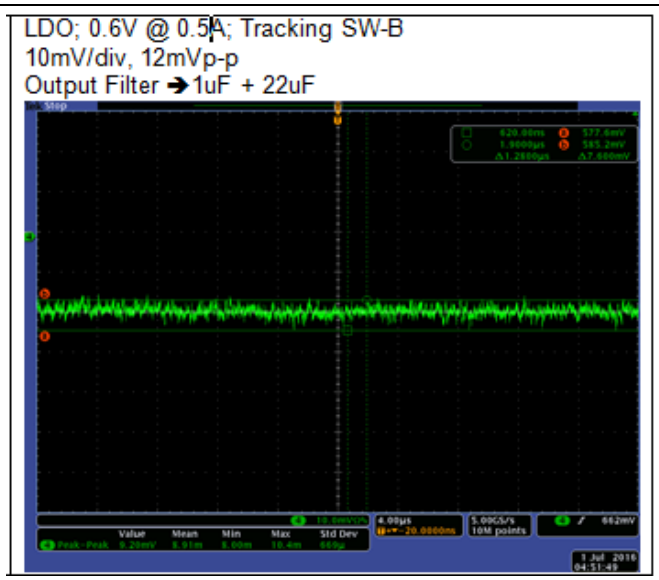
SW-B; 1.2 V @ 2 A
10 mV/div, 13 mVp-p
Output Filter ➔1 µH + 7* 22 µF



SW-C; 1.8 V @ 4 A
10 mV/div, 15 mVp-p
Output Filter ➔3.3 µH + 3* 22 µF

SW-D; 3.3 V @ 4 A
10 mV/div, 20 mVp-p
Output Filter ➔3.3 µH + 3* 22 µF

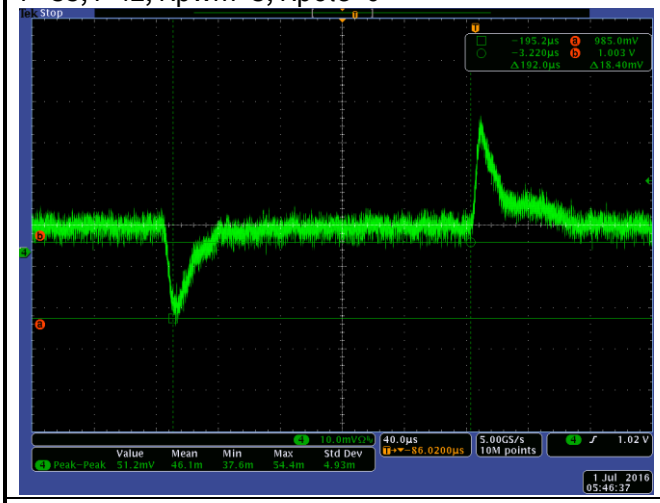




GREEN	VOUT

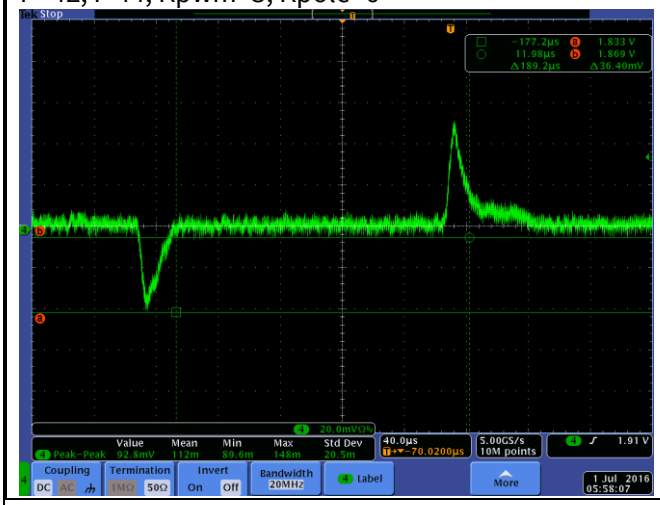
Figure 61 Output ripple

SW-A; 1.0 V @ 1 A Step
10m V/div, 1.8% droop
Output Filter ➔1 µH + 7* 22 µF
P=35, I=42, Kpwm=3, Kpole=6

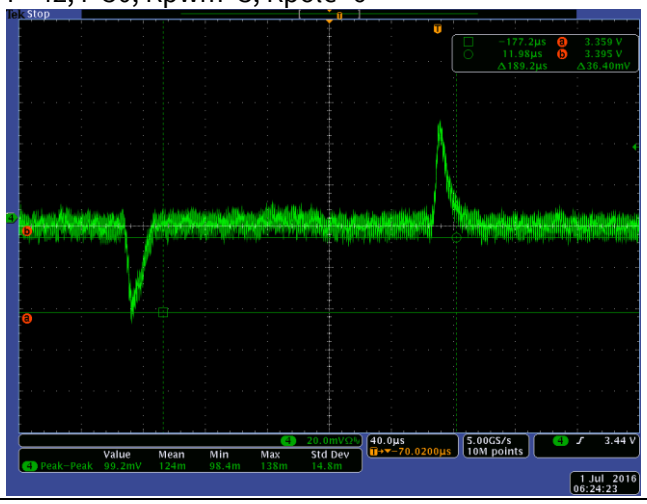


SW-B; 1.2 V @ 1 A Step
10 mV/div, 1.6% droop
Output Filter ➔1 µH + 7* 22 µF
P=36, I=43, Kpwm=3, Kpole=6

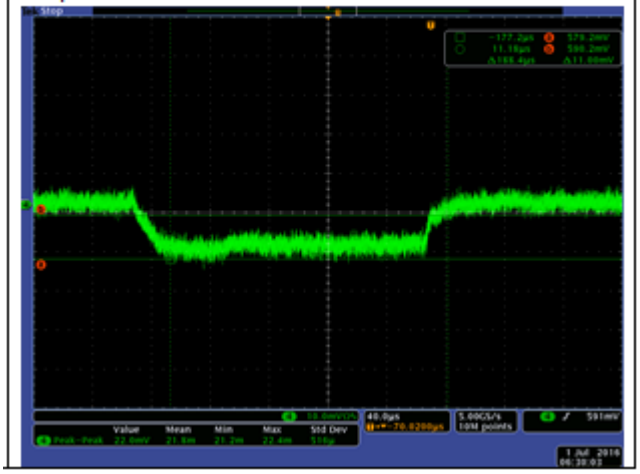
SW-C; 1.8 V @ 1 A Step
20 mV/div, 2% Droop
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=44, Kpwm=3, Kpole=6



SW-D; 3.3 V @ 1 A Step
20 mV/div, 1.1% Droop
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=50, Kpwm=3, Kpole=6



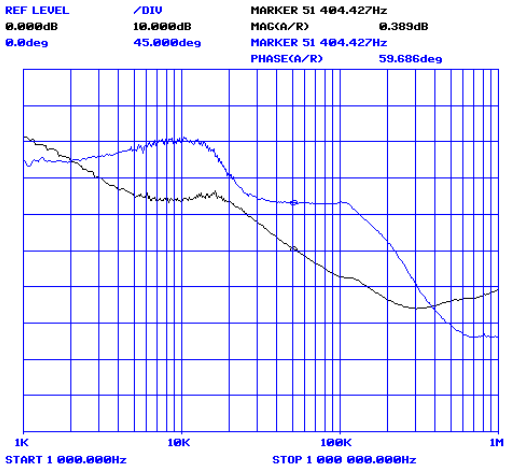
LDO; 0.6V @ 0.2A Step; Tracking SW-B
10mV/div, 1.8% droop
Output Filter ➔1uF + 22uF



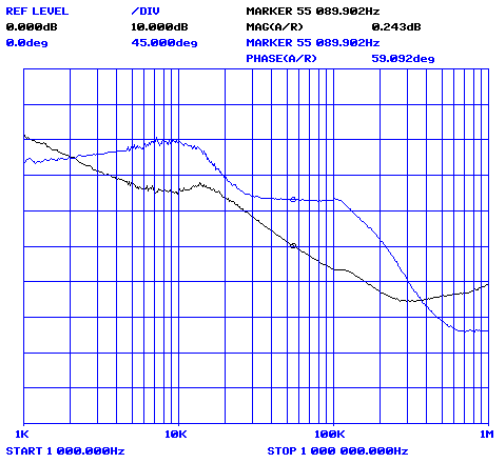
GREEN	VOUT

Figure 62 Transient response

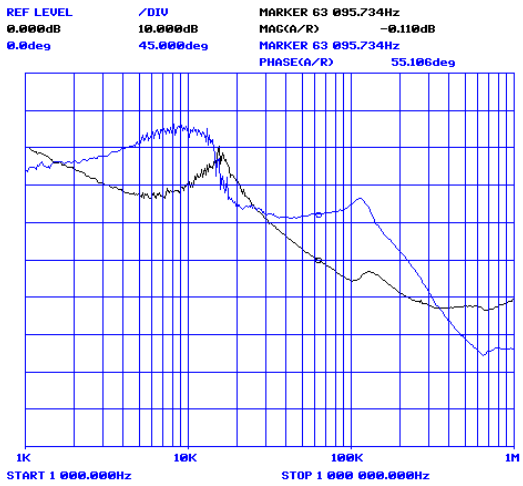
SW-A; 1.0 V @ 1 A
Fco = 51 kHz, PM = 59°
Output Filter ➔1 µH + 7* 22 µF
P=35, I=42, Kpwm=3, Kpole=6



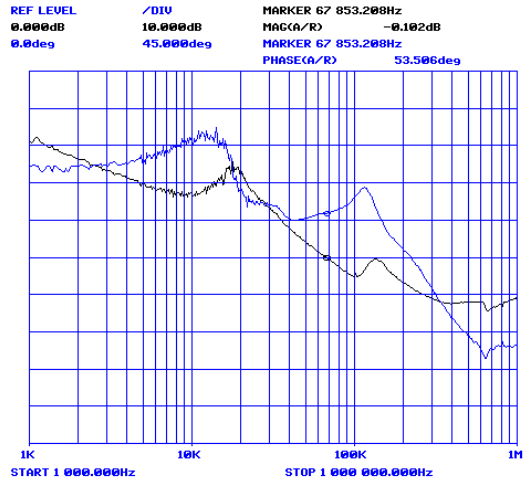
SW-B; 1.2 V @ 1 A
Fco = 55 kHz, PM = 59°
Output Filter ➔1 µH + 7* 22 µF
P=36, I=43, Kpwm=3, Kpole=6



SW-C; 1.8 V @ 2 A
Fco = 63 kHz, PM = 55°
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=44, Kpwm=3, Kpole=6



SW-D; 3.3 V @ 2 A
Fco = 67 kHz, PM = 53°
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=50, Kpwm=3, Kpole=6



LDO; 0.6 V @ 0.5 A; Tracking SW-B
Fco = 200 kHz, PM = 92°
Output Filter ➔1 µF + 22 µF

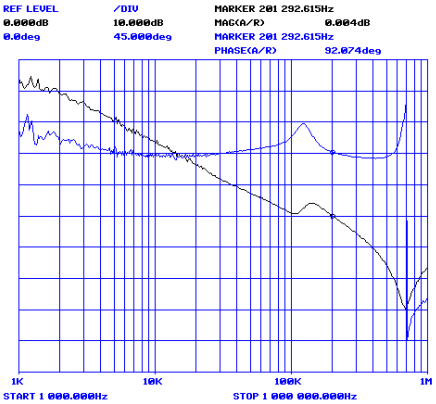
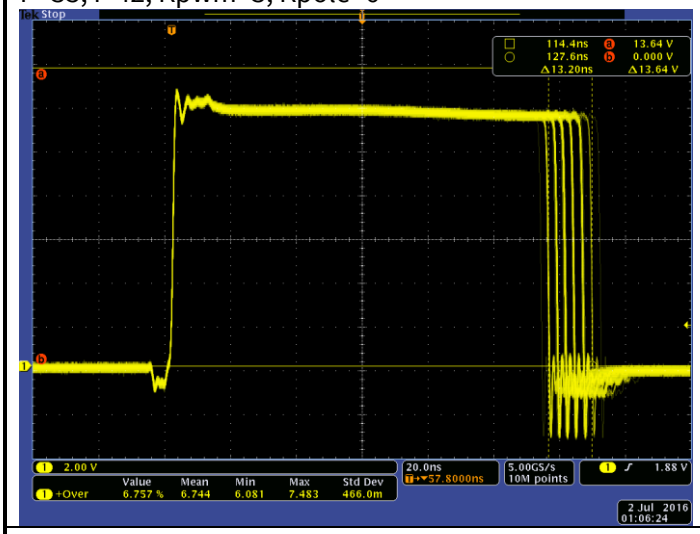
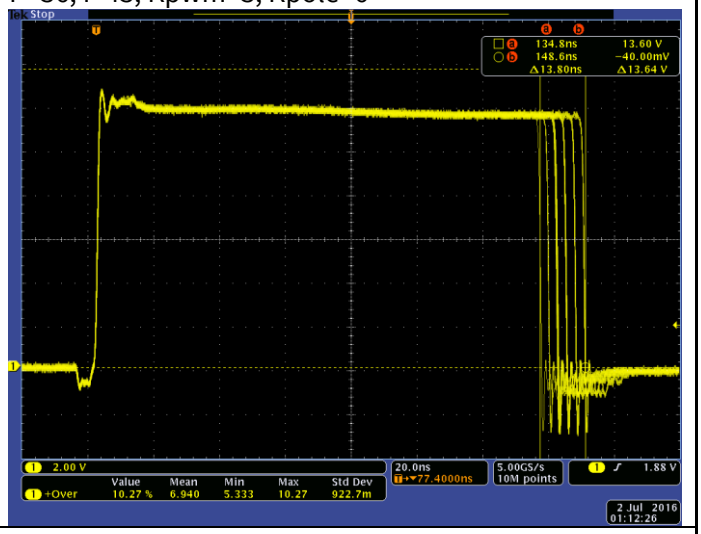


Figure 63 Bode plots

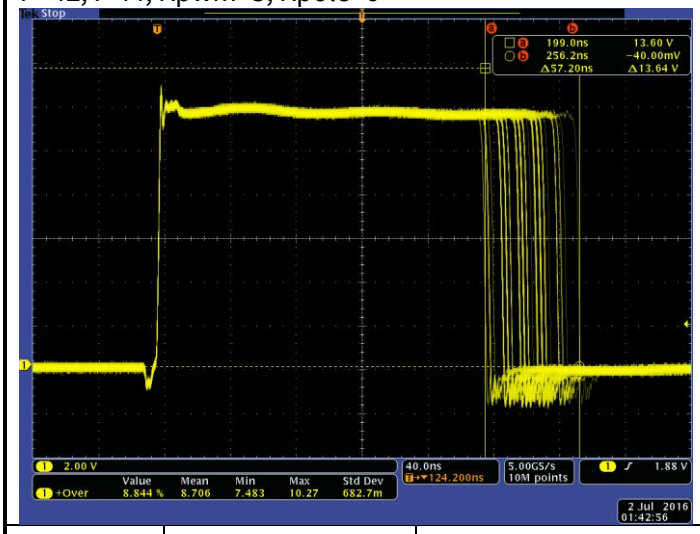
SW-A; 1.0 V @ 2 A
2 V/div, Vpeak = 12.6 V
Jitter=11 nsec
Output Filter ➔1 µH + 7* 22 µF
P=35, I=42, Kpwm=3, Kpole=6



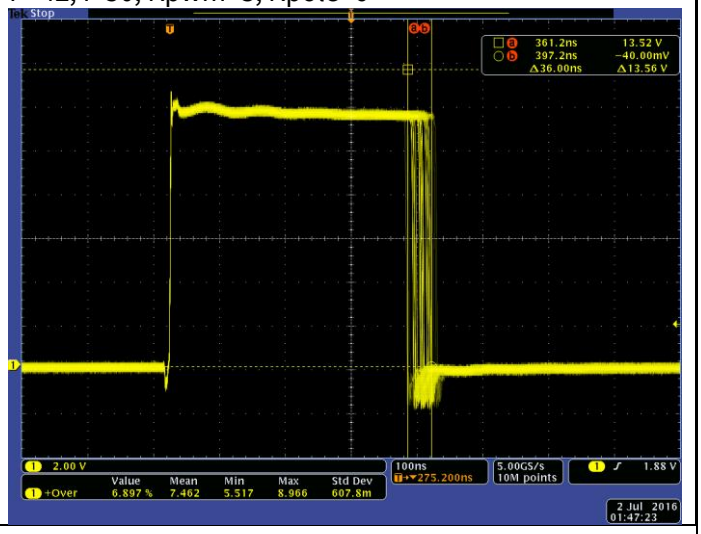
SW-B; 1.2 V @ 2 A
2 V/div, Vpeak = 12.6 V
Jitter = 11 nsec
Output Filter ➔1 µH + 7* 22 µF
P=36, I=43, Kpwm=3, Kpole=6



SW-C; 1.8 V @ 4 A
2 V/div, Vpeak = 12.7 V
Jitter = 57 nsec
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=44, Kpwm=3, Kpole=6



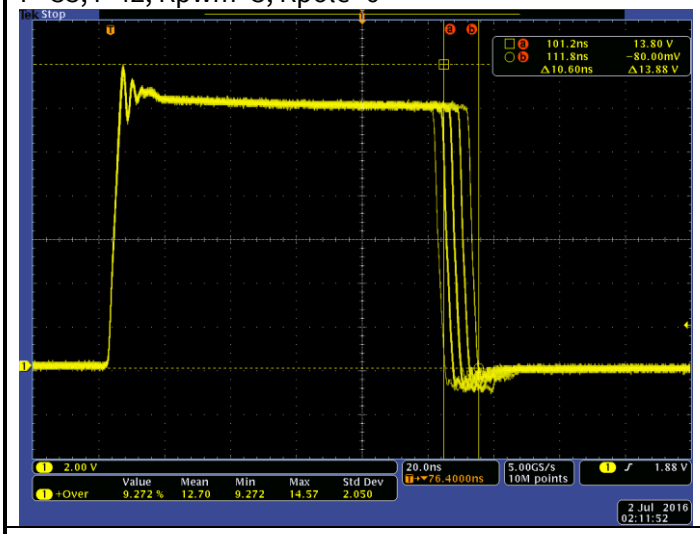
SW-D; 3.3 V @ 4 A
2 V/div, Vpeak = 12.6 V
Jitter = 36 nsec
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=50, Kpwm=3, Kpole=6



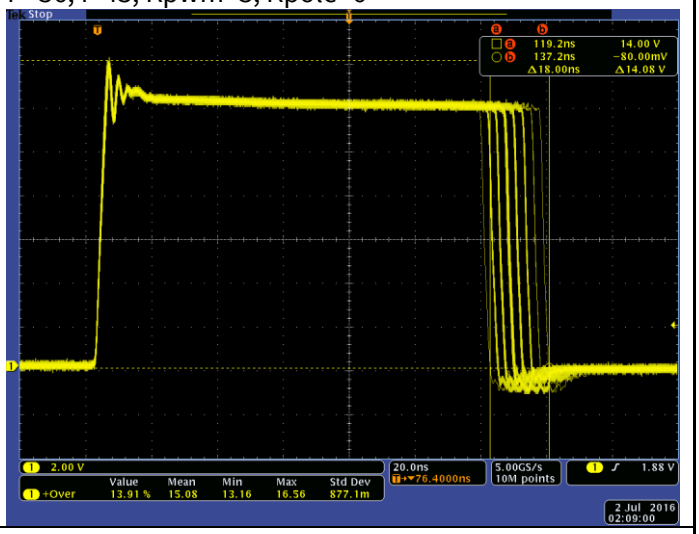
YELLOW	**SW-NODE**

Figure 64 Switch node peak and jitter (Max load)

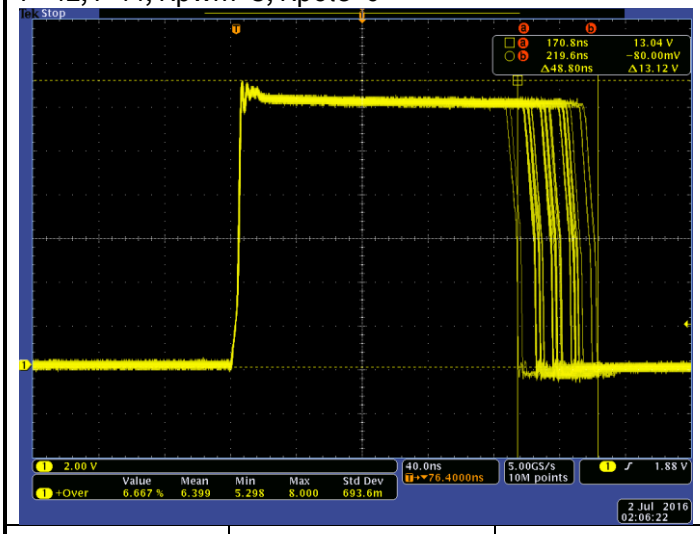
SW-A; 1.0 V @ 0 A
2 V/div, Vpeak = 13.8 V
Jitter = 17 nsec
Output Filter ➔1 µH + 7* 22µF
P=35, I=42, Kpwm=3, Kpole=6



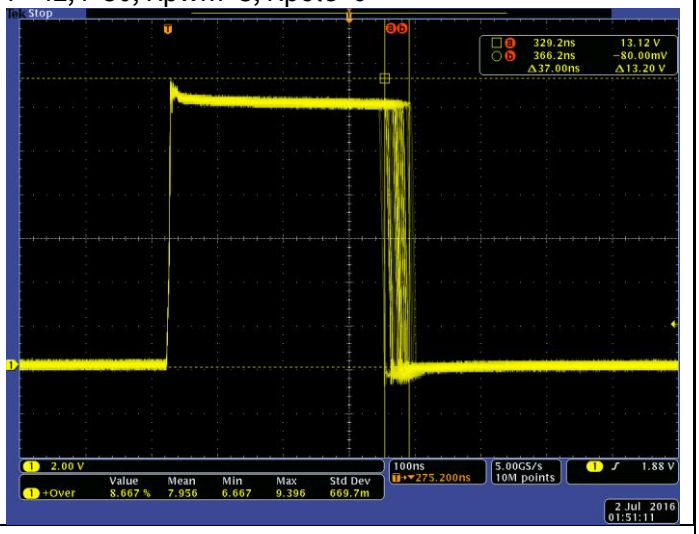
SW-B; 1.2 V @ 0 A
2 V/div, Vpeak = 14.0 V
Jitter = 18 nsec
Output Filter ➔1 µH + 7* 22 µF
P=36, I=43, Kpwm=3, Kpole=6



SW-C; 1.8 V @ 0 A
2 V/div, Vpeak = 13.1 V
Jitter = 48 nsec
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=44, Kpwm=3, Kpole=6



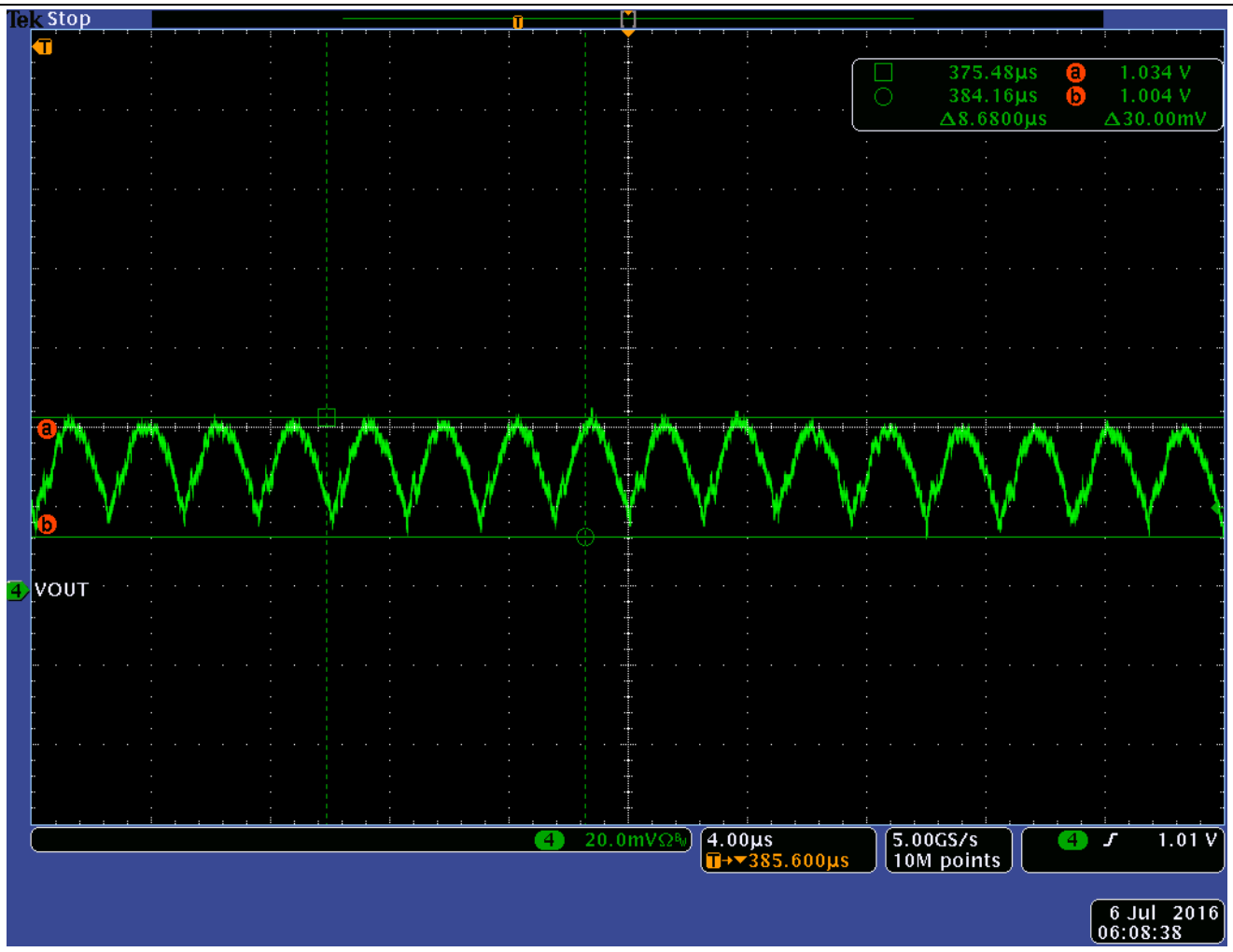
SW-D; 3.3 V @ 0 A
2 V/div, Vpeak = 13.1 V
Jitter = 17 nsec
Output Filter ➔3.3 µH + 3* 22 µF
P=42, I=50, Kpwm=3, Kpole=6



YELLOW	**SW-NODE**

Figure 65 Switch node peak and jitter (0 A load)

EXT SW-A➔ DB295



GREEN = VOUT

Figure 66 Output ripple (VIN = 12 V, VOUT = 1 V, Load = 40 A, fsw = 500 kHz)

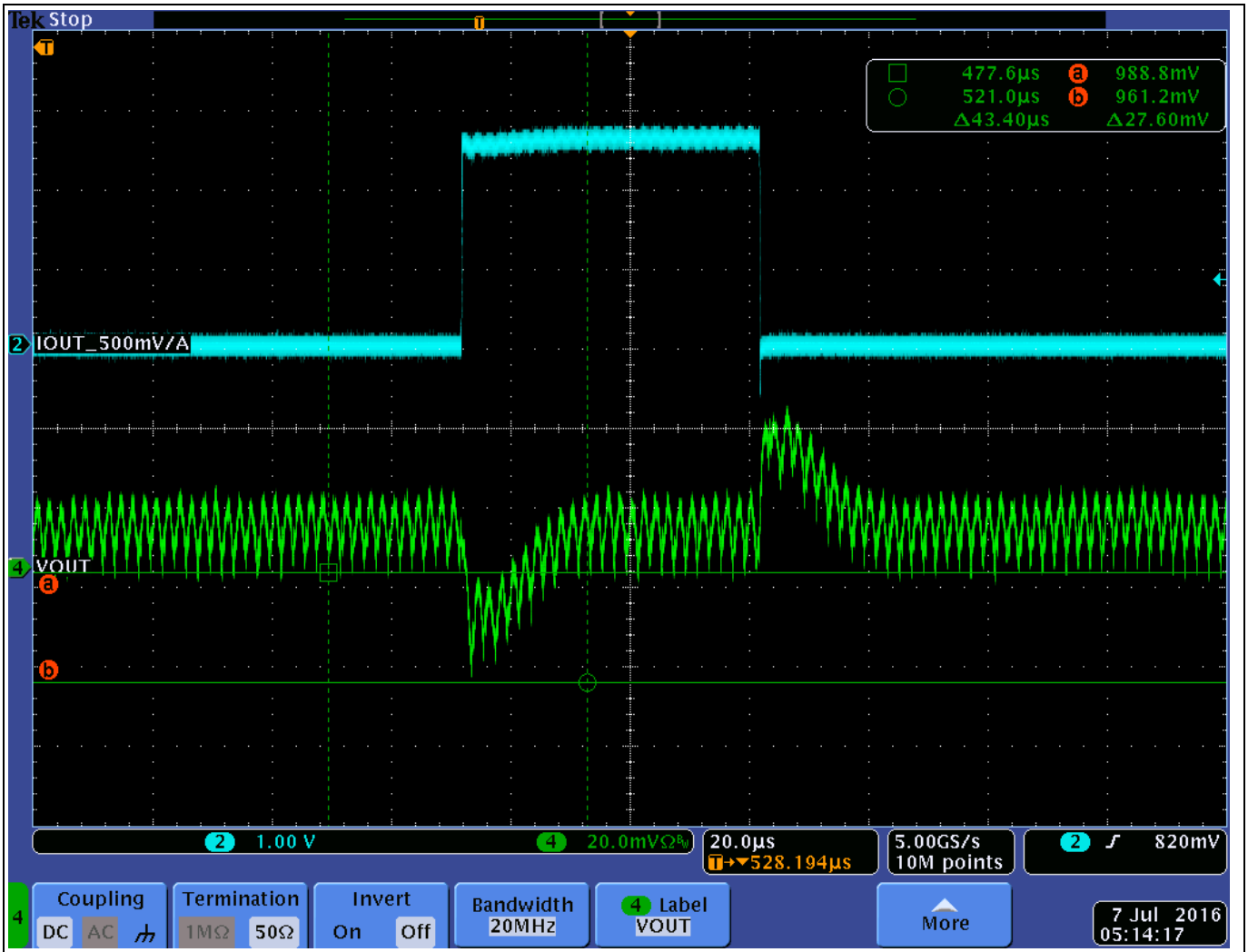
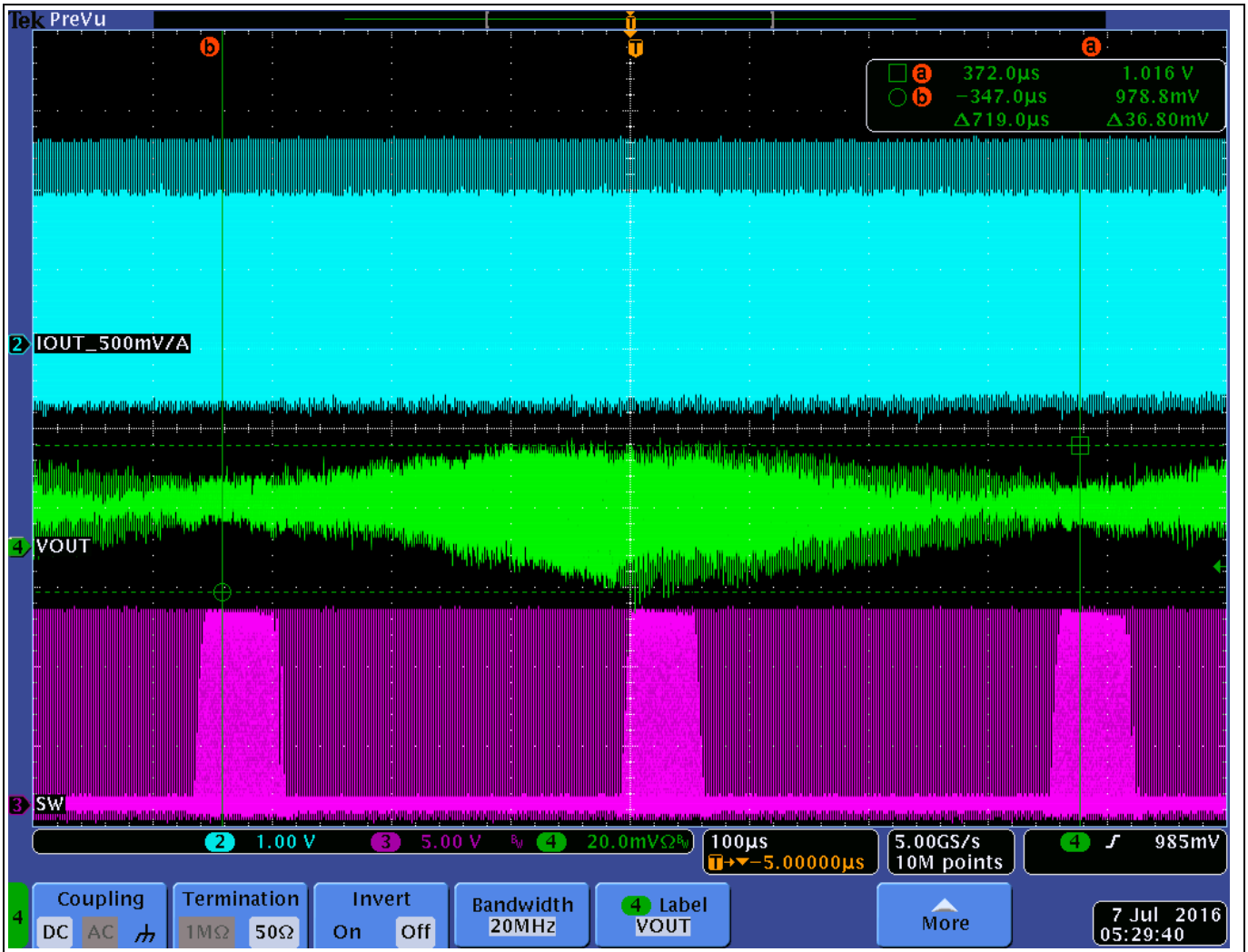


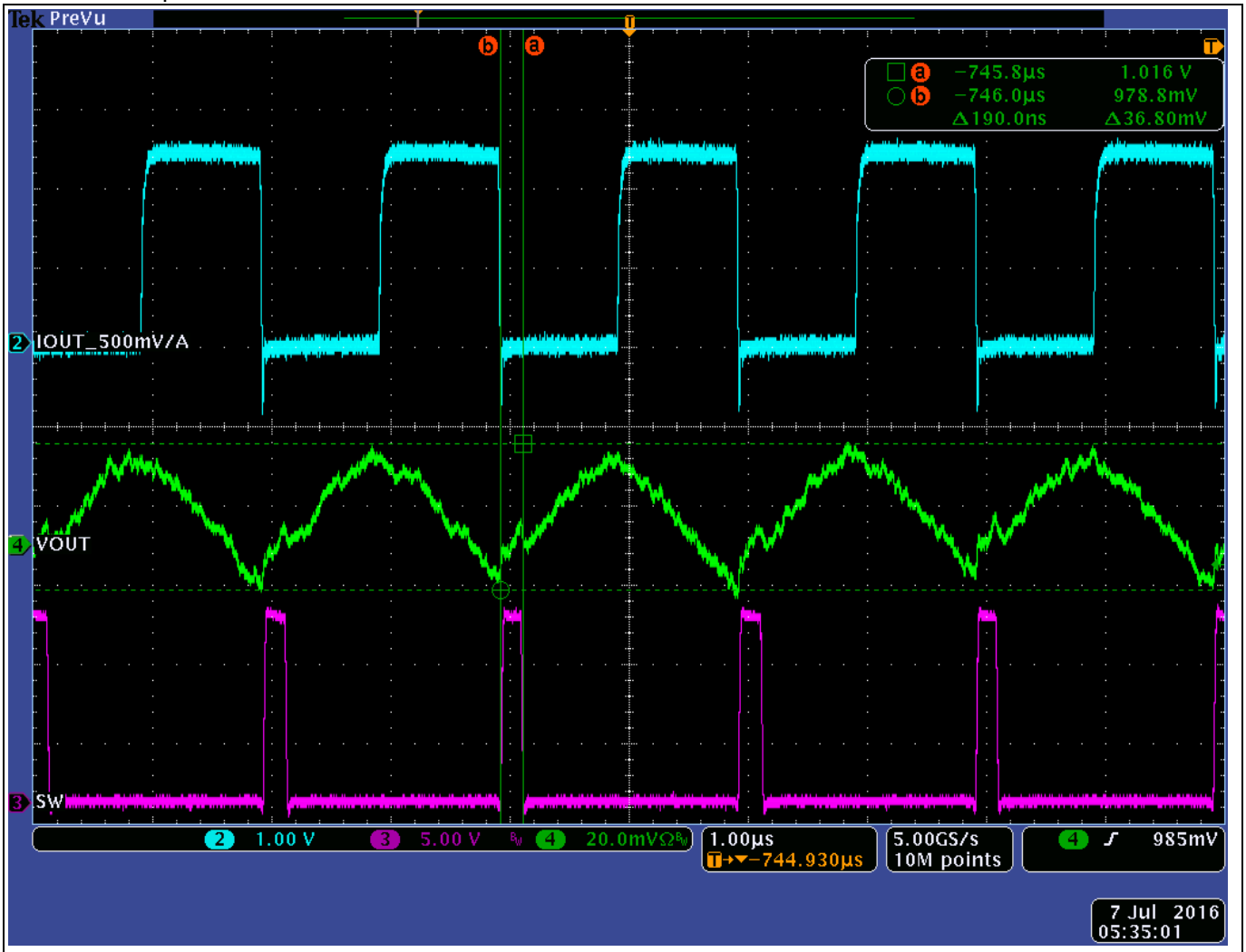
Figure 67 Mini slammer 5 A pulse (250 A/µsec) with 20 A DC load, 2kHz, 10% DC



BLUE = IOUT, GREEN = VOUT, CYAN = SW-NODE

Figure 68 Load REP RATE = 500 kHz, 50% DC, 500 kHz fsw, 1400 Hz beat frequency

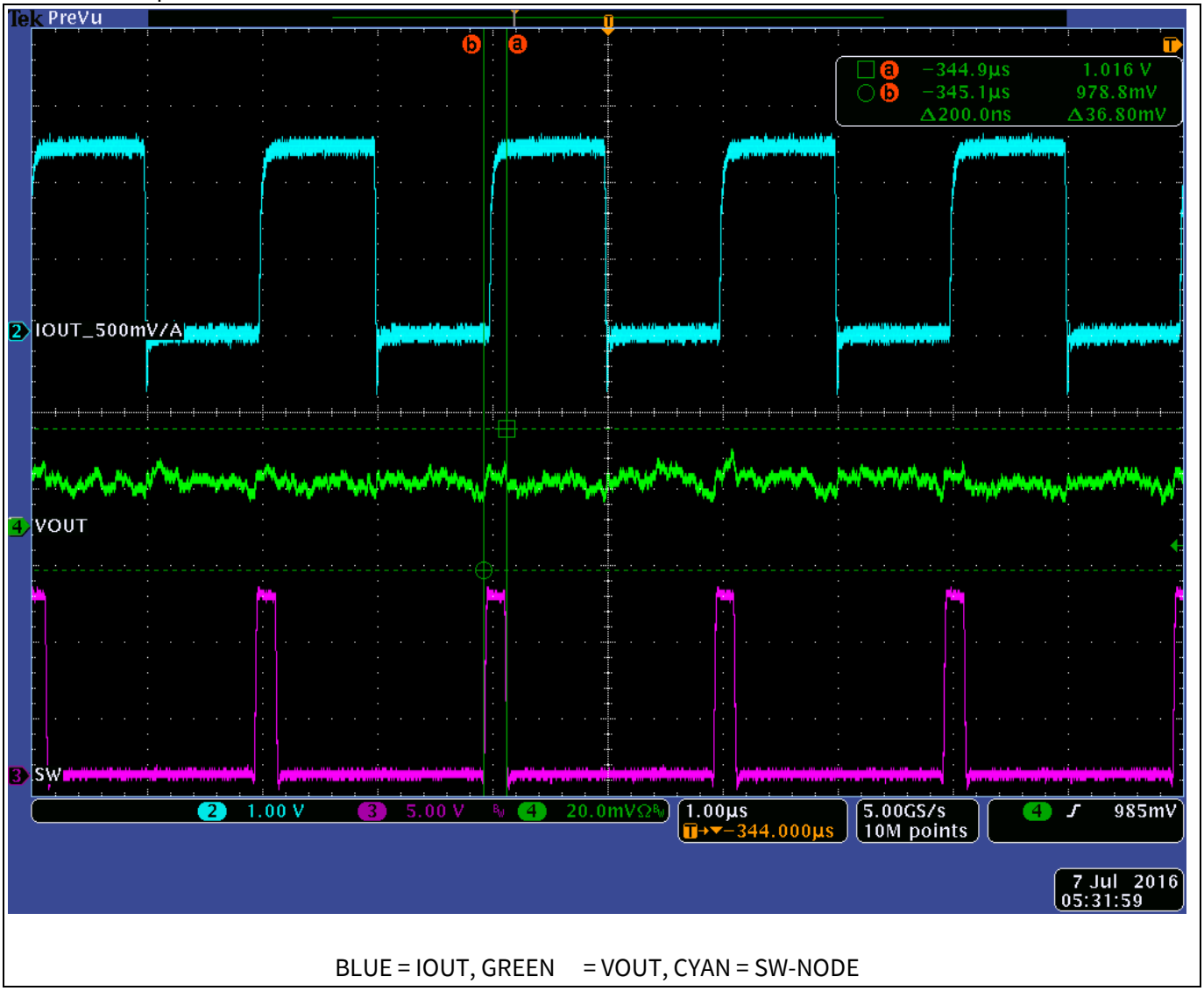
Zoom in on MAX Peak to Peak Ripple
The SW NODE pulse occurs at the end of the MAX load time



BLUE = IOUT, GREEN = VOUT, CYAN = SW-NODE

Figure 69 Max peak to peak ripple

Zoom in on MIN Peak to Peak Ripple
The SW NODE pulse occurs at the start of the MAX load time



BLUE = IOUT, GREEN = VOUT, CYAN = SW-NODE

Figure 70 Min peak to peak ripple

Efficiency of IRPS5401 + IR3555

IRPS5401 in C+D mode with VOUT_COMMAND = 3.3 V and load set to 8 A. SW_A set to 1 V with 40 A load
Total Input Power is 78.48 W. ➔(VIN=11.92*6.55 A+5.00 V*0.082 A)
Total Output Power is 66.87 W. ➔(VOUT = 1.016 V*39.97 A+3.356 V*7.96 A)
Total System Efficiency = 85.4%. The demo board is dissipating 11.6 W with a 75°C rise at the IR3555
The IRPS5401 has a case temperature of 83°C.

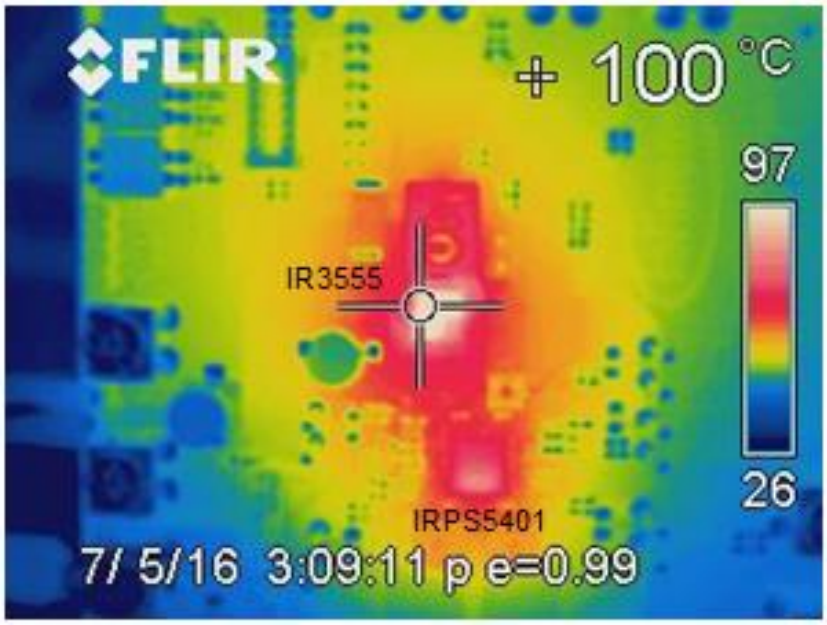


Figure 71 IR3555 thermal image

Efficiency of IRPS5401 + TDA21240

IRPS5401 with TDA21240 including PCB, inductor and capacitor loss
'Peak' -> Peak efficiency
'Max Load' -> Efficiency at maximum load current of 40A
'no VCC' -> Efficiency not taking bias for TDA21240 and IRPS5401 into account
'W/ VCC' -> System efficiency, taking all losses including bias supply for IRPS5401 and TDA21240 into account
Conditions: fsw=800kHz, L=100nH, DCR=0.35mOhm, VCC=5V

	SUMMARY							
	12V in				5V in			
	Peak		Max Load		Peak		Max Load	
VOUT	no VCC	W/ VCC	no VCC	W/ VCC	no VCC	W/ VCC	no VCC	W/ VCC
0.85	88.36%	86.99%	83.14%	82.68%	92.02%	89.83%	81.29%	80.86%
0.72	87.13%	85.72%	81.68%	81.16%	91.04%	88.42%	80.22%	79.73%
0.6	85.61%	83.94%	79.61%	79.02%	90.30%	87.43%	78.84%	78.28%

Revision history

Document version	Date of release	Description of changes
1.0		Initial release
1.1	2018-09-10	Schematic updates, restriction removed, chapters 8 and 13 removed
1.2	2018-12-11	Schematic updates, board errata for DB295, updated board references to TDA2124x family, adding ‘Design Advisements’ section

Figure 72

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