

# 74ALVC574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 3 — 30 April 2021

Product data sheet

## 1. General description

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The 74ALVC574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock input (CP) and an outputs enable input ( $\overline{OE}$ ) are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW to HIGH CP transition.

When pin  $\overline{OE}$  is LOW, the contents of the eight flip-flops is available at the outputs. When pin  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74ALVC574 is functionally identical to the 74ALVC374, but has a different pin arrangement.

## 2. Features and benefits

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- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC574D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC574PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC574BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram

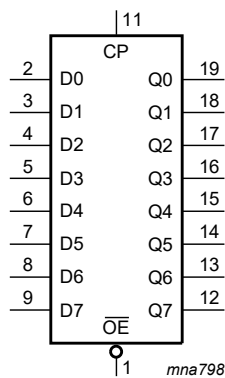


Fig. 1. Logic symbol

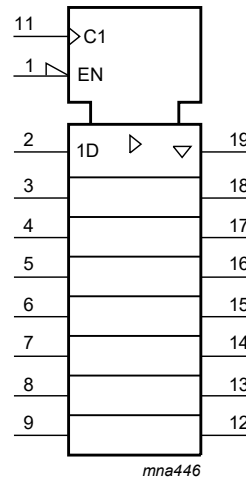


Fig. 2. IEC logic symbol

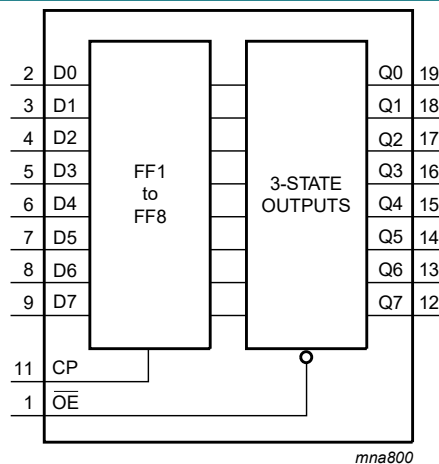


Fig. 3. Functional diagram

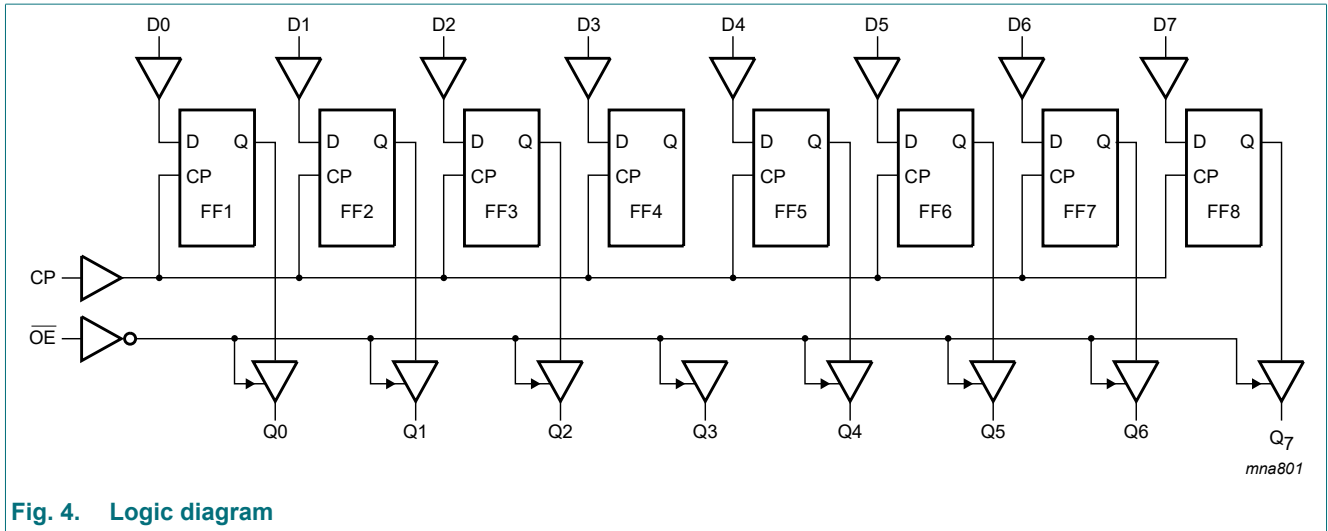


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning

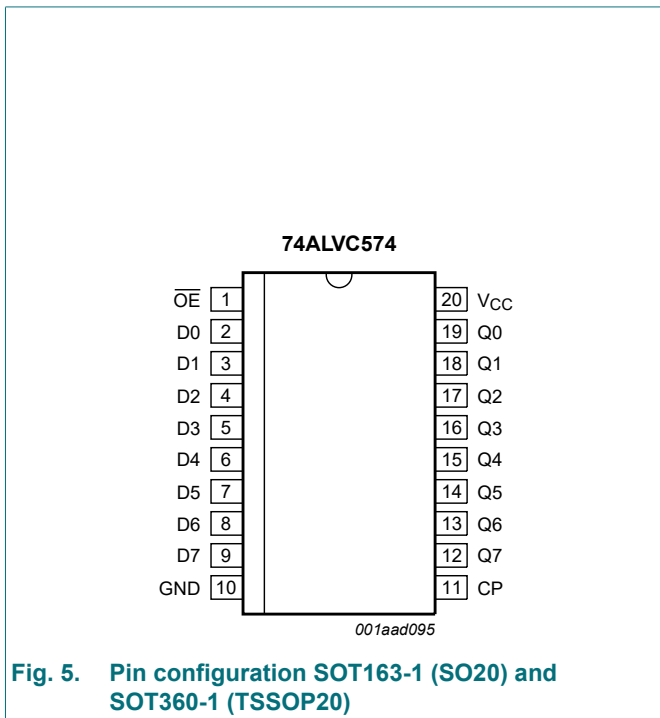


Fig. 5. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)

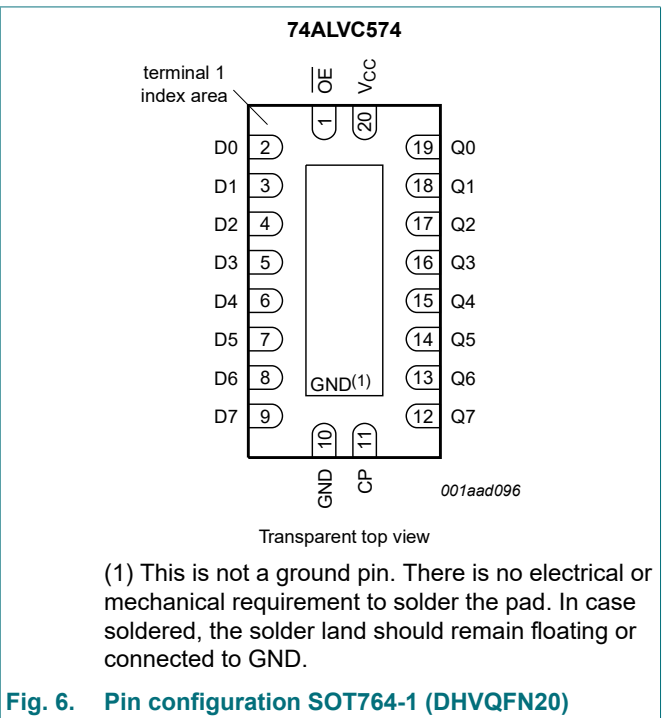


Fig. 6. Pin configuration SOT764-1 (DHVQFN20)

## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
CP	11	clock input (LOW to HIGH, edge-triggered)
$\overline{OE}$	1	output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	3-state flip-flop output
$V_{CC}$	20	supply voltage
GND	10	ground (0 V)

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition;  
 L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition;  
 Z = high-impedance OFF-state;  $\uparrow$  = LOW to HIGH clock transition.

Operating mode	Input			Internal flip-flop	Output Qn
	$\overline{OE}$	CP	Dn		
Load and read register	L	$\uparrow$	l	L	L
	L	$\uparrow$	h	H	H
Load register and disable outputs	H	$\uparrow$	l	L	Z
	H	$\uparrow$	h	H	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state [1]	-0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		power-down mode; $V_{CC} = 0$ V	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +85 $^{\circ}$ C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	output HIGH or LOW state	0	$V_{CC}$	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 3.6 V	-	$\pm 0.1$	$\pm 10$	$\mu$ A
		$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 3.6 V	-	$\pm 0.1$	$\pm 10$	$\mu$ A

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$I_{CC}$	supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.2	10	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; $V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$	-	5	750	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF

[1] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  (unless stated otherwise) and  $T_{amb} = 25\text{ °C}$ .

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

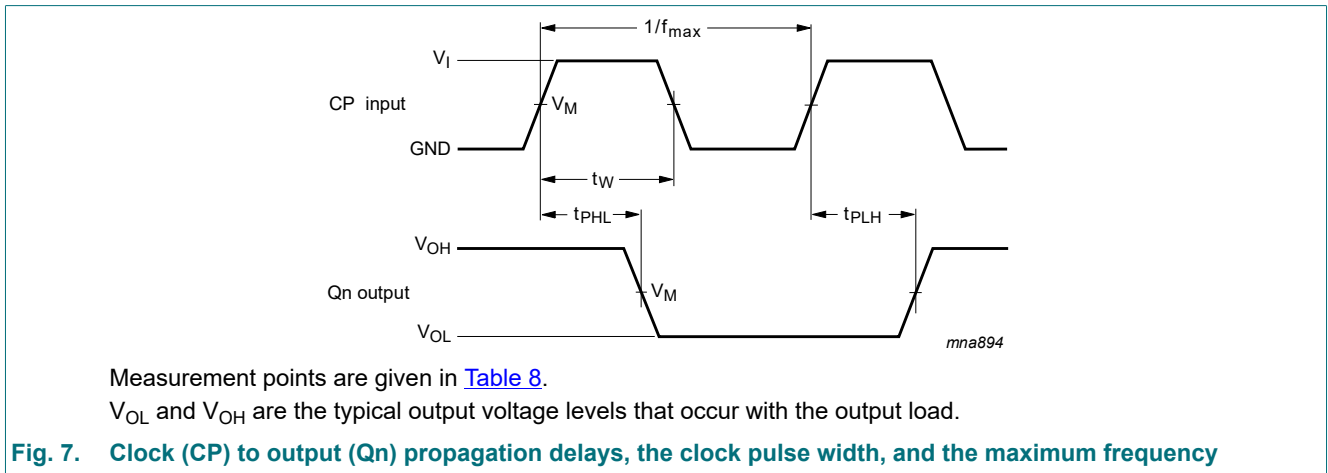
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$t_{pd}$	propagation delay	CP to Qn; see Fig. 7 [2]				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	1.0	3.1	6.4	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.0	2.3	3.9	ns
		$V_{CC} = 2.7\text{ V}$	1.0	2.5	3.6	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.0	2.5	3.6	ns
$t_{en}$	enable time	OE to Qn; see Fig. 8 [2]				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	1.0	3.2	6.4	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.0	2.6	4.5	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.2	4.6	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.0	2.4	4.0	ns
$t_{dis}$	disable time	OE to Qn; see Fig. 8 [2]				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	1.5	3.6	7.0	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	1.0	2.3	4.4	ns
		$V_{CC} = 2.7\text{ V}$	1.5	2.9	4.4	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	1.0	2.8	4.4	ns
$t_W$	pulse width	clock HIGH or LOW; see Fig. 7				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	3.8	1.1	-	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	3.3	0.9	-	ns
		$V_{CC} = 2.7\text{ V}$	3.3	0.8	-	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	3.3	1.2	-	ns
$t_{su}$	set-up time	Dn to CP; see Fig. 9				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	0.8	-0.1	-	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	0.8	0.1	-	ns
		$V_{CC} = 2.7\text{ V}$	0.8	0.3	-	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	0.8	0.0	-	ns
$t_h$	hold time	Dn to CP; see Fig. 9				
		$V_{CC} = 1.65\text{ V}$ to $1.95\text{ V}$	0.8	-0.1	-	ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	0.8	0.1	-	ns
		$V_{CC} = 2.7\text{ V}$	0.8	0.4	-	ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	0.7	-0.1	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
f <sub>max</sub>	maximum frequency	see Fig. 7				
		V <sub>CC</sub> = 2.3 V to 2.7 V	100	200	-	MHz
		V <sub>CC</sub> = 2.7 V	100	200	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	150	300	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V [3]				
		outputs HIGH or LOW state	-	21	-	pF
		outputs 3-state	-	13	-	pF

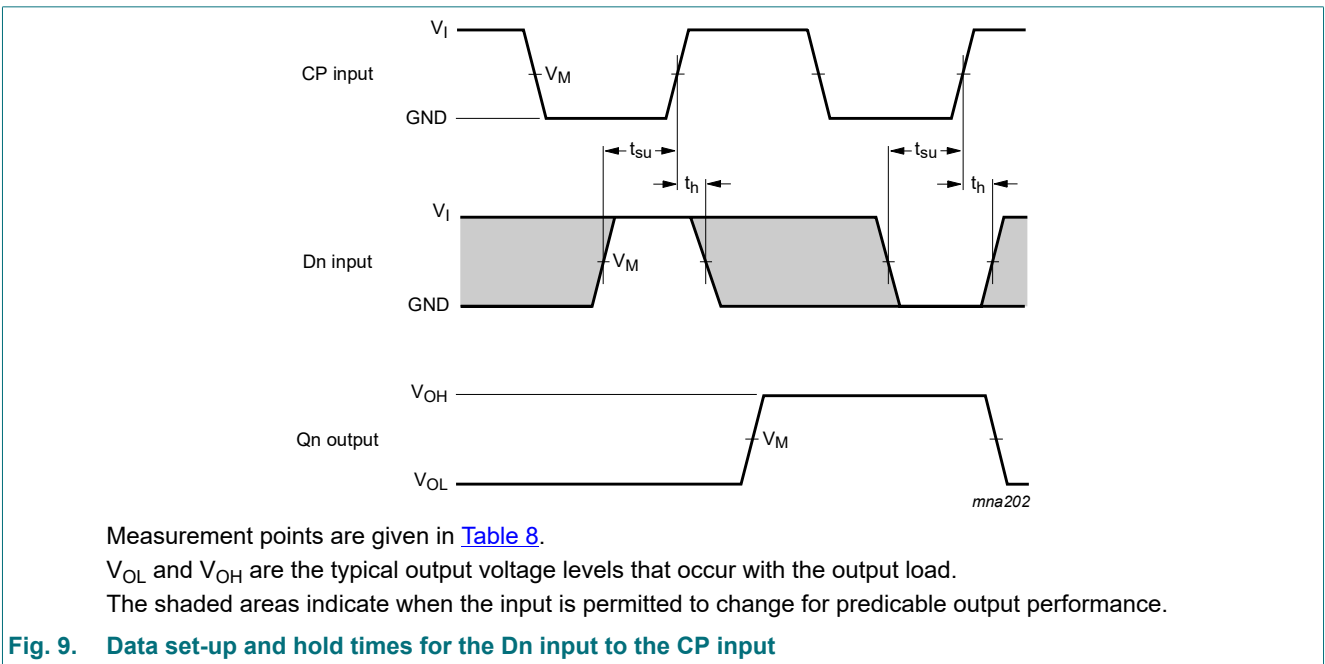
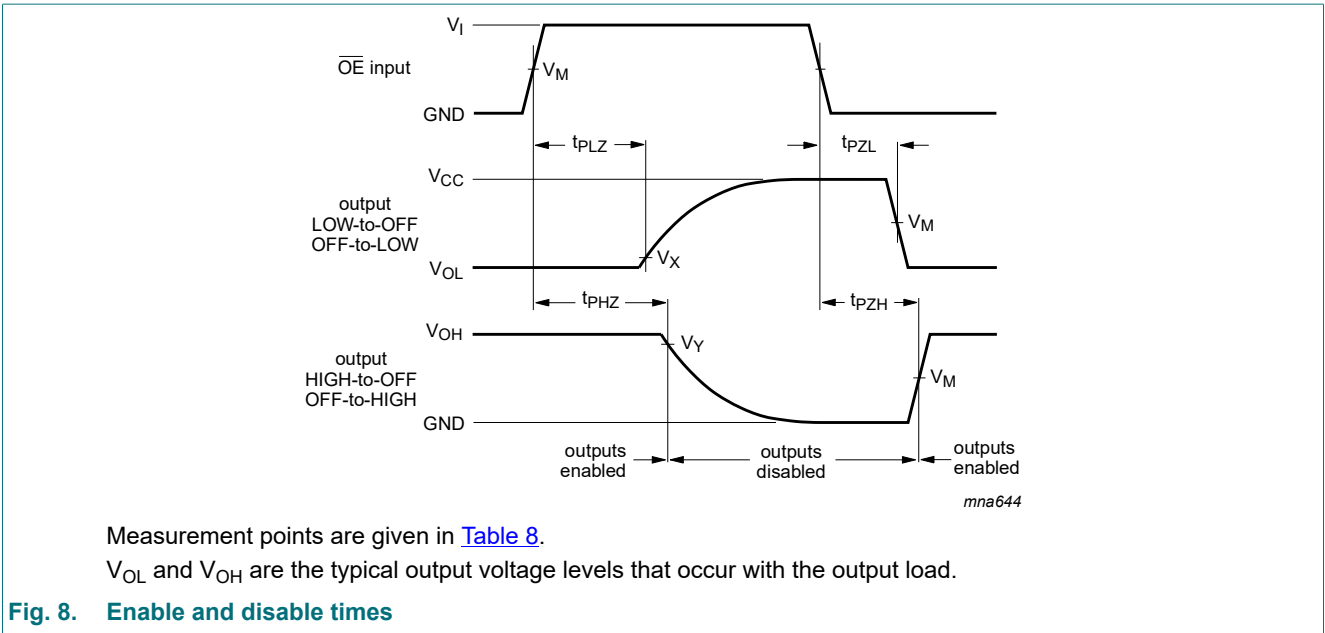
- [1] Typical values are measured at T<sub>amb</sub> = 25 °C
- [2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.  
t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.  
t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

### 10.1. Waveforms and test circuit



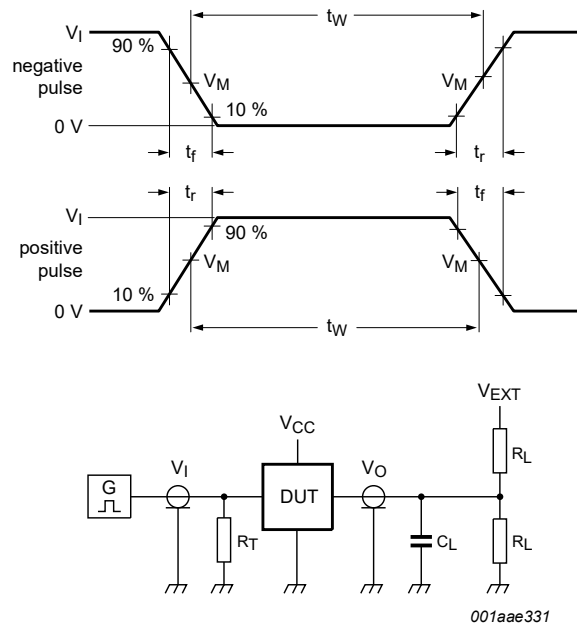
**Table 8. Measurement points**

Supply voltage	Input	Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.65 V to 1.95 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.3 V to 2.7 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V





Octal D-type flip-flop; positive edge-trigger; 3-state



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	$2V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	6 V	GND

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 13. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC574 v.3	20210430	Product data sheet	-	74ALVC574 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 2</a>: Reference to JESD36 removed.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation removed (errata).</li> <li>Package outline drawing of SOT764-1 (<a href="#">Fig. 13</a>) updated.</li> </ul>			
74ALVC574 v.2	20071108	Product data sheet	-	74ALVC574 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN20 package added.</li> <li><a href="#">Section 7</a>: derating values added for DHVQFN20 package.</li> <li><a href="#">Section 11</a>: outline drawing added for DHVQFN20 package.</li> </ul>			
74ALVC574 v.1	20020304	Product specification	-	-

## Octal D-type flip-flop; positive edge-trigger; 3-state

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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