National Semiconductor

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DS25MB200-EVK

Signal Conditioning Mux-Buffer

Demo Board User Guide

Introduction

The DS25MB200 is a signal conditioning 2:1 multiplexer and 1:2 buffer designed to support port redundancy. Advanced signal conditioning features utilizing input equalization and output driver pre-emphasis enable data communication for FR4 backplane over 0.8-2.5Gb/s.

The DS25MB200 demo board is designed to assist customers to evaluate the functionality and performance. All input and output ports of the DS25MB200 are brought out to SMA connectors for accessibility to instrumentation.

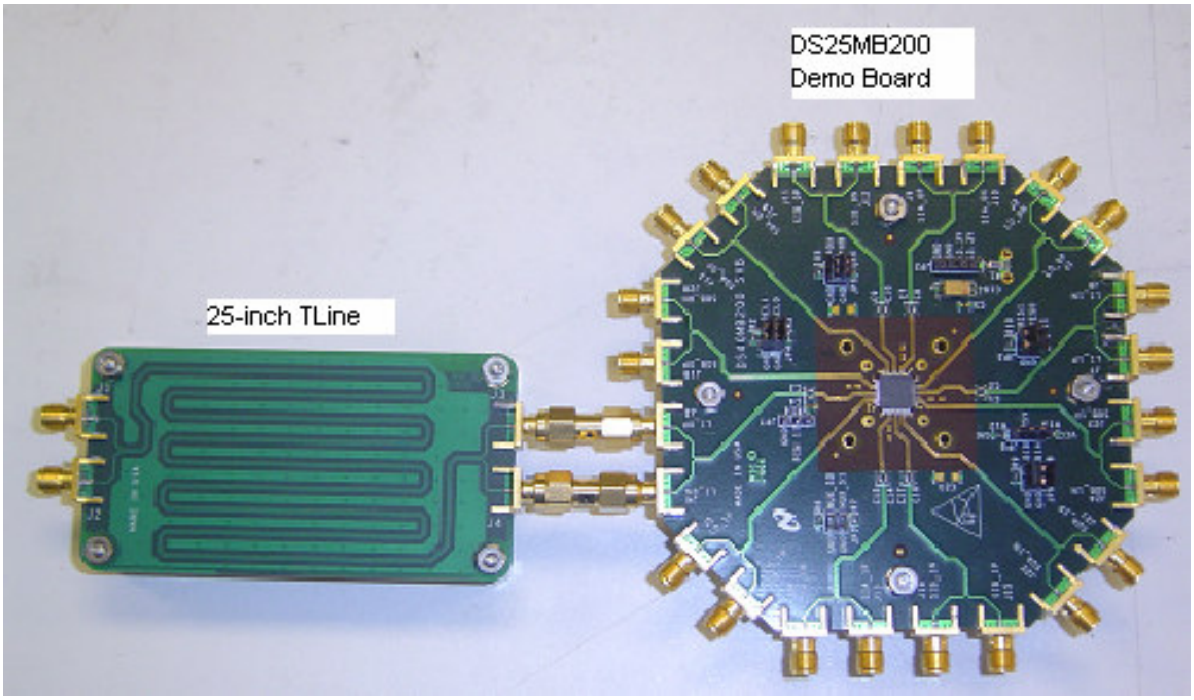
A 25-inch FR4 transmission line is provided along with the demo board to facilitate evaluation of the signal conditioning features. This 25-inch board trace has about 5dB loss from 375MHz to 1.9GHz. It is intended to use as the input transmission line to the DS25MB200, whose on-chip input equalizer is optimized to minimize the deterministic jitter caused by the input board trace. Customers can also connect the DS25MB200 to their backplanes for performance evaluation.

Evaluation Kit Content

This evaluation kit consists of the following components:

(1) DS25MB200 demo board
(2) A 25-inch FR4 differential board trace
(3) Demo Board User Guide (this document)
(4) Demo board schematic

DS25MB200 Demo Board and 25-inch Tline Board



Connection Diagram

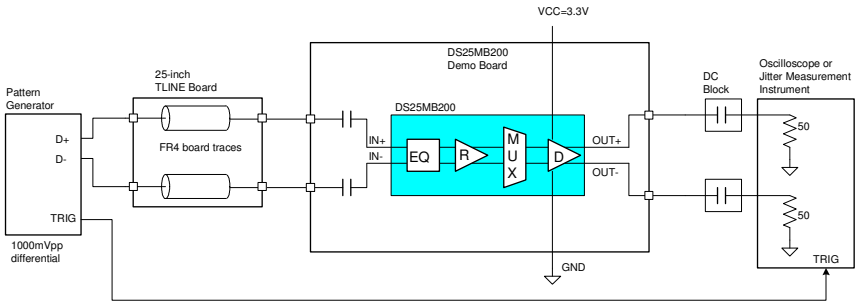


Figure 1. Typical connection for evaluation of the DS25MB200

Power		
VCC GND	JP2.3 JP2.1	3.3V ± 5% 0V

Pre-emphasis controls		
PREL0 PREL1	JP2.4 JP2.2	Set Pre-emphasis level for all outputs at the line side (LO_0± and LO_1±). Open is logic 1. Strap to GND is logic 0.
PRES0 PRES1	JP3.4 JP3.2	Set the pre-emphasis level for all outputs at the switch side (SOA_0±, SOB_0±, SOA_1± and SOB_1±). Open is logic 1. Strap to GND is logic 0.

Mux controls		
MUX_S0 MUX_S1	JP1.3 JP1.1	Set the multiplexer position to switch A or switch B. Open is logic 1. Strap to GND is logic 0.

Loopback controls		
LB0A LB0B LB1A LB1B	JP5.2 JP5.4 JP6.1 JB6.3	Enable or disable loopback. Open is logic 1. Strap to GND is logic 0.

RSV control		
RSV	JP8.2	Reserved for factory testing purposes. JP8.2 is permanently tied to GND.

Logic control for data paths

Following tables list the logic states of the control pins used to configure the data paths of the DS25MB200. More detailed information about pin functions and pin descriptions can be found in the DS25MB200 datasheet.

Logic table for multiplex controls

MUX_S0	*Mux Function*
0	MUX_0 select switch_B input, SIB_0±.
1 (default)	MUX_0 select switch_A input, SIA_0±.

MUX_S1	*Mux Function*
0	MUX_1 select switch_B input, SIB_1±.
1 (default)	MUX_1 select switch_A input, SIA_0±.

Logic table for loopback controls

LB0A	*Loopback Function*
0	Enable loopback from SIA_0± to SOA_0±.
1	Normal mode. Loopback disabled.

LB0B	*Loopback Function*
0	Enable loopback from SIB_0± to SOB_0±.
1	Normal mode. Loopback disabled.

LB1A	*Loopback Function*
0	Enable loopback from SIA_1± to SOA_1±.
1	Normal mode. Loopback disabled.

LB1B	*Loopback Function*
0	Enable loopback from SIB_1± to SOB_1±.
1	Normal mode. Loopback disabled.

Line-side pre-emphasis controls

PreL_[1:0]	***Pre-emphasis level in mVpp***	***De-emphasis level in mVpp***	***Pre-emphasis in dB***
0 0	1200	1200	0
0 1	1200	849.53	-3
1 0	1200	600	-6
1 1	1200	425.78	-9

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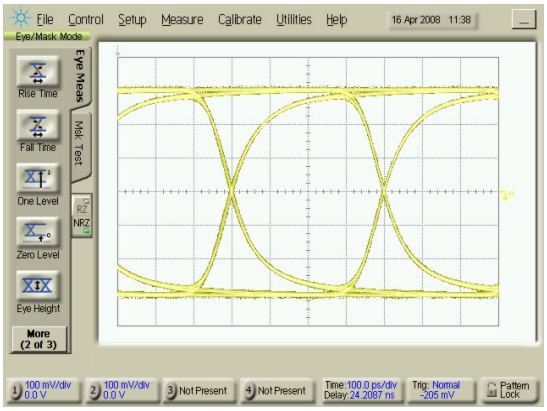
Switch-side pre-emphasis controls

PreS_[1:0]	***Pre-emphasis level in mVpp***	***De-emphasis level in mVpp***	***Pre-emphasis in dB***
0 0	1200	1200	0
0 1	1200	849.53	-3
1 0	1200	600	-6
1 1	1200	425.78	-9

Typical output waveforms

The followings are typical eye diagrams of the DS25MB200 using the demo board connected as shown in Figure 1.



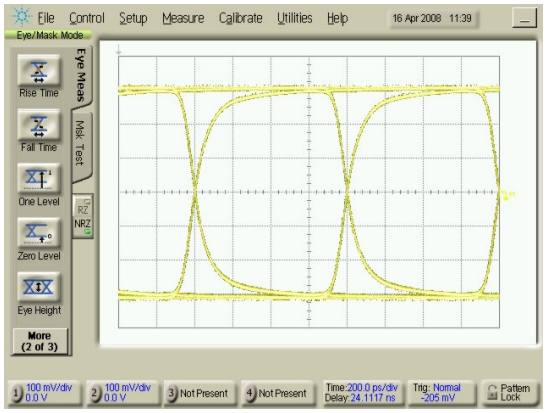
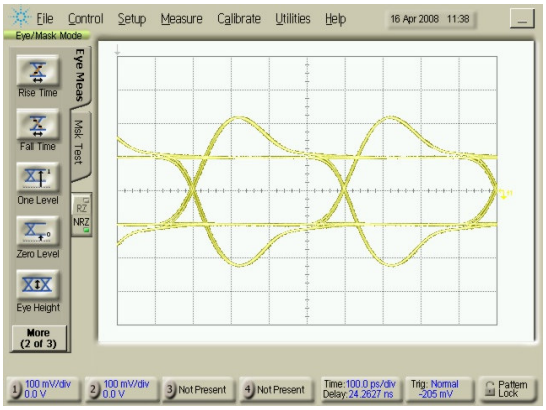


Figure 2a-b. Eye diagrams at 2.5 and 1.25 Gb/s, PRBS7 pattern, Pre-emphasis=0dB



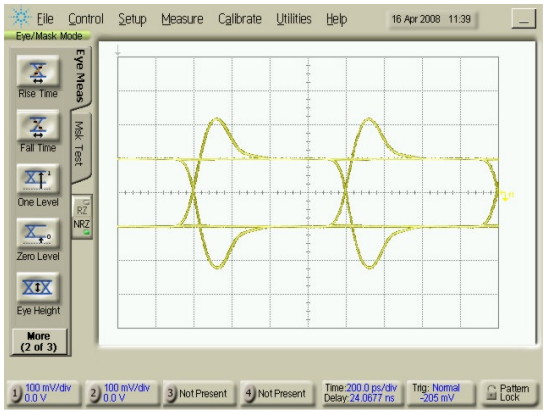
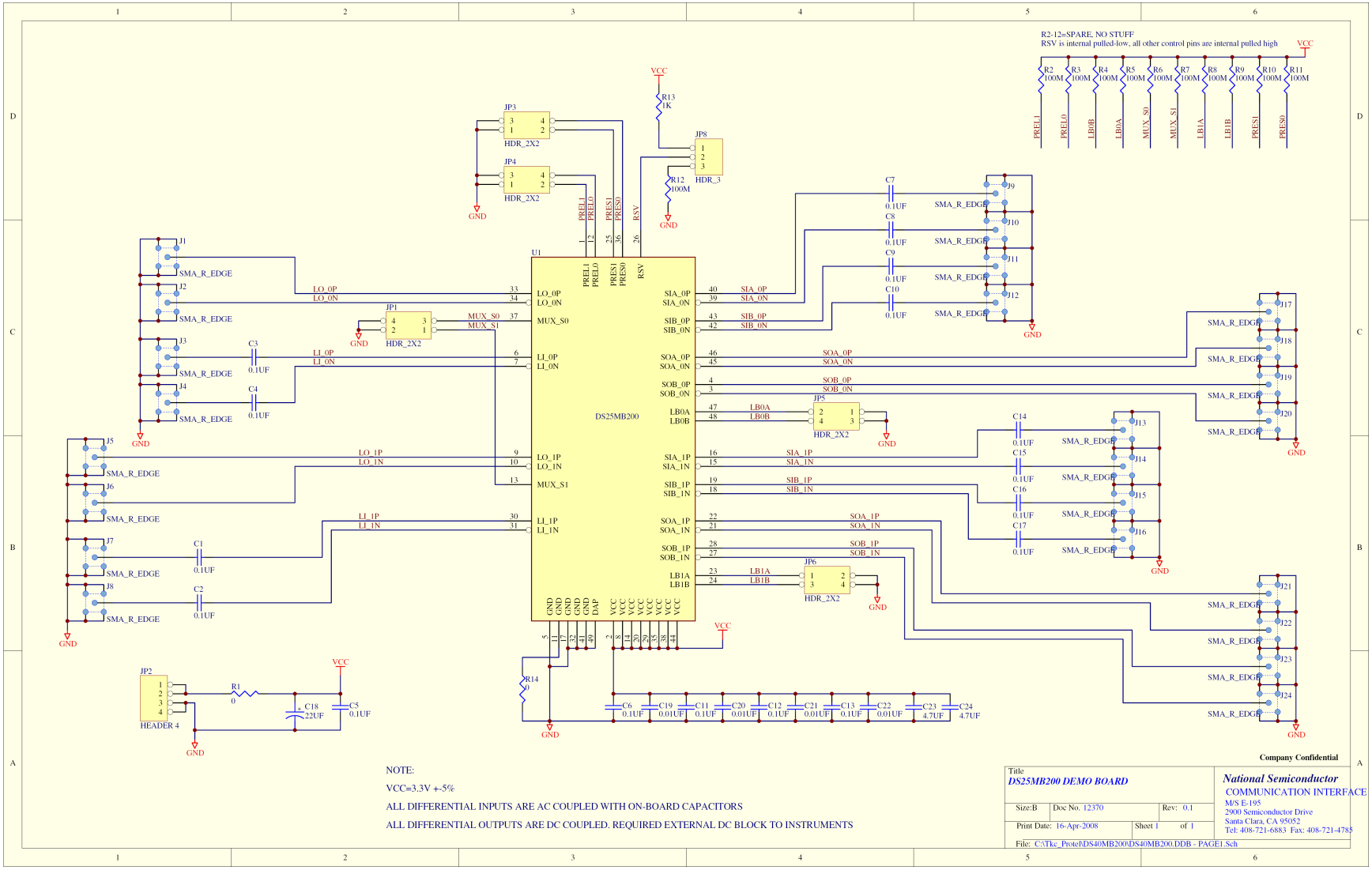


Figure 3a-b. Eye diagrams at 2.5 and 1.25 Gb/s, PRBS7 pattern, Pre-emphasis=9dB

Reference Material

DS25MB200 datasheet
National web site http://www.national.com/appinfo/lvds/

DS25MB200 demo board schematic



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