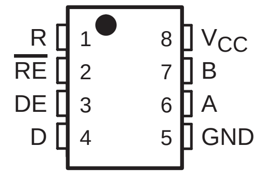
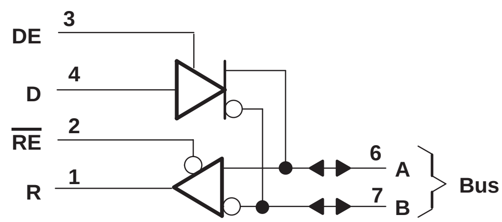
- **Designed for Signaling Rates† Up to 30 Mbps**
- **Bus-Pin ESD Protection Exceeds 12 kV HBM**
- **Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)**
- **Low Skew**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Very Low Disabled Supply-Current Requirements . . . 700 μA Maximum**
- **Common Mode Voltage Range of −7 V to 12 V**
- **Thermal-Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Open-Circuit Failsafe Receiver Design**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Available in Q-Temp Automotive**
  - **High Reliability Automotive Applications**
  - **Configuration Control / Print Support**
  - **Qualification to Automotive Standards**

SN65LBC176AQD (Marked as B176AQ)
SN65LBC176AD (Marked as BL176A)
SN65LBC176AP (Marked as 65LBC176A)
SN75LBC176AD (Marked as LB176A)
SN75LBC176AP (Marked as 75LBC176A)
(TOP VIEW)



logic diagram (positive logic)



description

The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and are compatible with ANSI standard TIA/EIA-485-A and ISO 8482. The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS $V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
$-0.2 \text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

† Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved using a different criteria (see *TYPICAL CHARACTERISTICS* section).

TEXAS INSTRUMENTS
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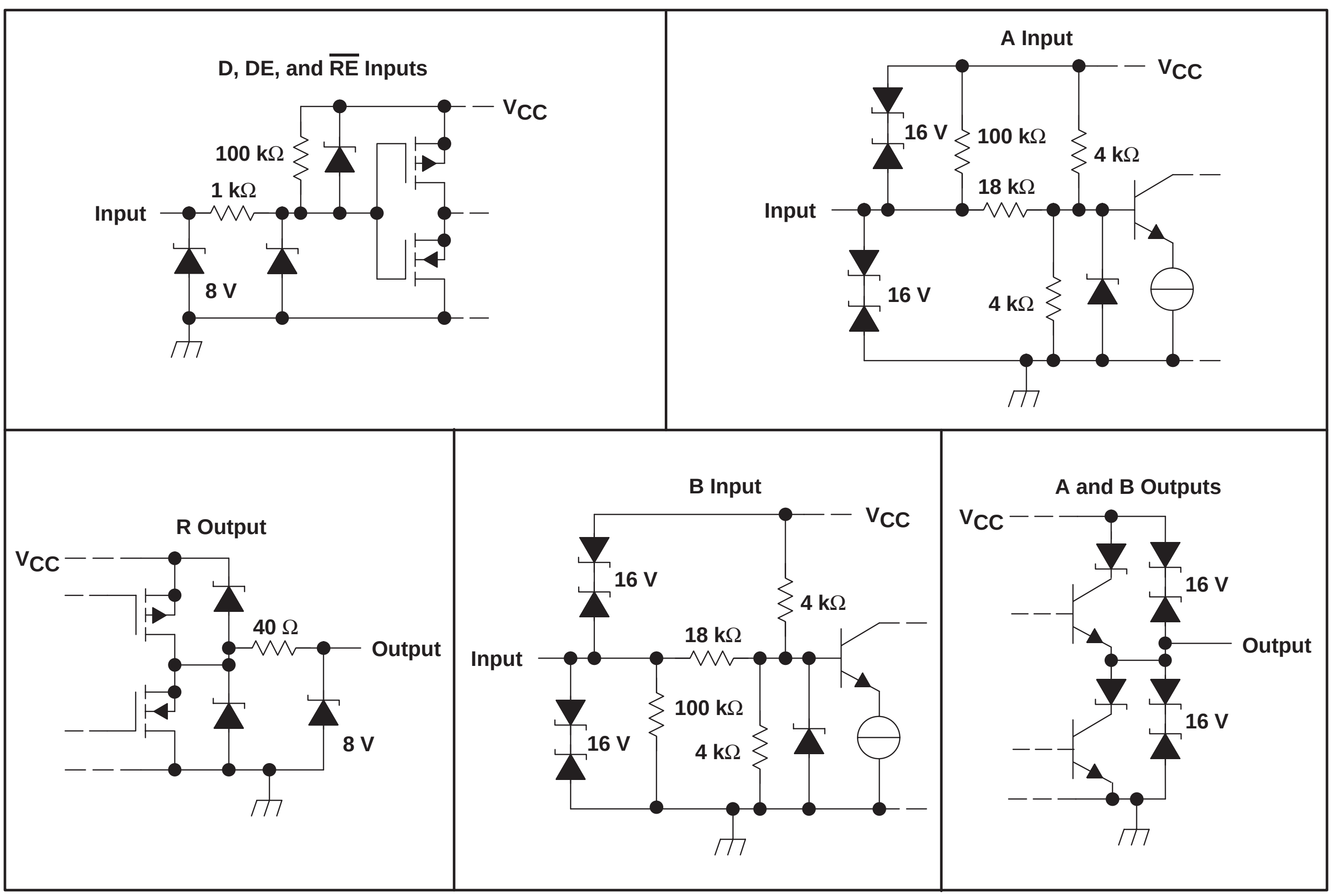
description (continued)

The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DUAL-IN-LINE
0°C to 70°C	SN75LBC176AD	SN75LBC176AP
−40°C to 85°C	SN65LBC176AD	SN65LBC176AP
−40°C to 125°C	SN65LBC176AQD	—

schematics of inputs and outputs



absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1) . . . . −0.3 V to 6 V
Voltage range at any bus terminal (A or B) . . . . −10 V to 15 V
Input voltage, V_I (D, DE, R, or $\overline{RE}$) . . . . −0.3 V to V_{CC} + 0.5 V
Electrostatic discharge: Bus terminals and GND, Class 3, A: (see Note 2) . . . . 12 kV
Bus terminals and GND, Class 3, B: (see Note 2) . . . . 400 V
All terminals, Class 3, A: . . . . 3 kV
All terminals, Class 3, B: . . . . 400 V
Continuous total power dissipation (see Note 3) . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
2. Tested in accordance with MIL−STD−883C, Method 3015.7
3. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$	0		0.8	V
Differential input voltage, V_{ID} (see Note 4)		−12§		12	V
High-level output current, I_{OH}	Driver	−60			mA
	Receiver	−8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65LBC176AQ	−40		125	°C
	SN65LBC176A	−40		85	
	SN75LBC176A	0		70	

§ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA		−1.5	−0.8		V
$\lvert V_{OD} \rvert$	Differential output voltage	I_O = 0	SN65LBC176AQ	1.5	4	6	V
			SN65LBC176A, SN75LBC176A		4		
		R_L = 54 Ω, See Figure 1	SN65LBC176AQ	0.9	1.5	6	
			SN65LBC176A	1	1.5	3	V
			SN75LBC176A	1.1	1.5	3	V
		V_{test} = −7 V to 12 V, See Figure 2	SN65LBC176AQ	0.9	1.5	6	
			SN65LBC176A	1	1.5	3	V
			SN75LBC176A	1.1	1.5	3	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage	See Figures 1 and 2		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 1	SN65LBC176AQ	1.8	2.4	3	V
			SN65LBC176A, SN75LBC176A	1.8	2.4	2.8	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		SN65LBC176AQ	−0.2		0.2	
			SN65LBC176A, SN75LBC176A	−0.1		0.1	
I_{OZ}	High-impedance output current	See receiver input currents					
I_{IH}	High-level enable input current	V_I = 2 V		−100			µA
I_{IL}	Low-level enable input current	V_I = 0.8 V		−100			µA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V		−250		250	mA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled		5	9	mA
			Receiver disabled and driver disabled		0.4	0.7	
			Receiver enabled and driver enabled		8.5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 3	2		12	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2		12	2	6	12	ns
$t_{sk(p)}$	Pulse skew (| t_{PLH} − t_{PHL} |)				2		0.3	1	ns
t_r	Differential output signal rise time		1.2		11	4	7.5	11	ns
t_f	Differential output signal fall time		1.2		11	4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, See Figure 4			22		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, See Figure 5			25		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	R_L = 110 Ω, See Figure 4			22		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, See Figure 5			22		12	22	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	I_O = 8 mA				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA			−1.5	−0.8		V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −8 mA,	See Figure 6	4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 6		0.1	0.8	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}		SN65LBC176AQ	−10		10	μA
				SN65LBC176A, SN75LBC176A	−1		1	
I_I	Bus input current	V_{IH} = 12 V,	V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_{IH} = 12 V,	V_{CC} = 0			0.5	1	
		V_{IH} = −7 V,	V_{CC} = 5 V		−0.8	−0.4		
		V_{IH} = −7 V,	V_{CC} = 0		−0.8	−0.3		
I_{IH}	High-level enable-input current	V_{IH} = 2 V			−100			μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.8 V			−100			μA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled			4	7	mA
			Receiver disabled and driver disabled			0.4	0.7	
			Receiver enabled and driver enabled			8.5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LBC176AQ			SN65LBC176A SN75LBC176A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, output↑	V_{ID} = −1.5 V to 1.5 V, See Figure 7	7		30	7	13	20	ns
t_{PHL}	Propagation delay time, output↓		7		30	7	13	20	ns
$t_{sk(p)}$	Pulse skew (| $t_{PHL} - t_{PLH}$ |)				6		0.5	1.5	ns
t_r	Rise time, output	See Figure 7			5		2.1	3.3	ns
t_f	Fall time, output				5		2.1	3.3	ns
t_{PZH}	Output enable time to high level	C_L = 10 pF, See Figure 8			50		30	45	ns
t_{PZL}	Output enable time to low level				50		30	45	ns
t_{PHZ}	Output disable time from high level				60		20	40	ns
t_{PLZ}	Output disable time from low level				40		20	40	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

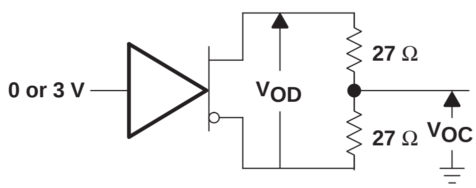


Figure 1. Driver V_{OD} and V_{OC}

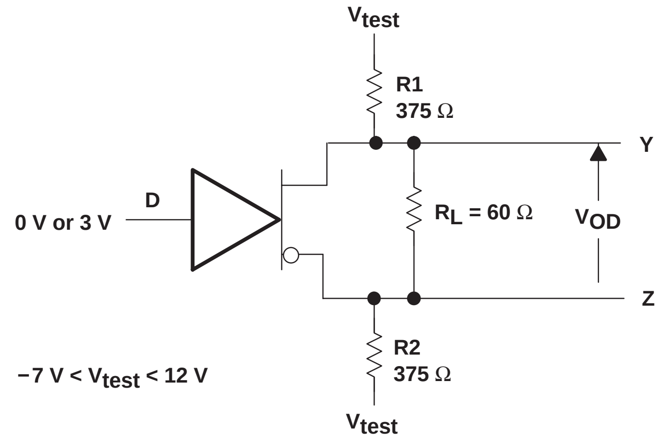
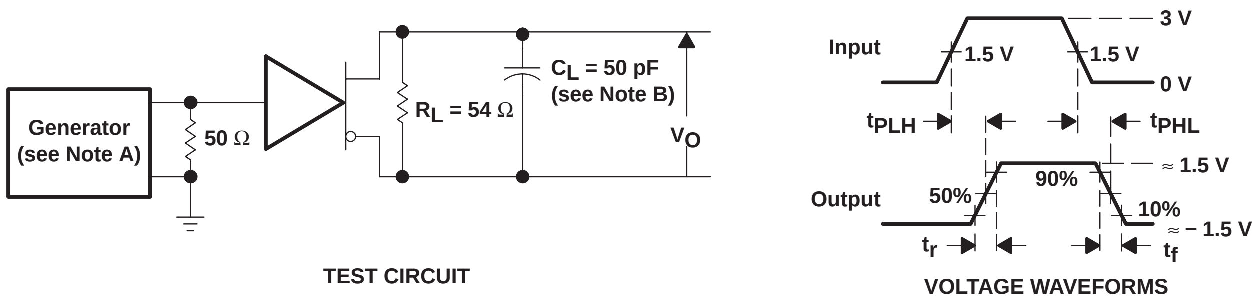
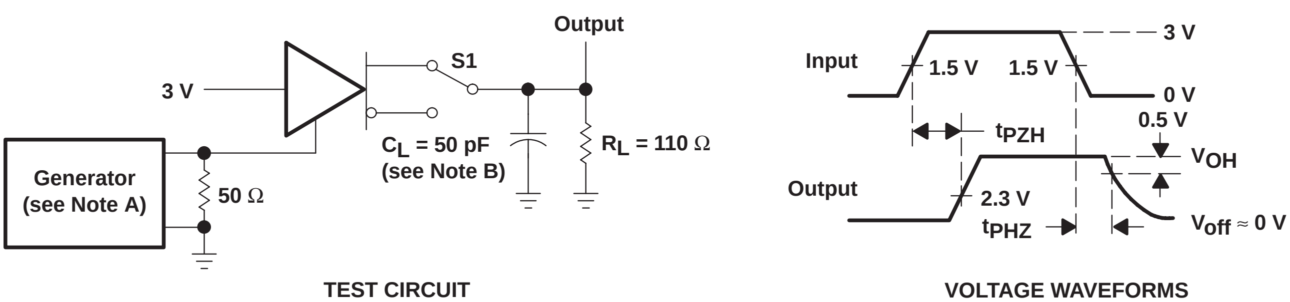


Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

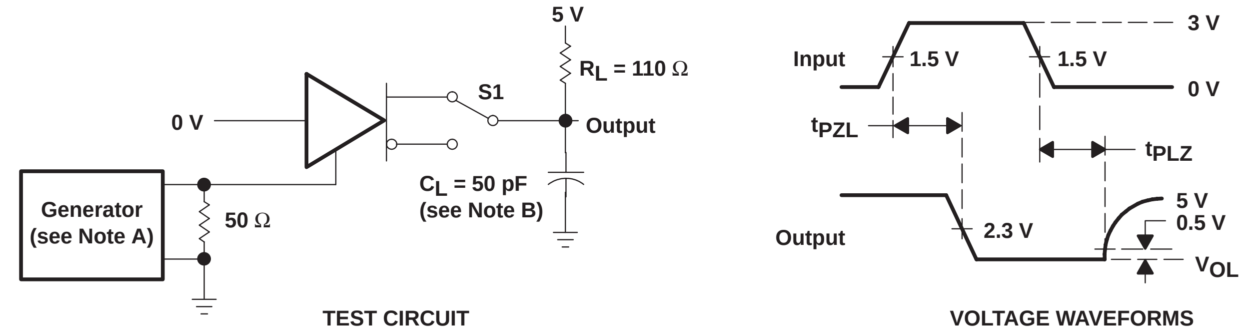
Figure 3. Driver Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

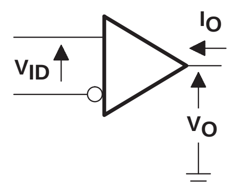
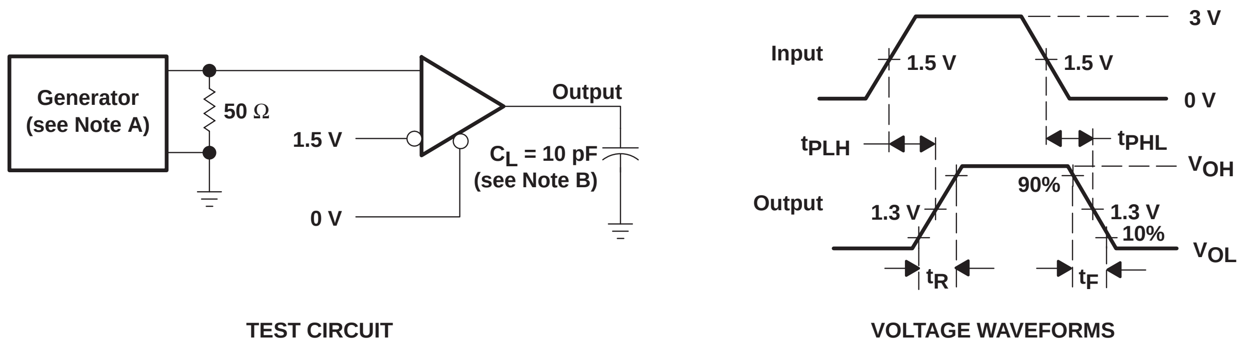


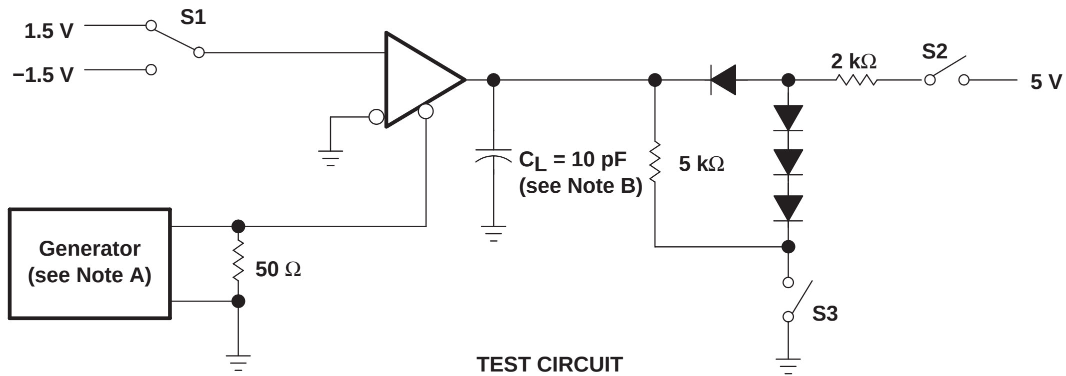
Figure 6. Receiver V_{OH} and V_{OL}



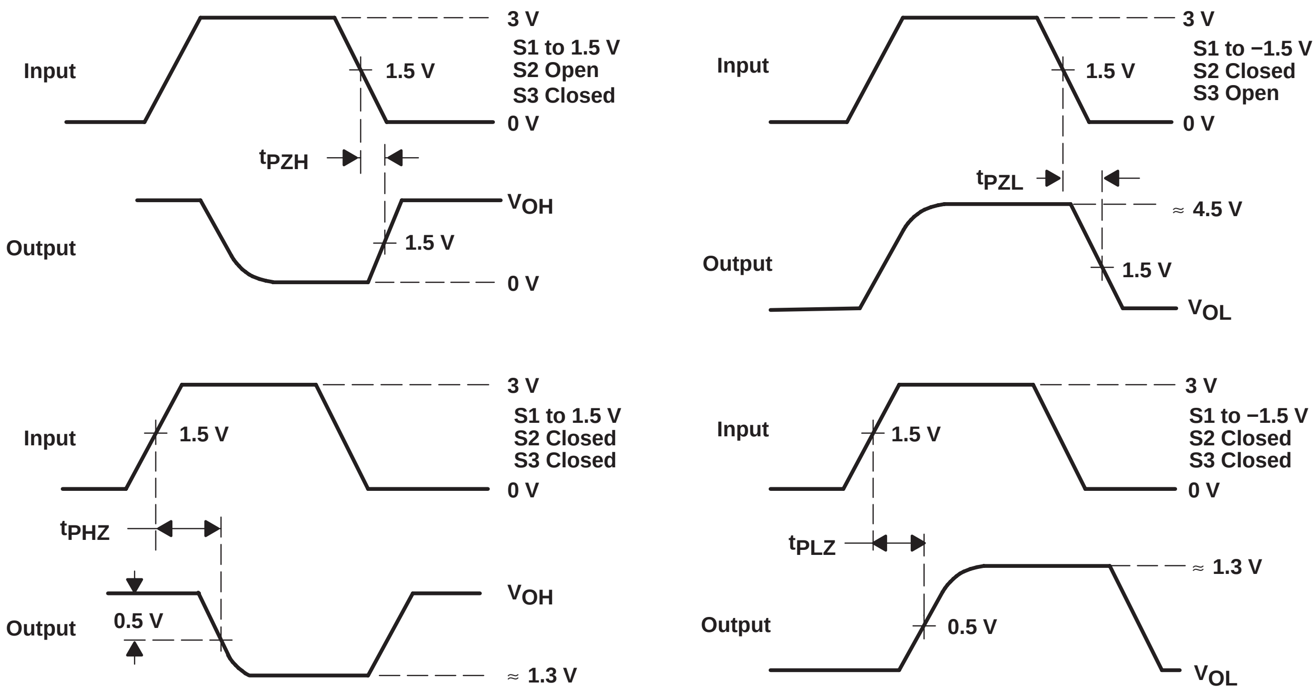
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

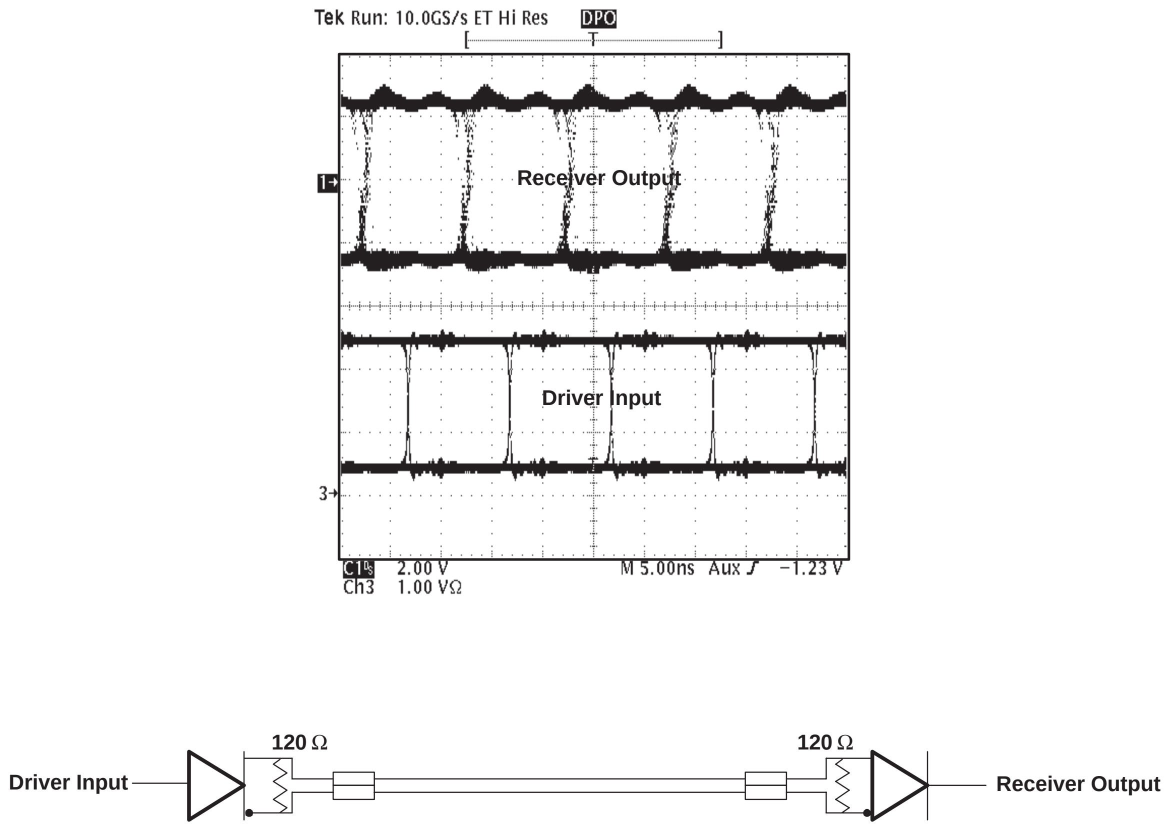


Figure 9. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard definition.

TYPICAL CHARACTERISTICS

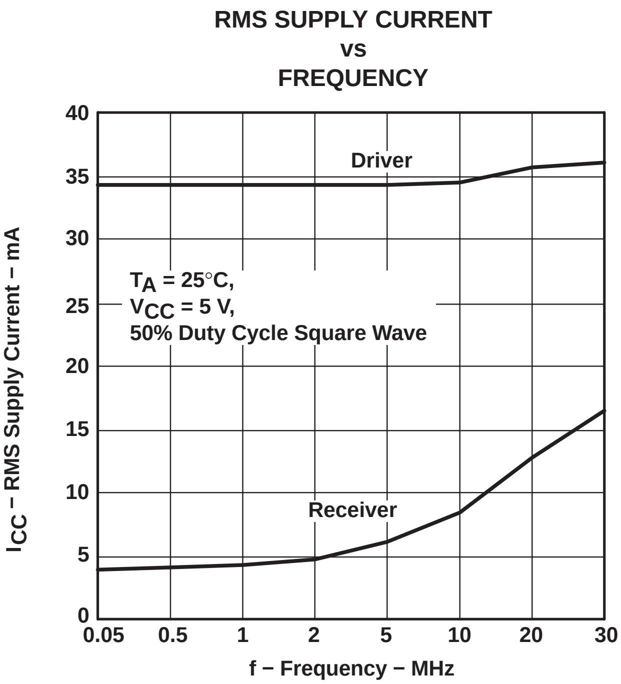


Figure 10

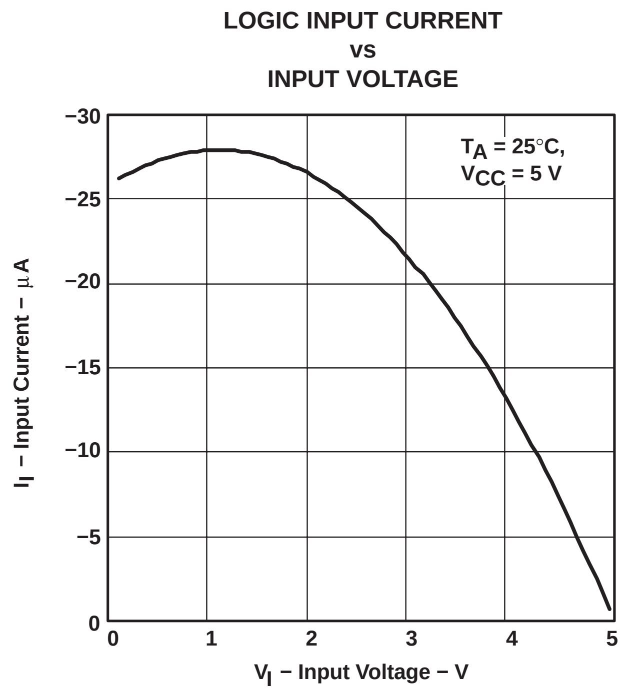


Figure 11

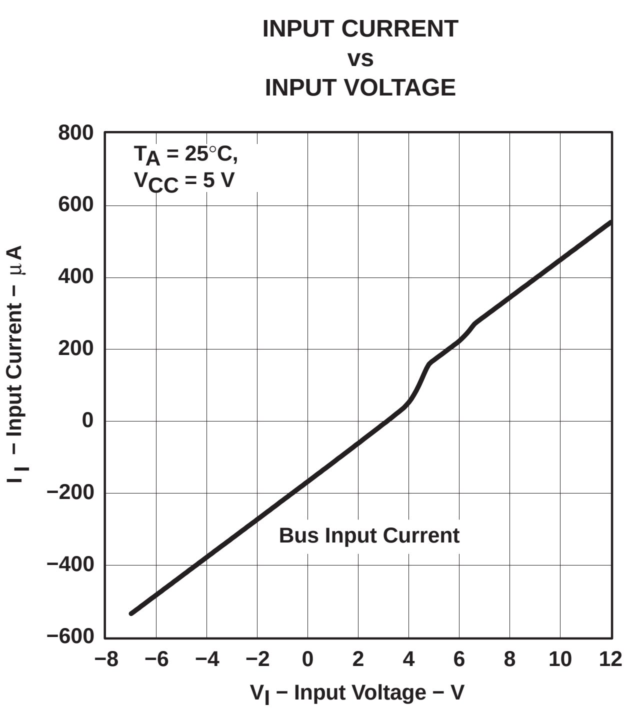


Figure 12

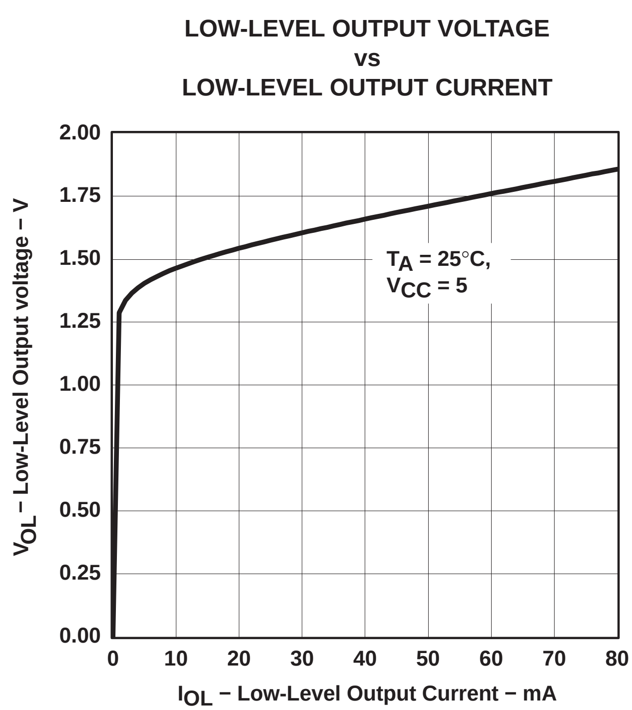


Figure 13

TYPICAL CHARACTERISTICS

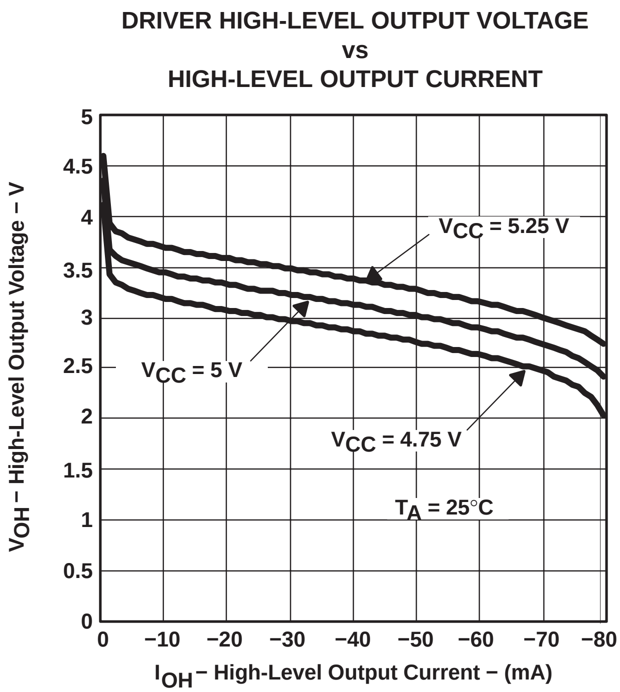


Figure 14

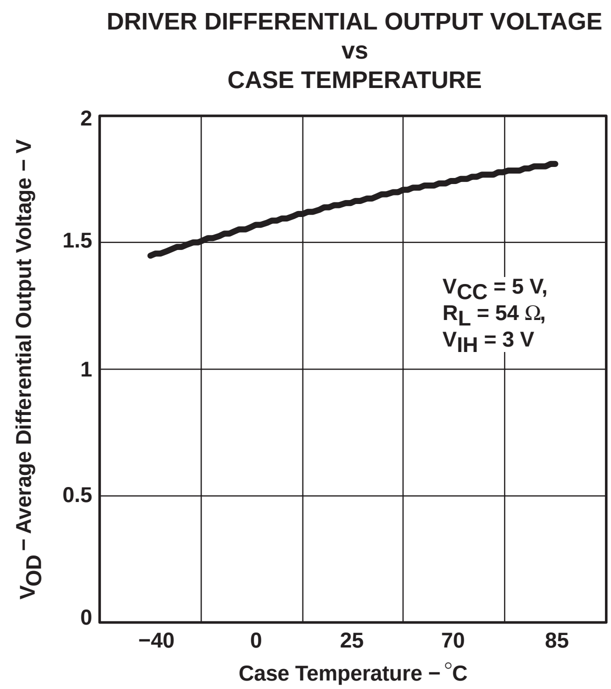


Figure 15

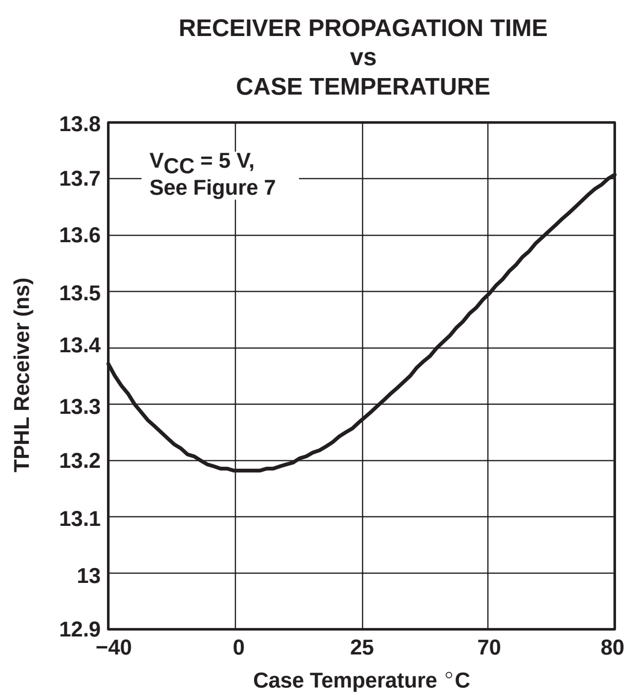


Figure 16

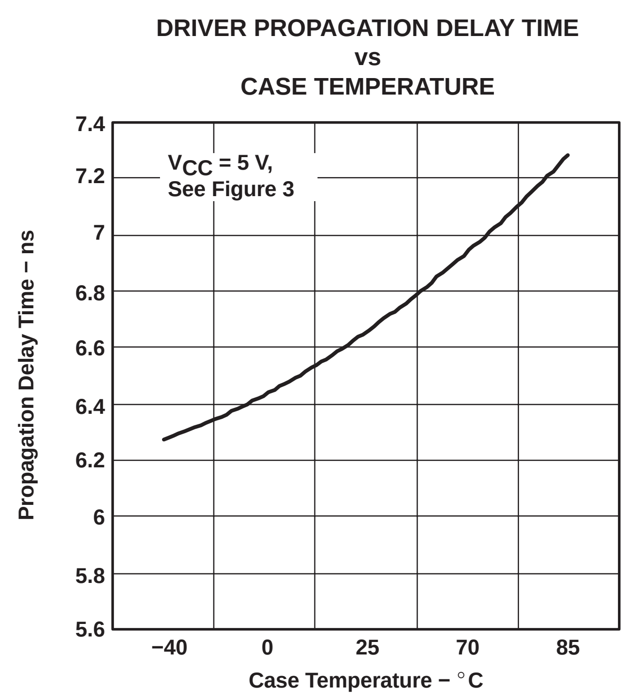


Figure 17

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

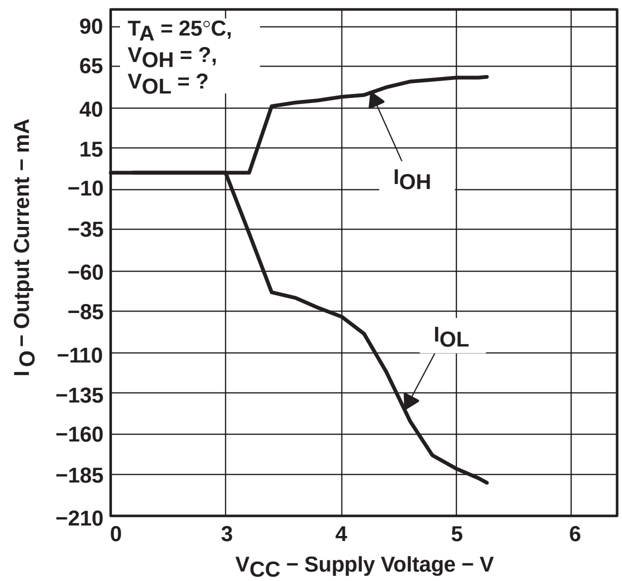


Figure 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC176AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	Samples
SN65LBC176ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	Samples
SN65LBC176ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL176A	Samples
SN65LBC176AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176A	Samples
SN65LBC176AQD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	Samples
SN65LBC176AQDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		B176AQ	Samples
SN65LBC176AQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B176AQ	Samples
SN65LBC176AQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		B176AQ	Samples
SN75LBC176AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	Samples
SN75LBC176ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	Samples
SN75LBC176ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	Samples
SN75LBC176ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB176A	Samples
SN75LBC176AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC176A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LBC176A :

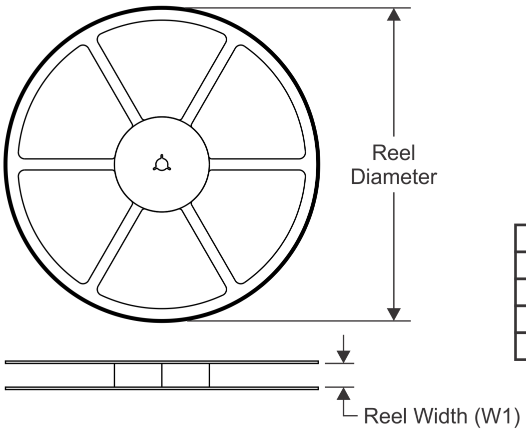
- Enhanced Product : SN65LBC176A-EP

NOTE: Qualified Version Definitions:

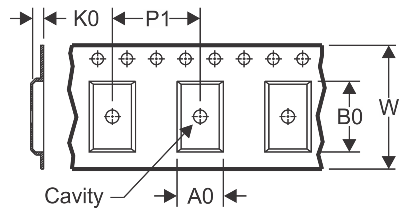
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

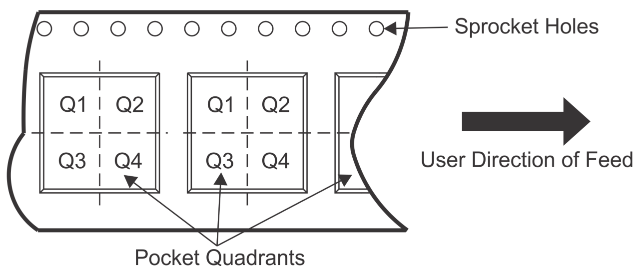


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

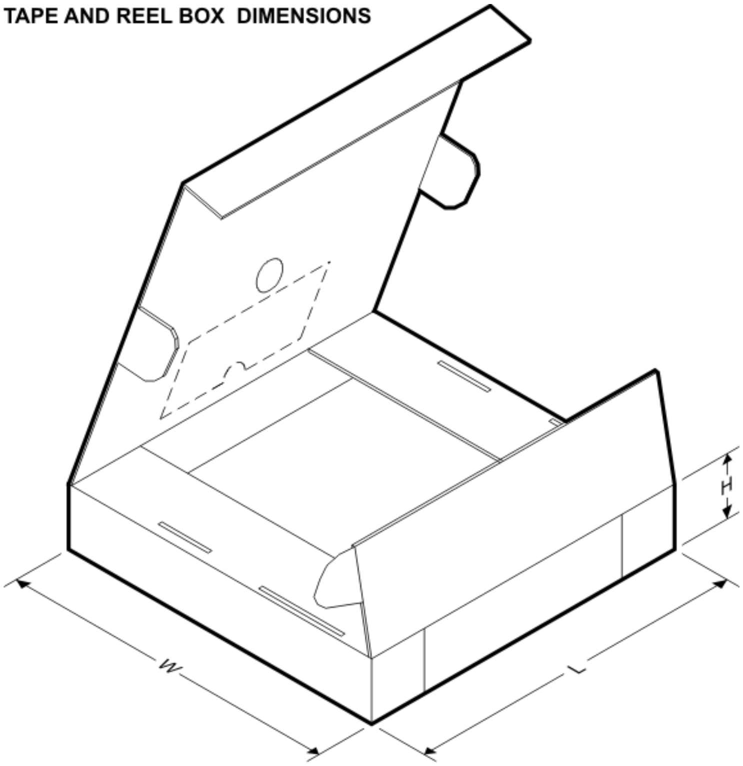
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

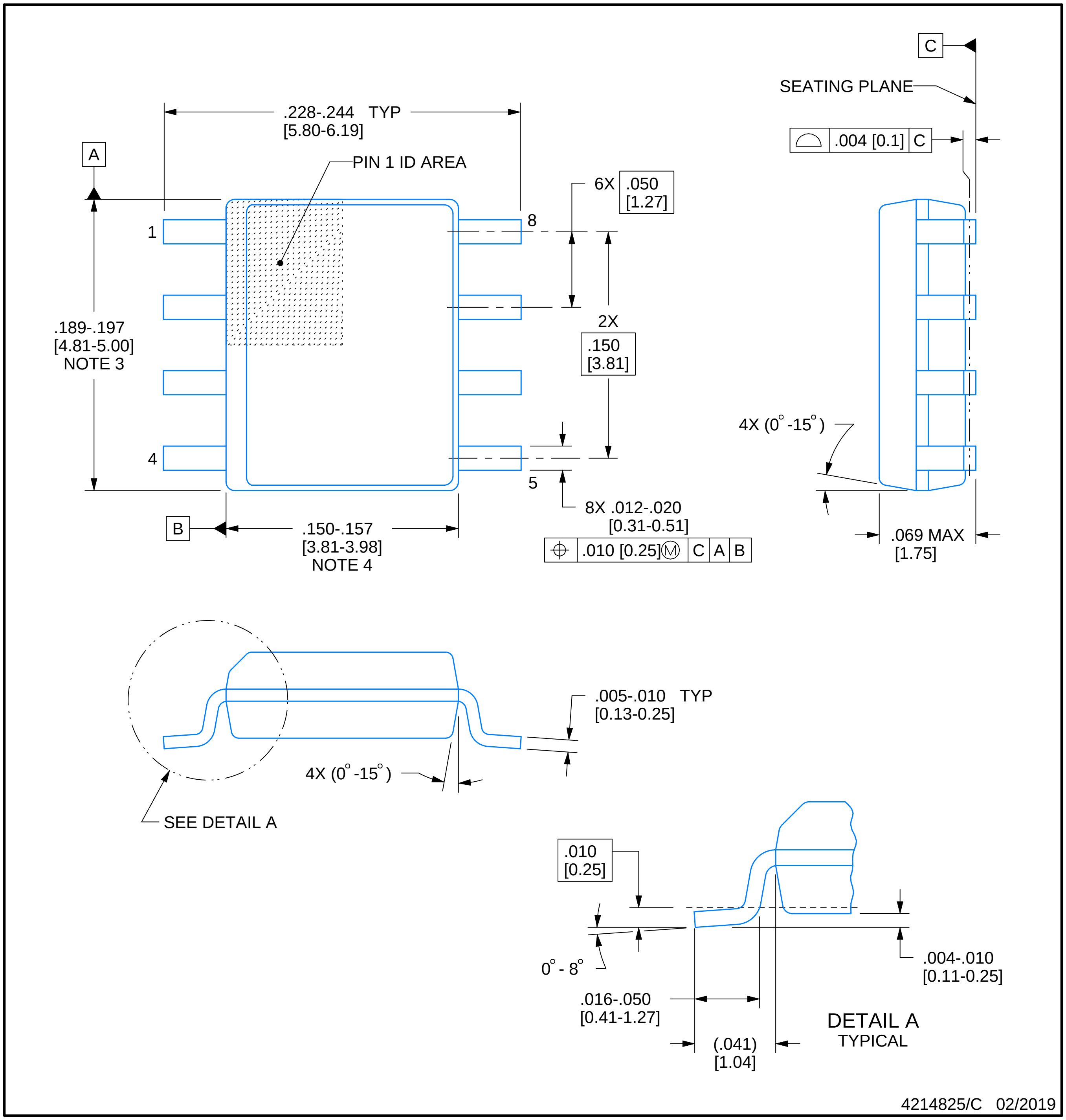
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC176ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



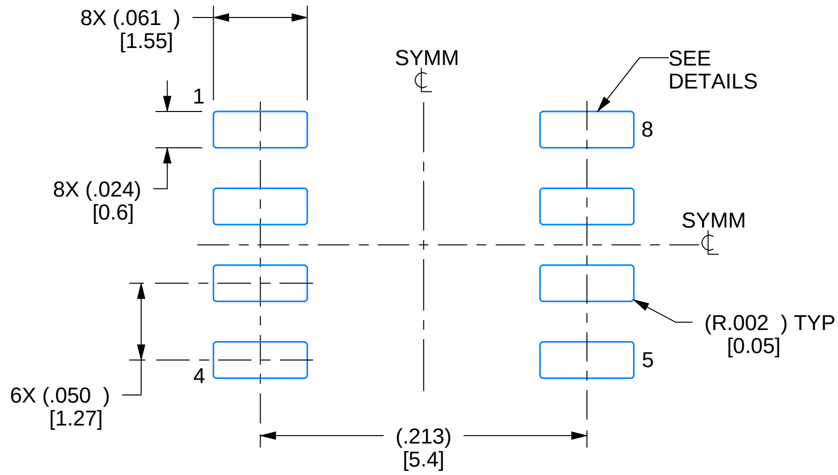
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176ADR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LBC176AQDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC176ADR	SOIC	D	8	2500	340.5	336.1	25.0

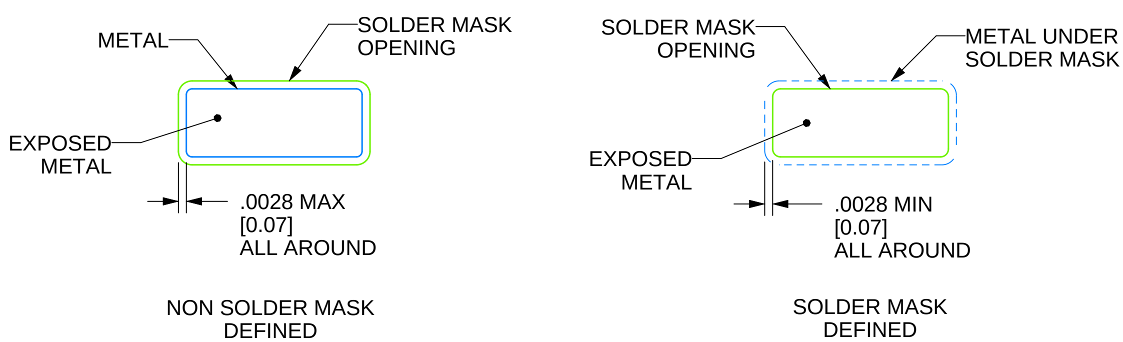


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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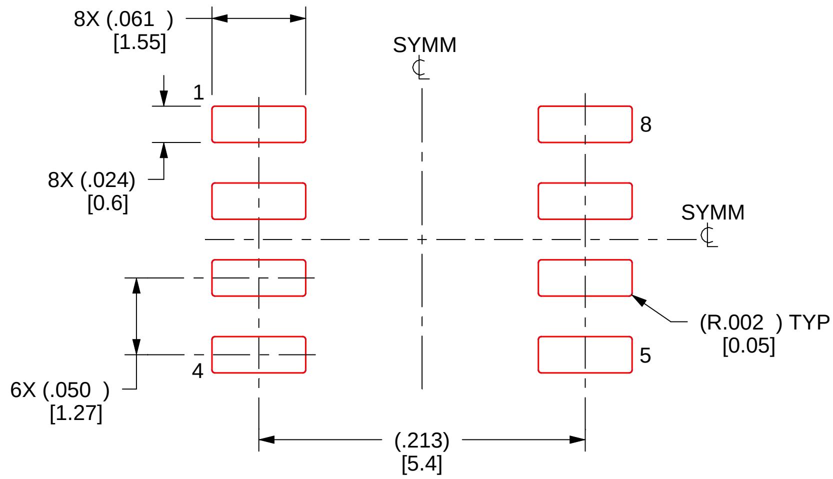
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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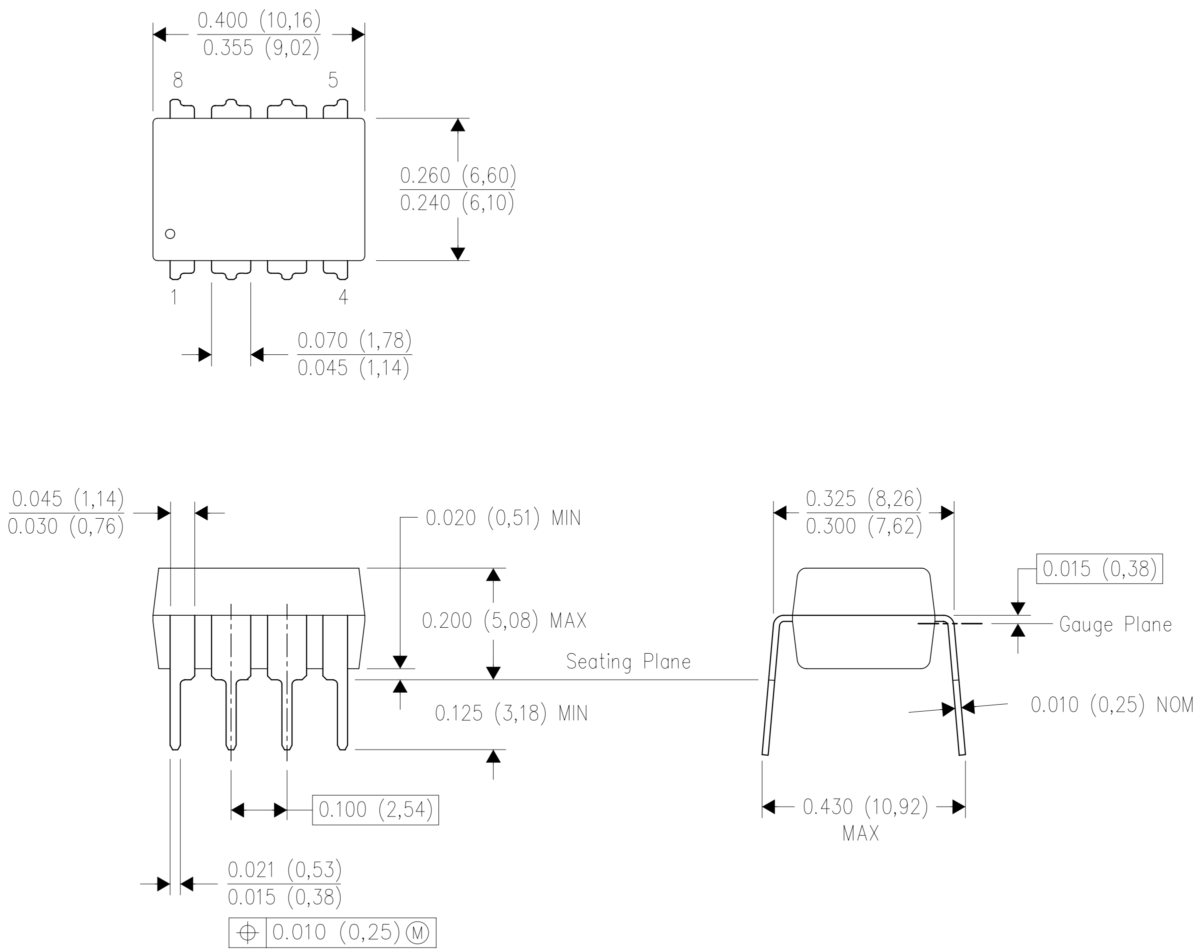
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.