

# NXS0104

Dual supply translating transceiver; open drain;  
auto direction sensing

Rev. 4 — 30 June 2021

Product data sheet

## 1. General description

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The NXS0104 is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 1.65 V and 3.6 V and  $V_{CC(B)}$  can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to  $V_{CC(A)}$  and pins Bn are referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Wide supply voltage range:
  - $V_{CC(A)}$ : 1.65 V to 3.6 V and  $V_{CC(B)}$ : 2.3 V to 5.5 V
- Maximum data rates:
  - Push-pull: 24 Mbps
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM: ANSI/ESDA/Jedec JS-001 Class 2 exceeds 2.5 kV for A port
  - HBM: ANSI/ESDA/Jedec JS-001 Class 3B exceeds 15 kV for B port
  - CDM: ANSI/ESDA/Jedec JS-002 Class C3 exceeds 1.5 kV
  - IEC61000-4-2 contact discharge exceeds 8000 V for B port
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Applications

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- Desktop PC
- Handset
- Smartphone
- Tablet

## 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXS0104PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
NXS0104BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
NXS0104GU12	-40 °C to +125 °C	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.0 × 0.50 mm	SOT1174-1
NXS0104UM	-40 °C to +125 °C	WLCSP12	wafer level chip-scale package; 12 bumps; 1.36 × 1.86 × 0.60 mm	SOT8019-1

## 5. Marking

Table 2. Marking

Type number	Marking code
NXS0104PW	NXS0104
NXS0104BQ	S0104
NXS0104GU12	m4
NXS0104UM	m4

6. Functional diagram

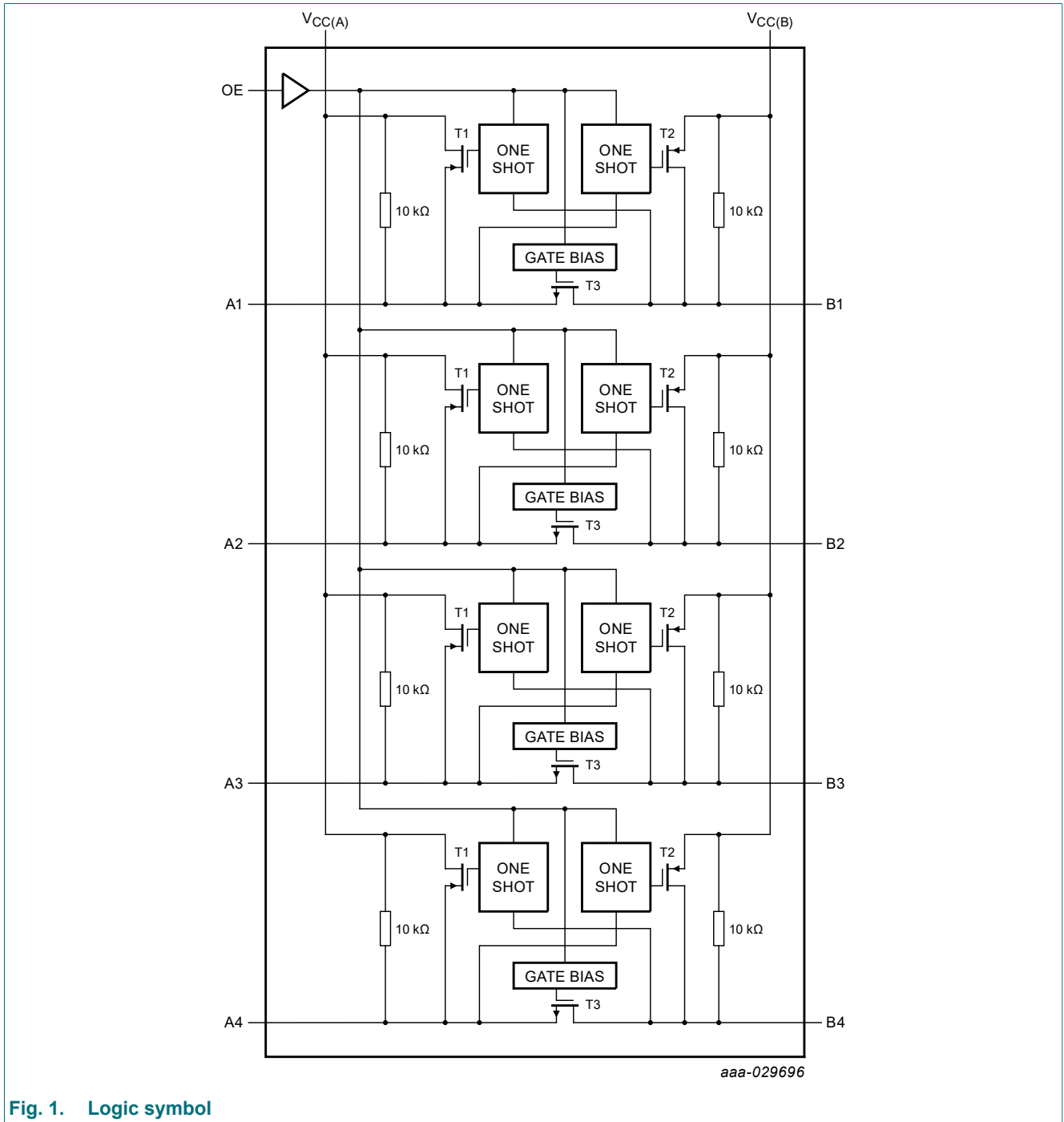
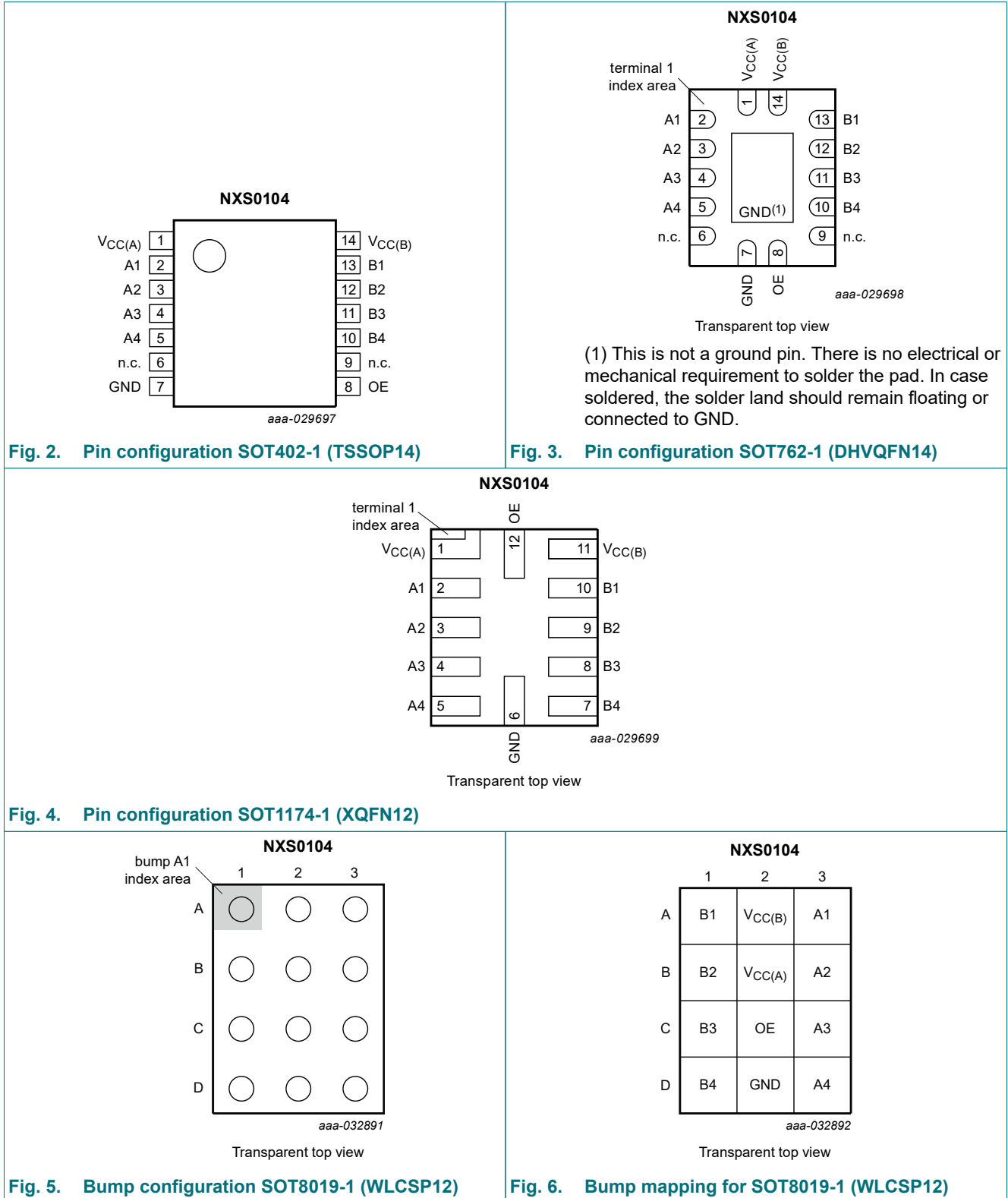


Fig. 1. Logic symbol

## 7. Pinning information

### 7.1. Pinning



## 7.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT402-1, SOT762-1	SOT1174-1	
$V_{CC(A)}$	1	1	supply voltage A
A1, A2, A3, A4	2, 3, 4, 5	2, 3, 4, 5	data input or output (referenced to $V_{CC(A)}$ )
n.c.	6, 9	-	not connected
GND	7	6	ground (0 V)
OE	8	12	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
B4, B3, B2, B1	10, 11, 12, 13	7, 8, 9, 10	data input or output (referenced to $V_{CC(B)}$ )
$V_{CC(B)}$	14	11	supply voltage B

Table 4. Bump description for SOT8019-1 (WLCSP12)

Symbol	Bump	Description
$V_{CC(A)}$	B2	supply voltage A
A1, A2, A3, A4	A3, B3, C3, D3	data input or output (referenced to $V_{CC(A)}$ )
GND	D2	ground (0 V)
OE	C2	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
B1, B2, B3, B4	A1, B1, C1, D1	data input or output (referenced to $V_{CC(B)}$ )
$V_{CC(B)}$	A2	supply voltage B

## 8. Functional description

Table 5. Function table

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Supply voltage		Input	Input/output	
$V_{CC(A)}$ [1]	$V_{CC(B)}$	OE	An	Bn
1.65 V to 3.6 V	2.3 V to 5.5 V	L	Z	Z
1.65 V to 3.6 V	2.3 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$  and  $V_{CC(A)}$  must not exceed 3.6 V.

[2] When either  $V_{CC(A)}$  or  $V_{CC(B)}$  is at GND level, the device goes into power-down mode.

## 9. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
$V_I$	input voltage	A port and OE input [1]	-0.5	+6.5	V
		B port [1]	-0.5	+6.5	V
$V_O$	output voltage	Active mode [1] [2]			
		A or B port	-0.5	$V_{CCO} + 0.5$	V
		Power-down or 3-state mode [1]			
		A port	-0.5	+4.6	V
		B port	-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$ [2]	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C			
		SOT402-1 (TSSOP14) SOT762-1 (DHSVFN14) [3]	-	500	mW
		SOT1174-1 (XQFN12) SOT8019-1 (WLCSP12) [4]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output.

[3] For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHSVFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

[4] For SOT8019-1 (WLCSP12) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 116 °C.

## 10. Recommended operating conditions

**Table 7. Recommended operating conditions [1] [2]**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V
		OE input			
		$V_{CC(A)} = 1.65$ V to 3.6 V; $V_{CC(B)} = 2.3$ V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CC1}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$  and  $V_{CC(A)}$  must not exceed 3.6 V.

## 11. Static characteristics

**Table 8. Typical static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ . [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	OE input; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; OE = 0 V; $V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
		B port; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$	-	2	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$				
		enabled	-	10	-	pF
		disabled	-	4	-	pF
		B port; $V_{CC(A)} = 3.3\text{ V}$ ; $V_{CC(B)} = 3.3\text{ V}$				
		enabled	-	10	-	pF
	disabled	-	7	-	pF	

[1]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$  and  $V_{CC(A)}$  must not exceed 3.6 V.

**Table 9. Typical supply current**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	$\mu\text{A}$
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	$\mu\text{A}$
3.3 V	-	-	0.1	0.1	0.1	2.8	$\mu\text{A}$

**Table 10. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	A port					
		$V_{CC(A)} = 1.65\text{ V to }1.95\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	$V_{CC(A)} - 0.2$	$V_{CC(A)}$	$V_{CC(A)} - 0.2$	$V_{CC(A)}$	V
		$V_{CC(A)} = 2.3\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	$V_{CC(A)} - 0.4$	$V_{CC(A)}$	$V_{CC(A)} - 0.4$	$V_{CC(A)}$	V
		B port					
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	$V_{CC(B)} - 0.4$	$V_{CC(B)}$	$V_{CC(B)} - 0.4$	$V_{CC(B)}$	V
		OE input					
	$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V}$ ; $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	$0.65V_{CC(A)}$	$V_{CC(A)}$	V	

## Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IL</sub>	LOW-level input voltage	A or B port					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0	0.15	0	0.15	V
		OE input					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0	0.35V <sub>CC(A)</sub>	0	0.35V <sub>CC(A)</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	A port; I <sub>O</sub> = -20 μA; V <sub>I</sub> ≥ V <sub>CC(B)</sub> - 0.4 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0.67V <sub>CC(A)</sub>	-	0.67V <sub>CC(A)</sub>	-	V
		B port; I <sub>O</sub> = -20 μA; V <sub>I</sub> ≥ V <sub>CC(A)</sub> - 0.2 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	0.67V <sub>CC(B)</sub>	-	0.67V <sub>CC(B)</sub>	-	V
V <sub>OL</sub>	LOW-level output voltage	A or B port; I <sub>O</sub> = 1 mA; V <sub>I</sub> ≤ 0.15 V					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	0.4	-	0.4	V
I <sub>I</sub>	input leakage current	OE input; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	±2	-	±12	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0 V to 5.5 V	-	±2	-	±12	μA
		B port; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0 V to 3.6 V	-	±2	-	±12	μA
I <sub>CC</sub>	supply current	OE = 0 V or V <sub>CC(A)</sub> ; An, Bn open					
		I <sub>CC(A)</sub>					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	2.4	-	15	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2.2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-1	-	-8	μA
		I <sub>CC(B)</sub>					
		V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	12	-	30	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-1	-	-5	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	1	-	6	μA
		I <sub>CC(A)</sub> + I <sub>CC(B)</sub>					
V <sub>CC(A)</sub> = 1.65 V to 3.6 V; V <sub>CC(B)</sub> = 2.3 V to 5.5 V	-	14.4	-	45	μA		

[1] V<sub>CC(A)</sub> must be less than or equal to V<sub>CC(B)</sub> and V<sub>CC(A)</sub> must not exceed 3.6 V.



## 12. Dynamic characteristics

**Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10; for waveforms see Fig. 7 to Fig. 9.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.8\text{ V} \pm 0.15\text{ V}$									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	4.6	-	4.7	-	5.8	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	7.1	-	6.8	-	7.0	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	4.4	-	4.5	-	4.7	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	5.3	-	4.5	-	0.5	ns
$t_{en}$	enable time	OE to A, B [1]	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	140	-	140	-	145	ns
		OE to B	-	125	-	175	-	125	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port	3.3	10.8	2.7	9.1	2.7	7.6	ns
$t_{THL}$	HIGH to LOW output transition time	A port	2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port	2.9	7.6	2.8	7.5	2.8	10.0	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
$t_W$	pulse width	data inputs	41	-	41	-	41	-	ns
$f_{data}$	data rate		-	24	-	24	-	24	Mbps

## Dual supply translating transceiver; open drain; auto direction sensing

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	3.2	-	3.3	-	3.4	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	3.5	-	4.4	-	4.6	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	3.0	-	3.6	-	4.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	2.5	-	1.6	-	0.7	ns
$t_{en}$	enable time	OE to A, B [1]	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	35	-	35	-	35	ns
		OE to A	-	105	-	105	-	105	ns
		OE to B	-	125	-	175	-	120	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	2.8	7.5	2.6	6.6	1.8	6.5	ns
		B port	3.2	8.5	2.9	7.3	2.4	6.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port	1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port	2.2	7.8	2.4	6.7	2.6	6.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.7	-	0.7	-	0.7	ns
$t_W$	pulse width	data inputs	41	-	41	-	41	-	ns
$f_{data}$	data rate		-	24	-	24	-	24	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	2.4	-	3.1	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	4.2	-	4.4	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	2.5	-	3.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	2.5	-	2.6	ns
$t_{en}$	enable time	OE to A, B [1]	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	-	-	35	-	35	ns
		OE to A	-	-	-	150	-	150	ns
		OE to B	-	-	-	170	-	120	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	2.3	6.2	1.9	6.3	ns
		B port	-	-	2.5	6.9	2.1	7.4	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	2.0	5.4	1.9	5.0	ns
		B port	-	-	2.3	7.4	2.4	7.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	-	-	0.7	-	0.7	ns
$t_W$	pulse width	data inputs	-	-	41	-	41	-	ns
$f_{data}$	data rate		-	-	-	24	-	24	Mbps

[1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] These values are guaranteed by design.

[3] Skew between any two outputs of the same package switching in the same direction.

## Dual supply translating transceiver; open drain; auto direction sensing

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10; for waveforms see Fig. 7 to Fig. 9.

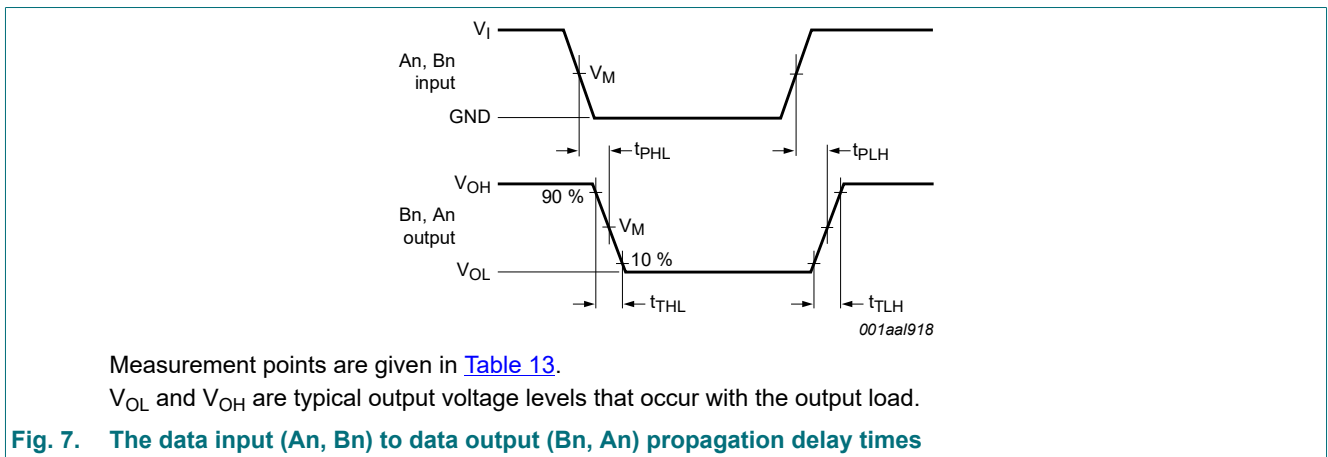
Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.8\text{ V} \pm 0.15\text{ V}$									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	0.7	ns
$t_{en}$	enable time	OE to A, B [1]	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	140	-	140	-	145	ns
		OE to B	-	125	-	175	-	125	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
$t_{THL}$	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs	50	-	41	-	41	-	ns
$f_{data}$	data rate		-	20	-	24	-	24	Mbps
$V_{CC(A)} = 2.5\text{ V} \pm 0.2\text{ V}$									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	0.9	ns
$t_{en}$	enable time	OE to A, B [1]	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A, B; no external load [1] [2]	-	45	-	45	-	45	ns
		OE to A	-	105	-	105	-	105	ns
		OE to B	-	125	-	175	-	120	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
$t_{sk(o)}$	output skew time	between channels [3]	-	0.8	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs	50	-	41	-	41	-	ns
$f_{data}$	data rate		-	20	-	24	-	24	Mbps

Dual supply translating transceiver; open drain; auto direction sensing

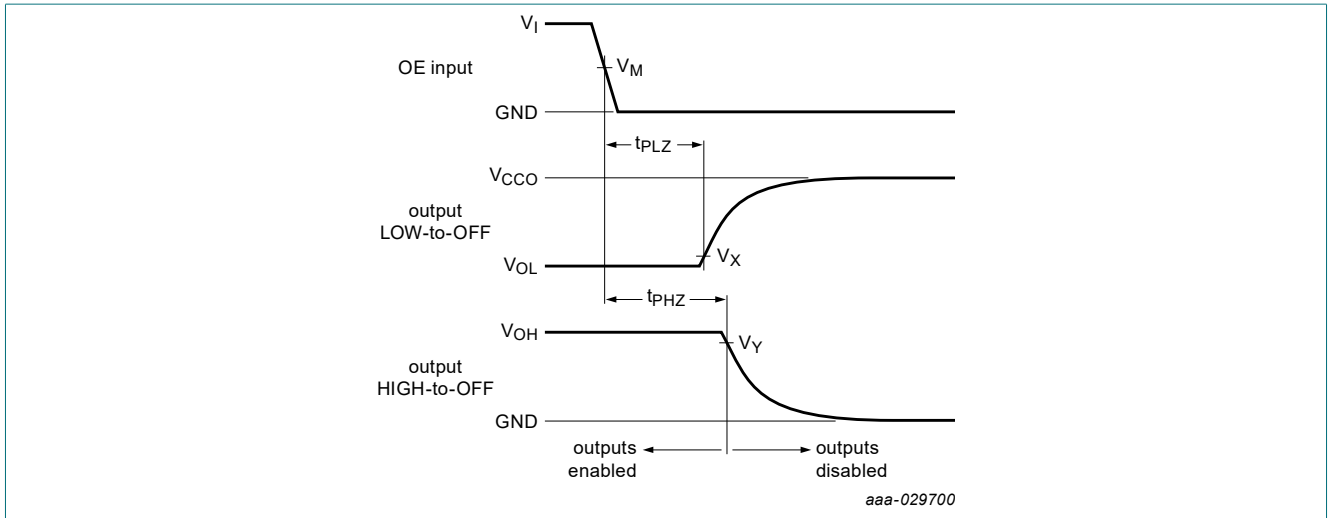
Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit	
			$2.5\text{ V} \pm 0.2\text{ V}$		$3.3\text{ V} \pm 0.3\text{ V}$		$5.0\text{ V} \pm 0.5\text{ V}$			
			Min	Max	Min	Max	Min	Max		
$V_{CC(A)} = 3.3\text{ V} \pm 0.3\text{ V}$										
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns	
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns	
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns	
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns	
$t_{en}$	enable time	OE to A, B	[1]	-	-	200	-	200	ns	
$t_{dis}$	disable time	OE to A, B; no external load	[1] [2]	-	-	45	-	45	ns	
		OE to A		-	-	150	-	150	ns	
		OE to B		-	-	170	-	120	ns	
$t_{TLH}$	LOW to HIGH output transition time	A port		-	-	2.3	7.0	1.9	7.4	ns
		B port		-	-	2.5	8.0	2.1	9.3	ns
$t_{THL}$	HIGH to LOW output transition time	A port		-	-	2.0	6.8	1.9	6.3	ns
		B port		-	-	2.3	9.3	2.4	9.5	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	0.8	-	0.8	ns
$t_W$	pulse width	data inputs		-	-	41	-	41	-	ns
$f_{data}$	data rate			-	-	-	24	-	24	Mbps

- [1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [2] These values are guaranteed by design.
- [3] Skew between any two outputs of the same package switching in the same direction.

12.1. Waveforms and test circuit

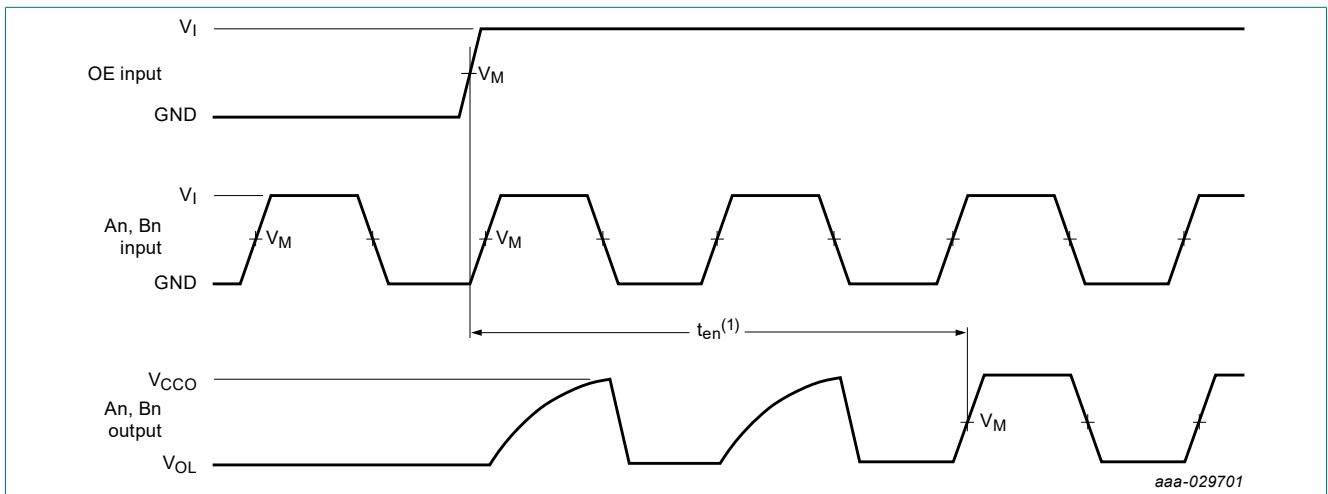


Dual supply translating transceiver; open drain; auto direction sensing



Measurement points are given in [Table 13](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.  
 $V_{CCO}$  is the supply voltage associated with the output.

**Fig. 8. Disable times**



(1) The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. See also [Section 13.6](#)  
 Measurement points are given in [Table 13](#).  
 $V_{OL}$  is a typical output voltage level that occur with the output load.  
 $V_{CCO}$  is the supply voltage associated with the output.

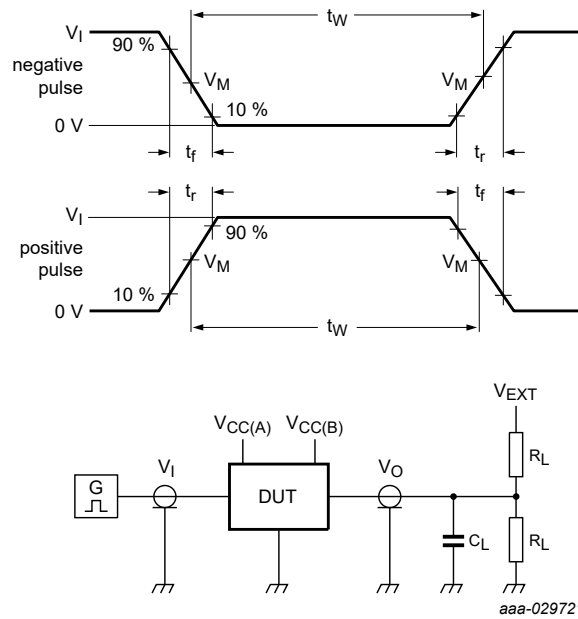
**Fig. 9. Enable times**

**Table 13. Measurement points**

Supply voltage	Input	Output		
$V_{CCO}$	$V_M$ [1]	$V_M$ [2]	$V_X$	$V_Y$
1.8 V ± 0.15 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.5 V ± 0.2 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.3 V ± 0.3 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
5.0 V ± 0.5 V	0.5 $V_{CCI}$	0.5 $V_{CCO}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

[1]  $V_{CCI}$  is the supply voltage associated with the input.  
 [2]  $V_{CCO}$  is the supply voltage associated with the output.

Dual supply translating transceiver; open drain; auto direction sensing



Test data is given in [Table 14](#).

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz; Z<sub>O</sub> = 50 Ω; dV/dt ≥ 1.0 V/ns.

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

V<sub>EXT</sub> = External voltage for measuring switching times.

**Fig. 10. Test circuit for measuring switching times**

**Table 14. Test data**

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	V <sub>I</sub> [1]	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> [2]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> [3]
1.65 V to 3.6 V	2.3 V to 5.5 V	V <sub>CCI</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub>

[1] V<sub>CCI</sub> is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ.

For measuring enable and disable times, R<sub>L</sub> = 50 kΩ.

[3] V<sub>CCO</sub> is the supply voltage associated with the output.

## 13. Application information

### 13.1. Applications

Voltage level-translation applications. The NXS0104 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I<sup>2</sup>C or 1-wire which use open-drain drivers, it may also be used in applications where push-pull drivers are connected to the ports, however the NXB0104 may be more suitable.

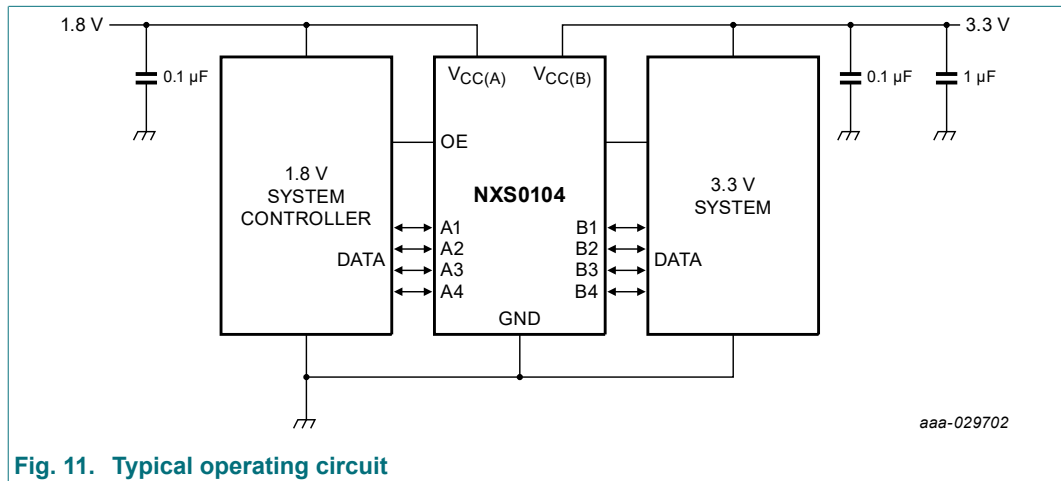


Fig. 11. Typical operating circuit

### 13.2. Architecture

The architecture of the NXS0104 is shown in Fig. 12. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

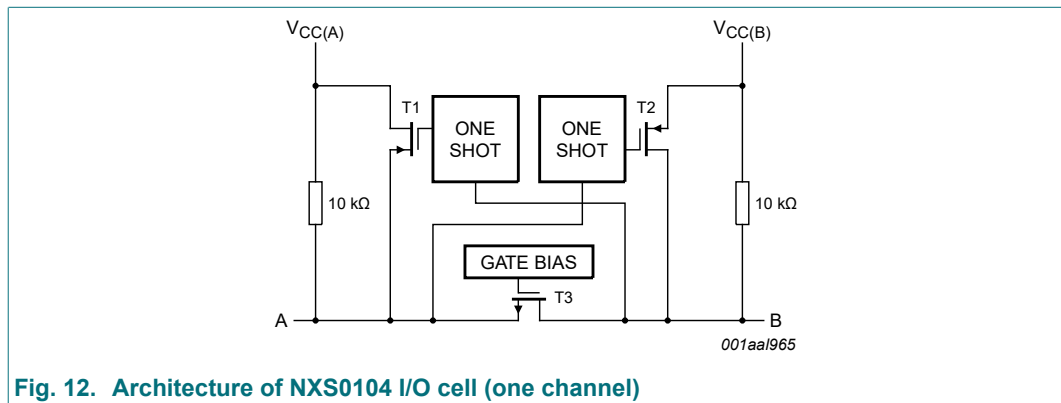


Fig. 12. Architecture of NXS0104 I/O cell (one channel)

The NXS0104 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the  $V_{CC}$  level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10 kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately  $0.5V_{CC}$ ; it is de-activated approximately 50 ns after the output reaches  $0.5V_{CC}$ . During the acceleration time the driver output resistance is between approximately 50 Ω and 70 Ω.

## Dual supply translating transceiver; open drain; auto direction sensing

To avoid signal contention and minimize dynamic  $I_{CC}$ , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

### 13.3. Input driver requirements

As the NXS0104 is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time ( $t_{THL}$ ) and propagation delay ( $t_{PHL}$ ) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50  $\Omega$  is used.

### 13.4. Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on NXS0104 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration.

### 13.5. Power up

During operation  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ , however during power-up  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so any power supply can be ramped up first. There is no special power-up sequencing required. The NXS0104 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 13.6. Enable and disable

An output enable input (OE) is used to disable the device. Setting OE to LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### 13.7. Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(A)}$ , and each B port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(B)}$ . If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 k $\Omega$ , this will effect the  $V_{OL}$  level. When OE goes LOW the internal pull-ups of the NXS0104 are disabled.



14. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

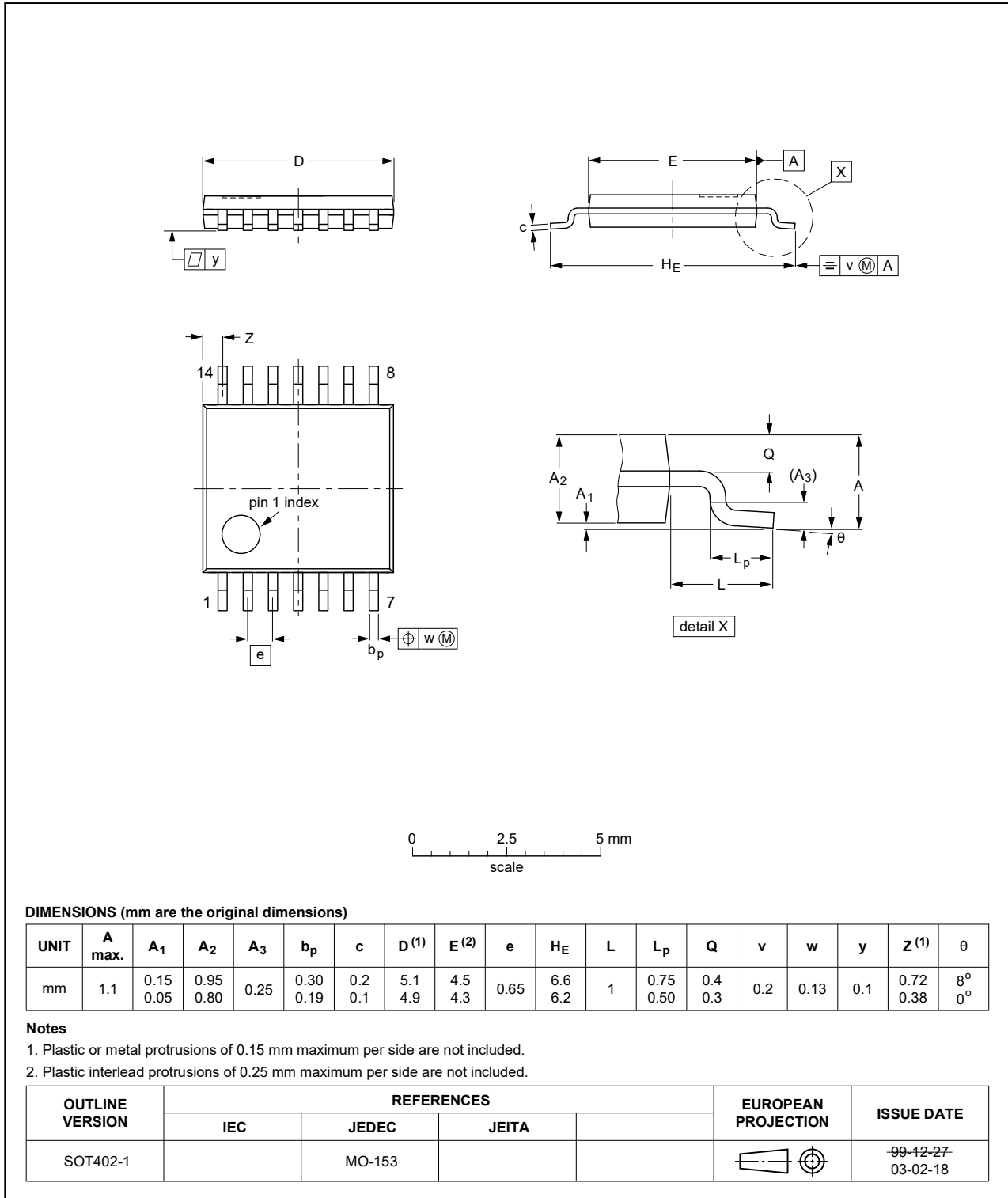


Fig. 13. Package outline SOT402-1 (TSSOP14)

Dual supply translating transceiver; open drain; auto direction sensing

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 14. Package outline SOT762-1 (DHVQFN14)

XQFN12: plastic, extremely thin quad flat package; no leads;  
12 terminals; body 1.70 x 2.00 x 0.50 mm

SOT1174-1

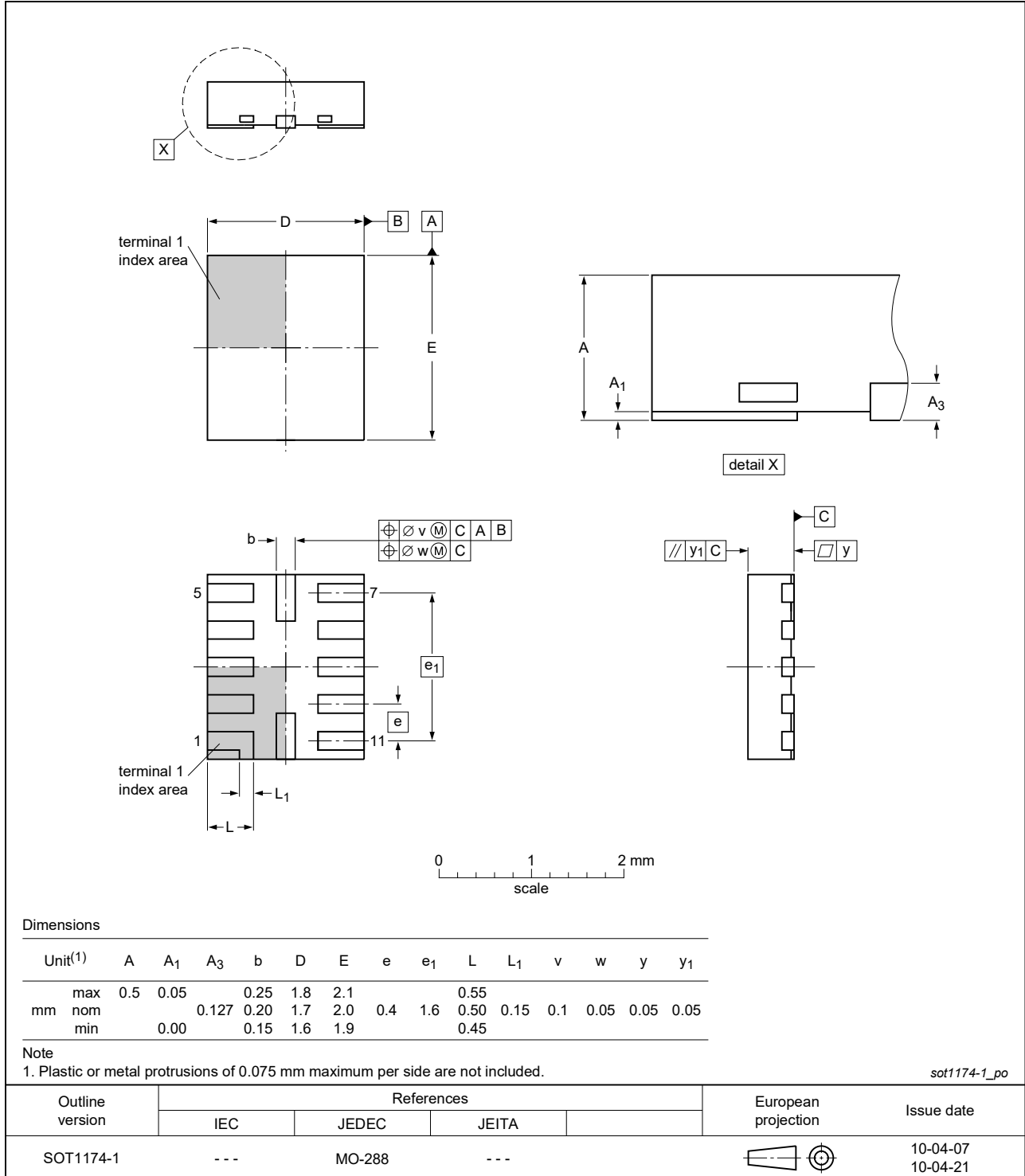


Fig. 15. Package outline SOT1174-1 (XQFN12)

WLCSP12: wafer level chip-scale package, 12 bumps; 1.36 x 1.86 x 0.60 mm

SOT8019-1

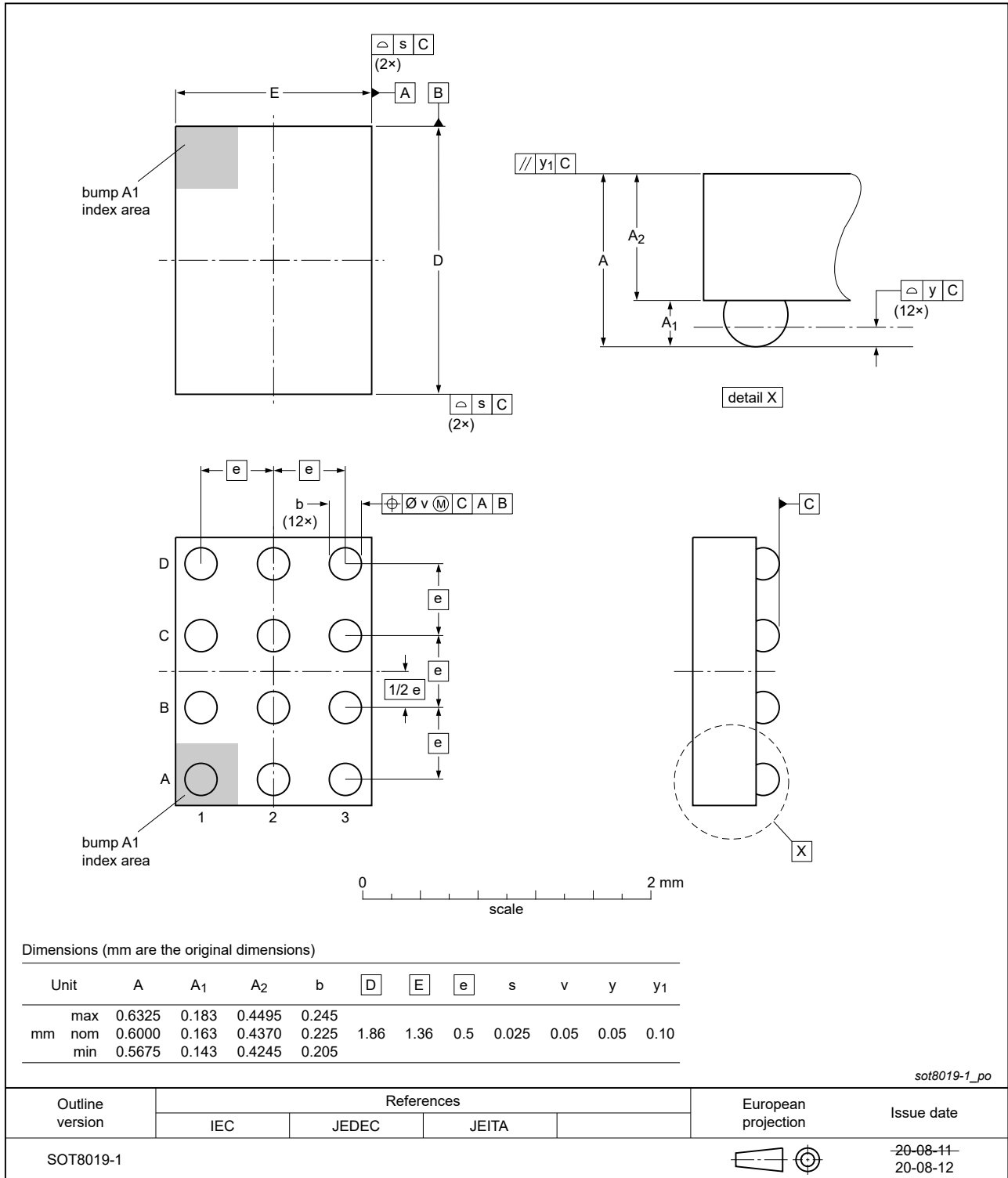


Fig. 16. Package outline SOT8019-1 (WLCSP12)

## 15. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
PCB	Printed Circuit Board
PRR	Pulse Rate Repetition

## 16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXS0104 v.4	20210630	Product data sheet	-	NXS0104 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type number NXS0104UM (SOT8019-1 / WLCSP12) added.</li> </ul>			
NXS0104 v.3	20201113	Product data sheet	-	NXS0104 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 11</a> and <a href="#">Table 12</a>: Disable times updated..</li> </ul>			
NXS0104 v.2	20200827	Product data sheet	-	NXS0104 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 6</a>: Derating values for P<sub>tot</sub> total power dissipation updated.</li> <li><a href="#">Table 11</a> and <a href="#">Table 12</a>: Footnotes corrected.</li> </ul>			
NXS0104 v.1	20190228	Product data sheet	-	-

## 17. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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