

General Description

The MAX17606 is a secondary-side synchronous driver and controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM) or Border Conduction Mode (BCM). By replacing the secondary diode with a MOSFET, the device improves the efficiency and simplifies thermal management. The 7V  $V_{DRV}$  of the device makes it suitable for switching both logic-level and standard MOSFETs used for flyback synchronous rectification. The 36V input voltage allows it to drive from either the output voltage or rectified drain voltage of the secondary MOSFET. Programmable minimum on and off-times provide flexibility needed to handle transformer parasitic element-related ringing in a robust manner. With 2A/4A source/sink currents, the MAX17606 is ideal for driving low  $R_{DS(on)}$  power MOSFETs with fast gate transition times.

Benefits and Features

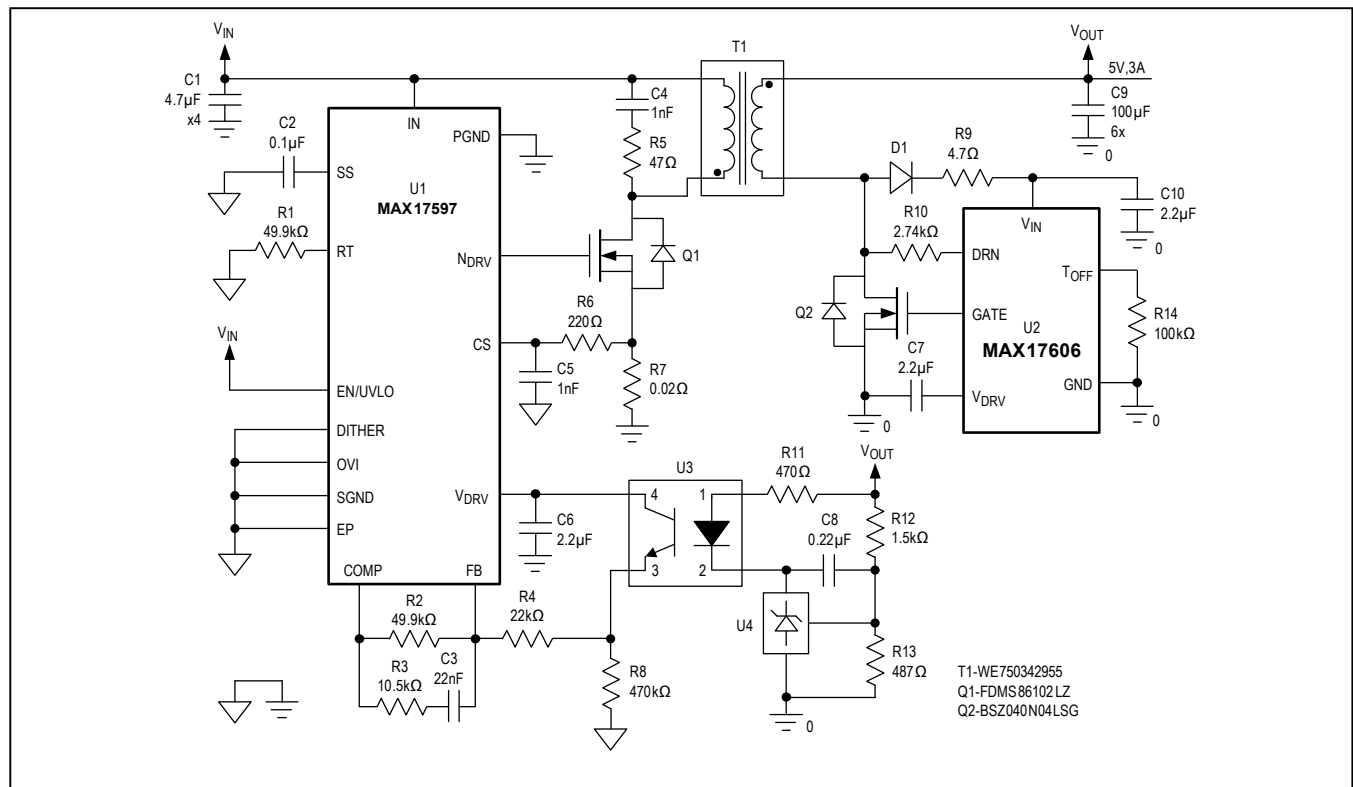
- Wide 4.5V to 36V Input
- 2A/4A Peak Source/Sink Gate Drive Currents
- Suitable for Discontinuous Conduction Mode (DCM), Border Conduction Mode (BCM)
- 320 $\mu$ A (typ) Low Quiescent Current
- Programmable Turn-Off Trip Point
- Programmable Minimum Off-Time to Handle DCM Ringing
- Thermal-Shutdown Protection
- 6-Lead SOT-23 Package

Applications

- High-Efficiency Isolated Flyback Converters

*Ordering Information appears at end of data sheet.*

Typical Application Circuit for 24V to 5V, 3A Isolated Flyback Converter



**Absolute Maximum Ratings**

V <sub>IN</sub> to GND	-0.3V to +40V	Continuous Power Dissipation (multilayer board) (T <sub>A</sub> = +70°C, derate 9.1mW/°C above +70°C.).....727.3mW Operating Temperature Range ..... -40°C to +125°C Junction Temperature ..... +150°C Storage Temperature Range ..... -40°C to +150°C Soldering Temperature (reflow) ..... +260°C
T <sub>OFF</sub> to GND	-0.3V to +6V	
DRN (low impedance source) to GND	-0.3V to +70V	
DRN to GND (up to 5mA of pull out current)	Self-Limiting	
GATE to GND	-0.3V to V <sub>DRV</sub> + 0.3V	
V <sub>DRV</sub> to GND	-0.3V to Min (V <sub>IN</sub> + 0.3, 18)V	
Continuous Power Dissipation (single-layer board) (T <sub>A</sub> = +70°C, derate 2.7mW/°C above +70°C.).....	219.1mW	

**Package Thermal Characteristics (Note 1)**

SOT-23 6L	Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) ..... 110°C/W	Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ).....50°C/W
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**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

V<sub>IN</sub> = 12V, C<sub>VIN</sub> = 100nF, C<sub>VDRV</sub> = 2.2µF, GATE = OPEN, DRN = 0V, GND = 0V, R<sub>TOFF</sub> = 40.2kΩ, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C. All voltages are referenced to GND, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>V<sub>IN</sub></b>						
V <sub>IN</sub> Operating Range	V <sub>IN</sub>		4.5		36	V
V <sub>IN</sub> Quiescent Current	I <sub>Q</sub>	DRN = 2V, no switching		320	450	µA
V <sub>IN</sub> Switching Current	I <sub>SW</sub>	DRN switching -150mV to +2V, 300kHz, 50% duty cycle		600		µA
<b>V<sub>DRV</sub></b>						
V <sub>DRV</sub> Regulation Voltage	V <sub>DRV_LOAD</sub>	1mA ≤ V <sub>DRV</sub> ≤ 20mA	6.6	7.0	7.4	V
V <sub>DRV</sub> Regulation Voltage	V <sub>DRV_LINE</sub>	I <sub>VDRV</sub> = 1mA; 8.5V ≤ V <sub>IN</sub> ≤ 36V	6.6	7.0	7.4	V
V <sub>DRV</sub> Dropout Voltage	V <sub>DRV-DO</sub>	I <sub>VDRV</sub> = 20mA, V <sub>IN</sub> = 4.5V	4.1	4.3		V
V <sub>DRV</sub> Current Limit	I <sub>VDRV</sub>	V <sub>DRV</sub> = 6V; V <sub>IN</sub> = 8.5V	26.5	55		mA
V <sub>DRV</sub> Undervoltage Lockout	V <sub>DRV-UVR</sub>	V <sub>DRV</sub> rising	4.0	4.25	4.47	V
	V <sub>DRV-UVH</sub>	V <sub>DRV</sub> falling	3.75	4	4.25	V
<b>DRN</b>						
Maximum Drain Operating Voltage	V <sub>DRN</sub>				60	V
GATE Turn-On Detect Threshold	V <sub>GATE-ON</sub>		-150	-94		mV
GATE Turn-Off Detect Threshold	V <sub>GATE-OFF</sub>		24	30	35	mV
DRN Rising Threshold for T <sub>OFF</sub> Enable	V <sub>DRN-TOFF_EN</sub>	DRN voltage rising		0.87		V
DRN Bias Current	IDRN	R <sub>TOFF</sub> = 40.2KΩ, DRN = 0V	26.5	30.5	34.5	µA

**Electrical Characteristics (continued)**

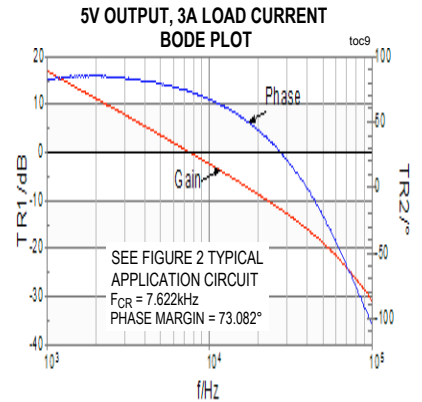
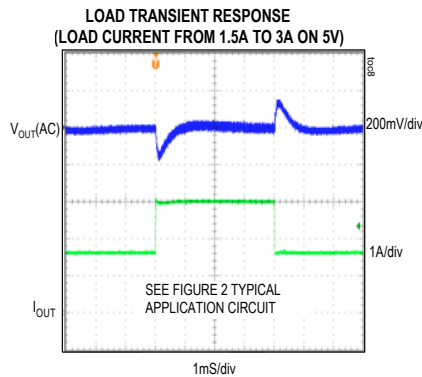
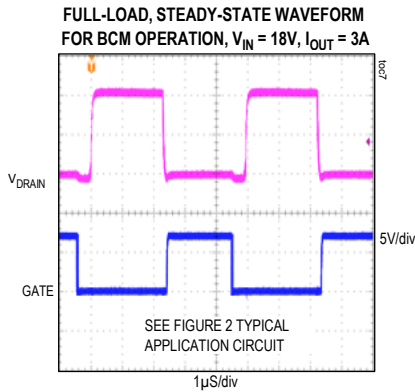
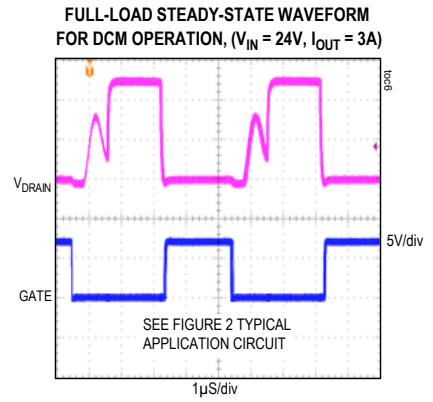
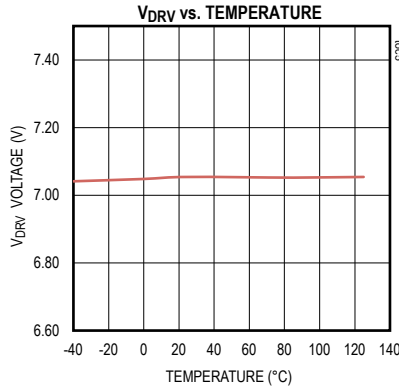
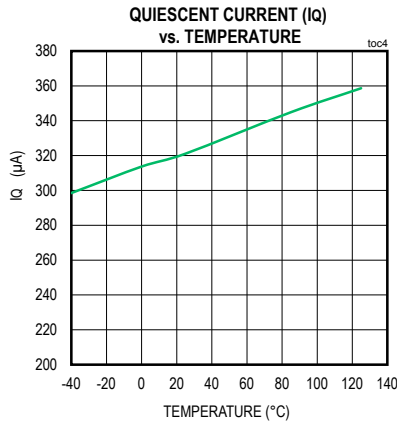
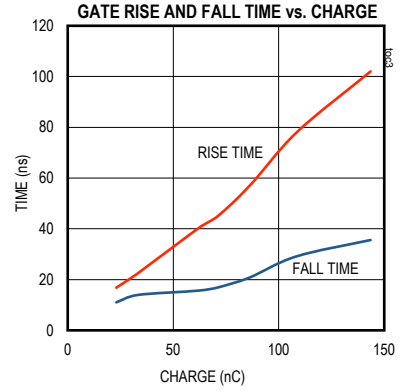
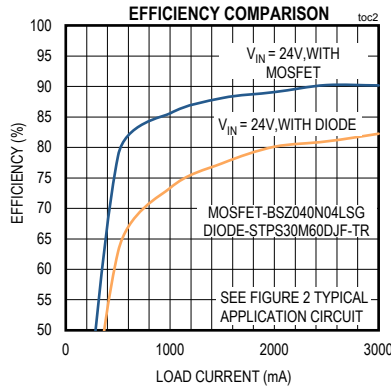
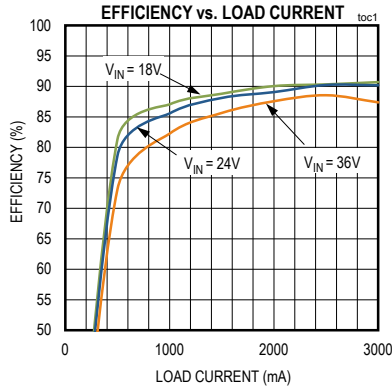
$V_{IN} = 12V$ ,  $C_{VIN} = 100nF$ ,  $C_{VDRV} = 2.2\mu F$ , GATE = OPEN, DRN = 0V, GND = 0V,  $R_{TOFF} = 40.2k\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to GND, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SWITCHING CHARACTERISTICS (GATE, <math>T_{OFF}</math>)</b>						
GATE Output Pullup Resistance	$R_{ON-P}$	$V_{IN} = V_{DRV} 7V$ , $I_{GATE} = -50mA$		1.5	2.8	$\Omega$
GATE Output Pulldown Resistance	$R_{ON-N}$	$V_{IN} = 7V$ , $I_{GATE} = 190mA$		0.5	0.9	$\Omega$
GATE Peak Source Current	$I_{G-SOURCE}$			2		A
GATE Peak Sink Current	$I_{G-SINK}$			4		A
Turn-On Propagation Delay	$T_{ON-D}$	DRN falling to gate rising		26	40	ns
Turn-Off Propagation Delay	$T_{OFF-D}$	DRN rising to gate falling		32	50	ns
$T_{OFF}$ Programmable range	$T_{OFF}$		115		1550	ns
$T_{OFF}$ Accuracy		$R_{TOFF} = 40.2k\Omega$	315	425	540	ns
		$R_{TOFF} = 150k\Omega$	1150	1550	2000	ns
Minimum On-Time	$T_{ON\_MIN}$		150	240	330	ns

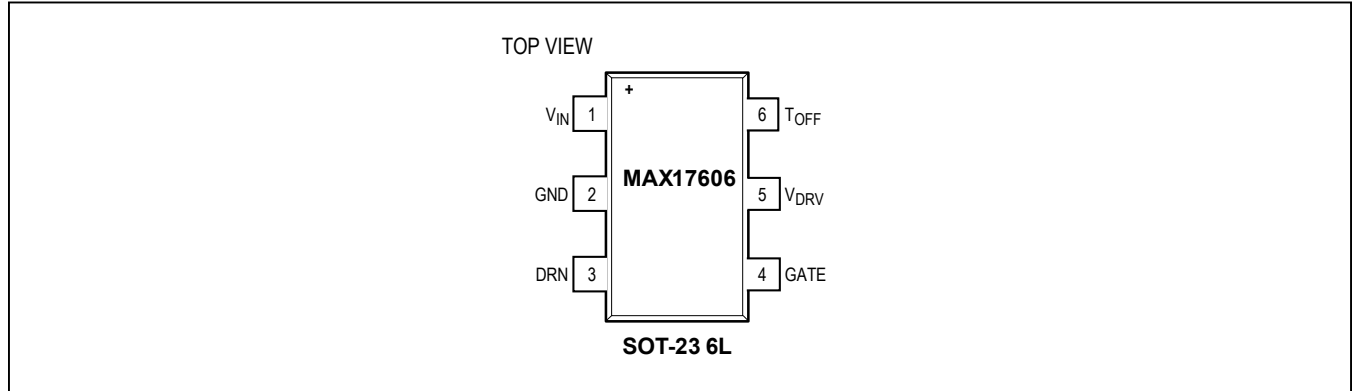
**Note 2:** Limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

Typical Operating Characteristics

$V_{IN} = 13V, V_{GND} = 0V, R_{TOFF} = 100k\Omega, R_{DRN} = 2.74k\Omega, C_{VDRV} = 2.2\mu F, T_A = +25^\circ C$ , unless otherwise noted.



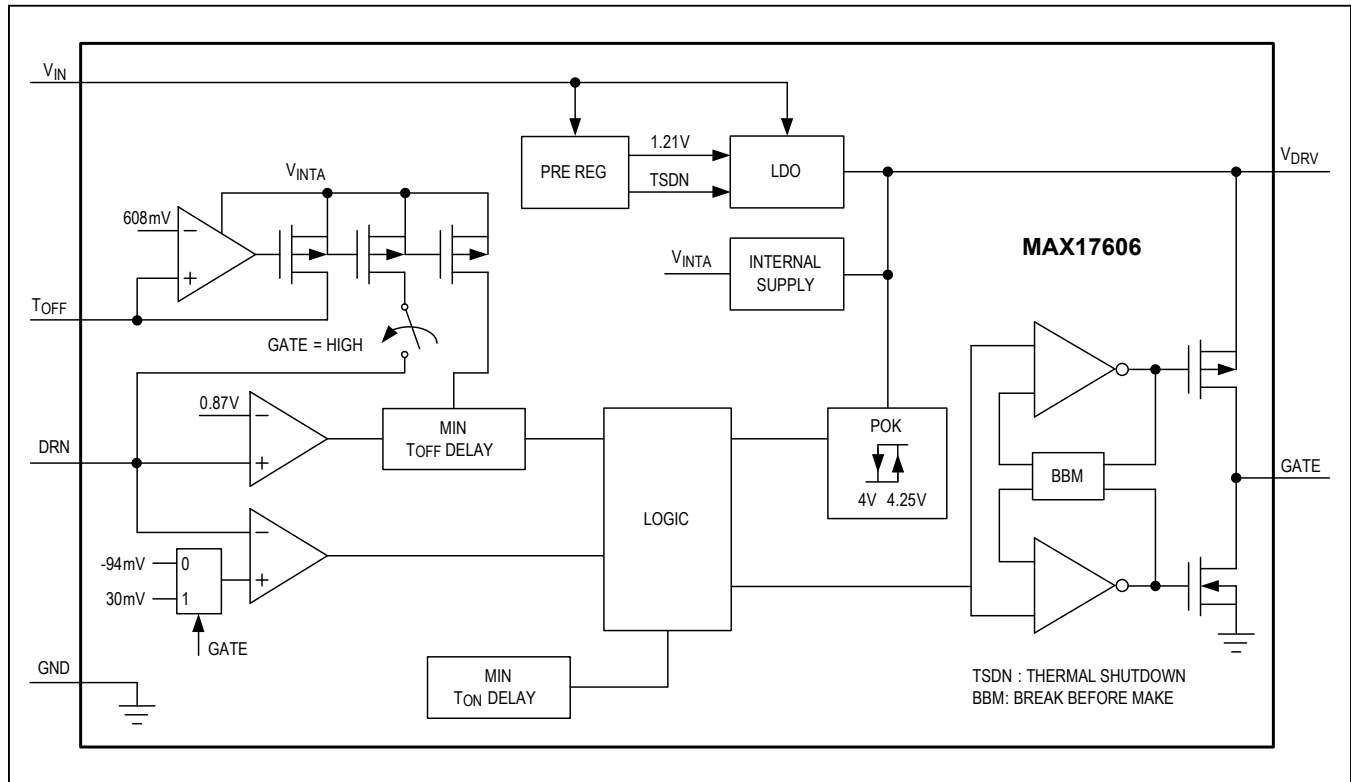
## Pin Configurations



## Pin Description

PIN	NAME	FUNCTION
1	V <sub>IN</sub>	Input Voltage. Connect at least 2.2μF X7R ceramic capacitor from V <sub>IN</sub> to GND for bypassing.
2	GND	IC Ground. The external MOSFET source should be kelvin connected to this pin. See the MAX17606 EV kit PCB for example layout.
3	DRN	Drain Sense Pin of the External MOSFET. Connect the external MOSFET drain to this pin through a resistor. See the MAX17606 EV kit PCB for example layout.
4	GATE	External nMOSFET GATE Driver Output.
5	V <sub>DRV</sub>	LDO Output and Driver Input. Connect a 2.2μF bypass capacitor from V <sub>DRV</sub> pin to GND, as close as possible to the IC. See the MAX17606 EV kit PCB for example layout.
6	T <sub>OFF</sub>	Connect a resistor from T <sub>OFF</sub> to GND to set the programmable minimum off time.

## Functional (or Block) Diagram



## Detailed Description

For low and medium-power applications, the flyback converter is the preferred choice due to its simplicity and low cost. However, in high-output-current applications, the high power dissipation and resulting need for thermal management of the secondary diode rectifier, is a concern. The MAX17606 eliminates this constraint by allowing replacement of the secondary diode with a synchronous rectifier nMOSFET. The use of an nMOSFET as the secondary synchronous rectifier reduces the power dissipation and improves the system efficiency, while providing a higher deliverable output current compared to a rectifier diode.

The device contains all the control and logic circuitry needed to implement a secondary-side synchronous rectifier in a flyback converter operating in DCM. Essentially, by sensing the drain-to-source voltage of the external nMOSFET, and turning on the nMOSFET with the correct timing, the device emulates an ideal diode rectifier. See [Principle of Operation](#) section for details.

## Principle of Operation

The MAX17606 uses the synchronous nMOSFET's body-diode forward voltage to determine when to drive the GATE pin high and turn on the nMOSFET. Whenever the voltage across the nMOSFET goes 94mV (typ) below ground, GATE is pulled-up to  $V_{DRV}$ . GATE is held high for a minimum duration of 240ns (typ) to make the device immune to ringing in the secondary current (caused by transformer leakage inductance). This ringing should be limited by using an RC snubber, RCD clamp, or both. This ringing period should not last longer than 150ns.

Noting that the voltage across the MOSFET drain-source terminals ( $V_{DS}$ ) is equal to  $R_{DS(on)}$  times the secondary current, the ideal point to turn-off the gate would be when secondary current is zero. However, MOSFET packages have a significant internal inductance and the high secondary  $di/dt$  through this lead inductance can create a positive voltage across the MOSFET. Also, to account for the turn-off propagation delay and to avoid the cross conduction, it is required to turn-off the MOSFET when a

positive current is flowing through the MOSFET. A series resistor ( $R_{\text{DRAIN}}$ ) connected between drain of the external MOSFET to the IC DRN pin with precise internal current source is used to program the turn-off trip point. When the DRN pin goes above +30mV (typ), the gate is pulled-down to GND. The following equation is used to program the turn-off trip point,

$$V_{\text{turn-off}} = 30\text{mV} - \frac{1.21}{R_{\text{TOFF}}} \times R_{\text{DRAIN}} - L_{\text{LEAD}} \times \frac{di_{\text{sec}}}{dt}$$

where,

$R_{\text{TOFF}}$  - The resistor connected between  $T_{\text{OFF}}$  pin to GND.

$R_{\text{DRAIN}}$  - The resistor connected between the DRN pin and drain of the MOSFET.

$L_{\text{LEAD}}$  - The sum of lead inductance of the MOSFET package on source and drain.

$\frac{di_{\text{sec}}}{dt}$  - is equal to  $V_{\text{OUT}} / (L_{\text{PRI}} \times K^2)$ ; and  $K = N_{\text{sec}}/N_{\text{PRI}}$

$V_{\text{TURN-OFF}}$  - RDS(on) times the secondary current at the desired turn-off secondary current.

Refer to the MOSFET data sheet, or consult with the MOSFET manufacturer, to determine the total inductance for the specific MOSFET being used in the application.

### Supply Voltage ( $V_{\text{IN}}$ )

The MAX17606 has a wide input voltage range from 4.5V to 36V. When the output voltage is 5V and greater,  $V_{\text{OUT}}$  can be directly used to drive  $V_{\text{IN}}$  as shown in [Figure 3](#). In this configuration, connect a series resistor of 22 $\Omega$  in  $V_{\text{IN}}$  path to limit the  $V_{\text{DRV}}$  capacitor discharge current during output short. For driving standard MOSFETS, rectified drain voltage of the secondary synchronous MOSFET is ideal choice to drive  $V_{\text{IN}}$ , when output voltage is 5V and lesser. In this configuration, connect a series resistor ( $R_9$ ) in the  $V_{\text{IN}}$  path to limit the current in the rectifier diode (D1) as shown in [Figure 2](#).

### Linear Regulator ( $V_{\text{DRV}}$ )

The  $V_{\text{IN}}$  powers internal LDO of the device. The regulated output of the LDO is connected to the  $V_{\text{DRV}}$ . The LDO output voltage is 7V (typ) and has a current limit of 55mA (typ). Connect a minimum of 2.2 $\mu\text{F}$  ceramic capacitor between  $V_{\text{DRV}}$  and GND, for the stable operation over the full temperature range. Place this capacitor close to the IC.

### Programmable $T_{\text{OFF}}$ Pin Resistor ( $R_{\text{TOFF}}$ )

After the synchronous MOSFET has turned off, we observe a ringing across the drain to source due to voltage oscillations caused by magnetizing inductance and the MOSFET drain node capacitance. In some cases, this ringing causes the DRN pin of the device to go 94mV below ground. This may trigger the turn-on threshold comparator and turn-on the gate pulse. To avoid this fault triggering, every time the DRN pin goes above 0.87V, the device introduces a minimum  $T_{\text{OFF}}$  time and blanks the next turn-on threshold comparison during this time. After the minimum  $T_{\text{OFF}}$  is elapsed, next time the DRN pin goes 94mV below ground the gate will be pulled high to  $V_{\text{DRV}}$ . The resistor connected between the  $T_{\text{OFF}}$  pin to GND sets the minimum  $T_{\text{OFF}}$  time.

$$R_{\text{TOFF}} = \frac{T_{\text{OFF}} - 13(\text{typ})}{10.25}$$

where,

$R_{\text{TOFF}}$  - The resistor connected between the  $T_{\text{OFF}}$  pin to GND in k $\Omega$ .

$T_{\text{OFF}}$  - The minimum  $T_{\text{OFF}}$  time in ns.

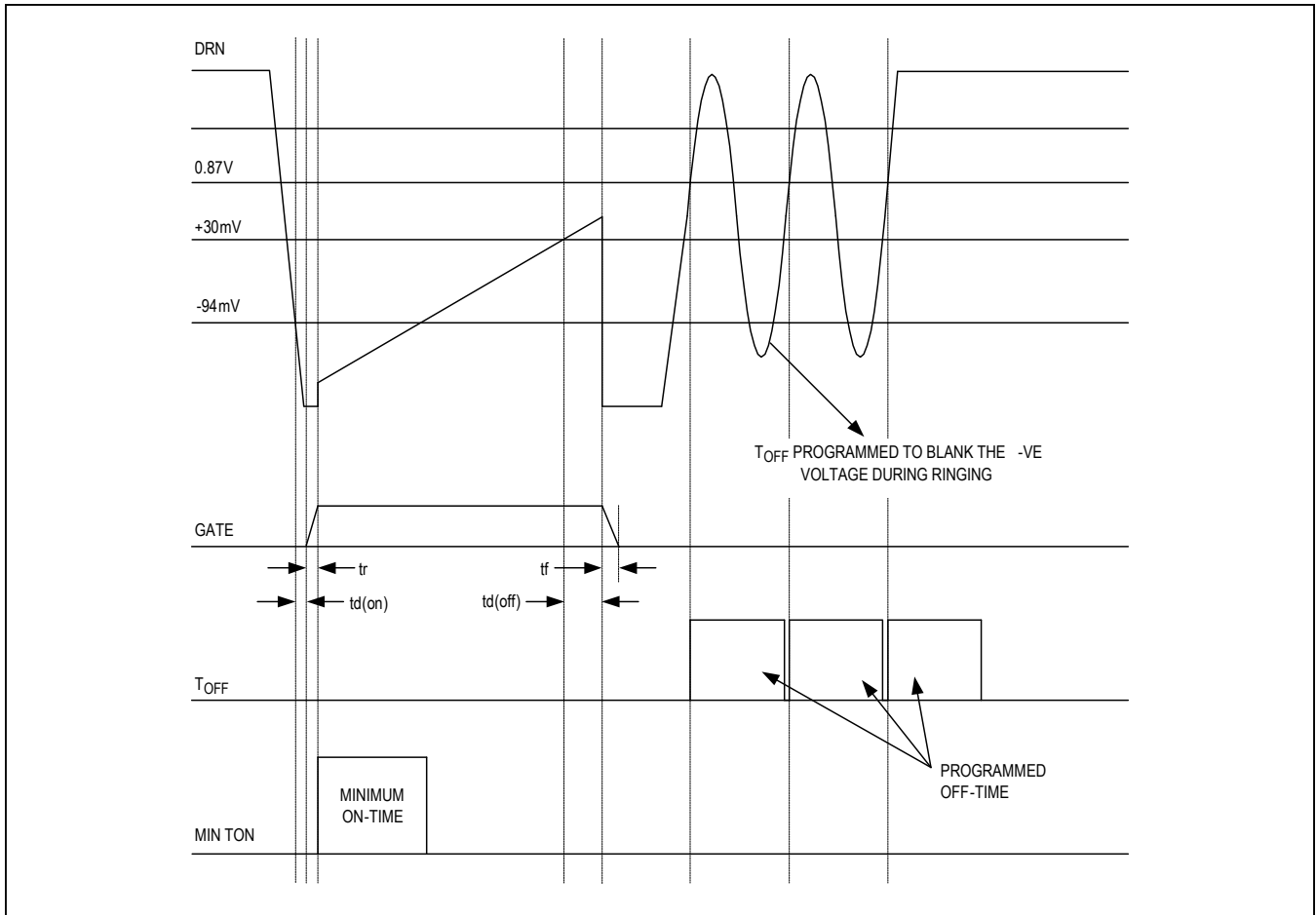


Figure 1. Timing Diagram of MAX17606:

### PCB Layout guidelines

Careful PCB layout is critical to achieve clean and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17606 evaluation kit layouts available at [www.maximintegrated.com](http://www.maximintegrated.com).

Follow the below guidelines for good PCB layout:

- 1) The loop area of paths carrying the pulsed currents should be kept as small as possible.
- 2)  $V_{DRV}$  and  $V_{IN}$  bypass capacitors should be connected close to the respective pins and returned to GND pin of the IC. This loop area should be as small as possible.
- 3) The proper sensing of drain-to-source voltage across the MOSFET is critical in this IC. The  $R_{DRAIN}$  should be kelvin connected to the drain of the Synchronous MOSFET. The source pin of the MOSFET should be kelvin connected to the IC GND pin as well.
- 4) Connect the  $R_{TOFF}$  resistor directly between  $T_{OFF}$  pin and the IC GND pin. The return path should not be connected to ground plane.



Typical Application Circuit

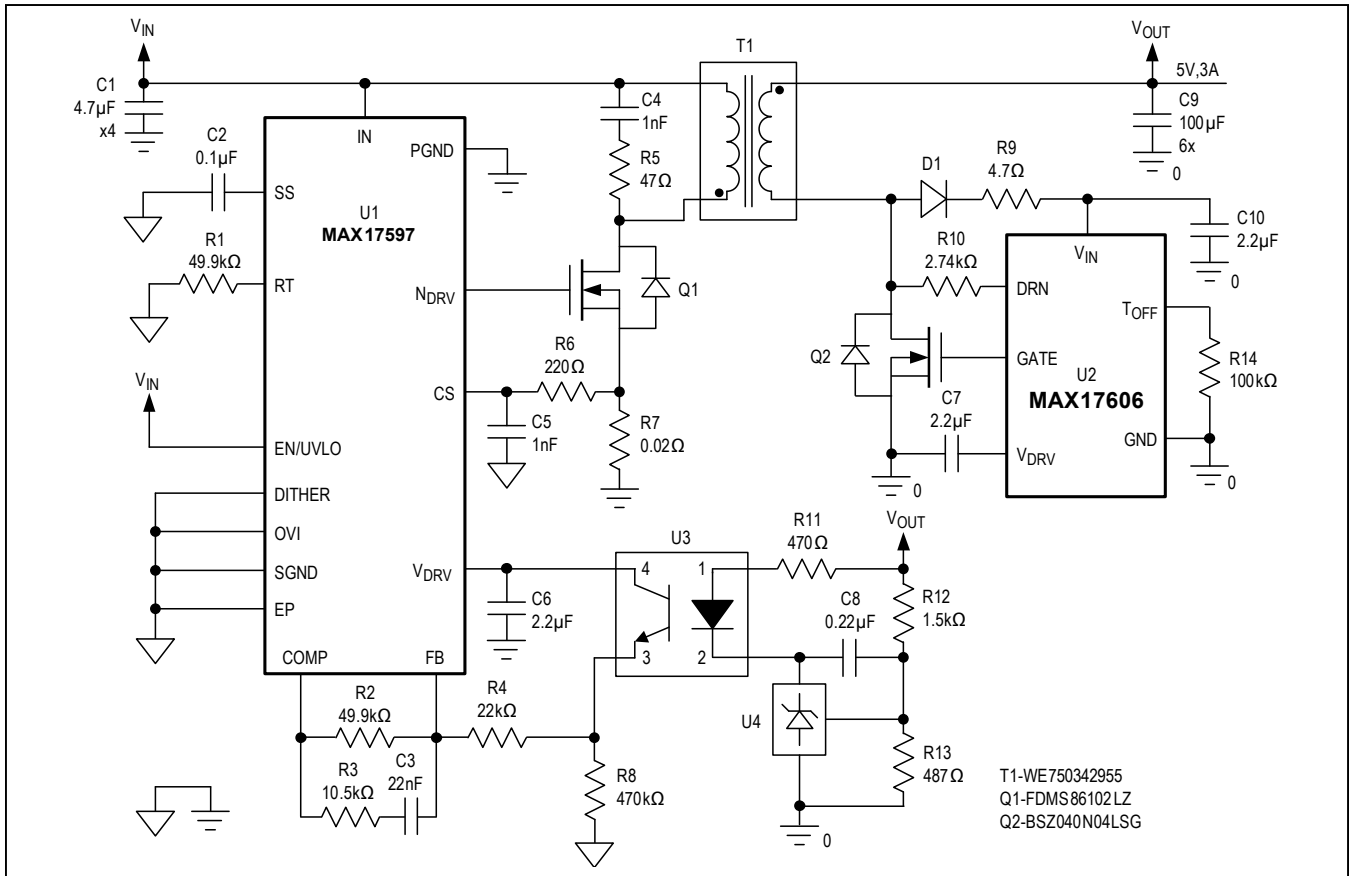


Figure 2. Typical Application Circuit for 24V to 5V, 3A Isolated Flyback Converter

Typical Application Circuit

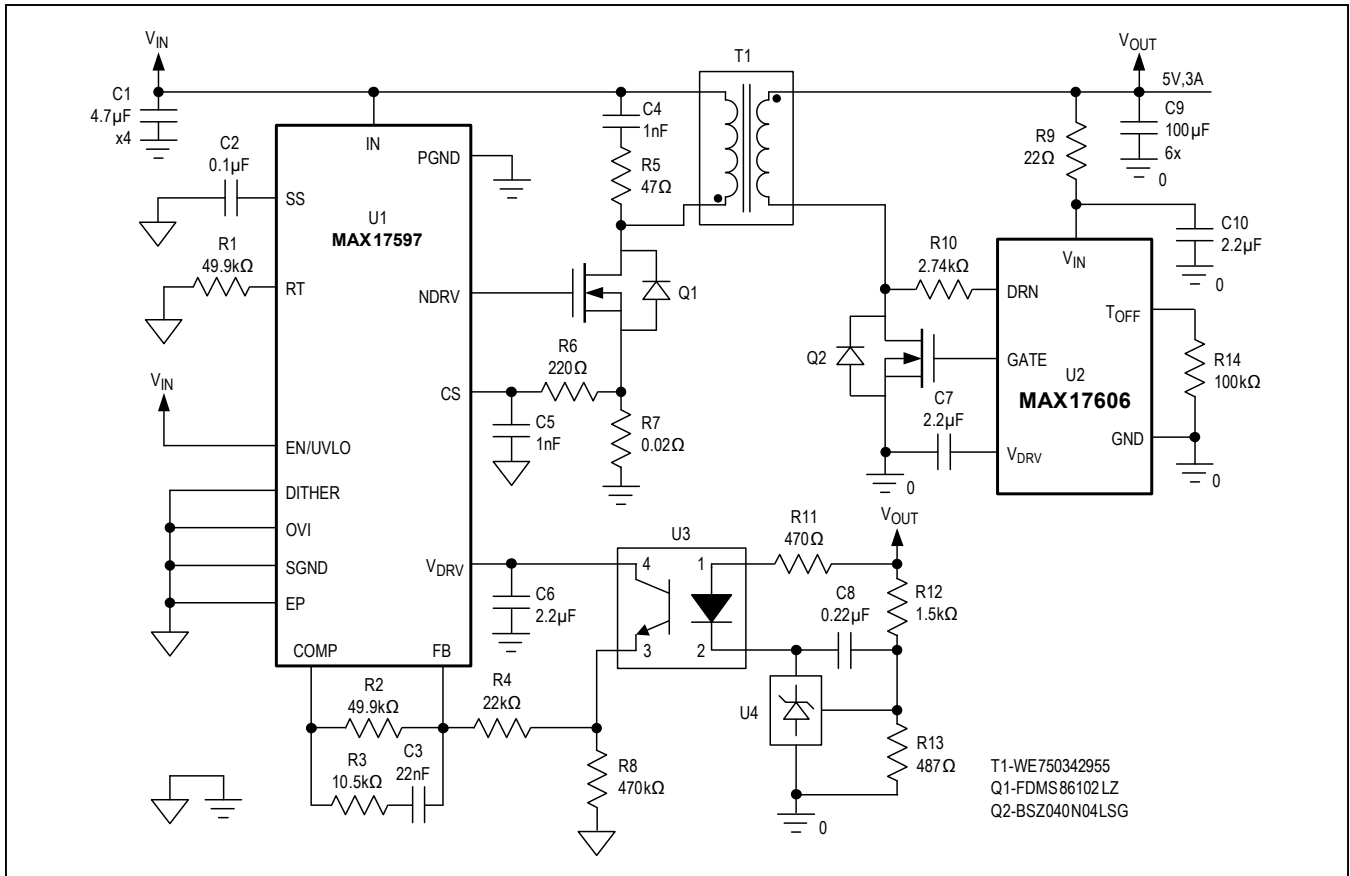


Figure 3. 24V to 5V, 3A Isolated Flyback Circuit, MAX17606 V<sub>IN</sub> Driven From V<sub>OUT</sub>

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17606AZT+	-40°C to +125°C	6-LEAD THIN SOT23

+Denotes a lead (Pb)-free/RoHS-compliant package

### Chip Information

PROCESS: BCD

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
TSOT23	Z6+1	<a href="#">21-0114</a>	<a href="#">90-0242</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/15	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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