74HC11-Q100; 74HCT11-Q100

Triple 3-input AND gate Rev. 4 — 11 August 2021

1. General description

The 74HC11-Q100; 74HCT11-Q100 is a triple 3-input AND gate. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)

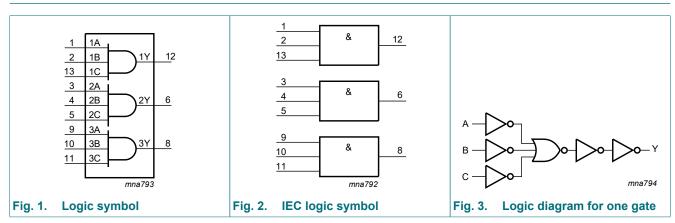
 Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
 - For 74HC11-Q100: CMOS level
 - For 74HCT11-Q100: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

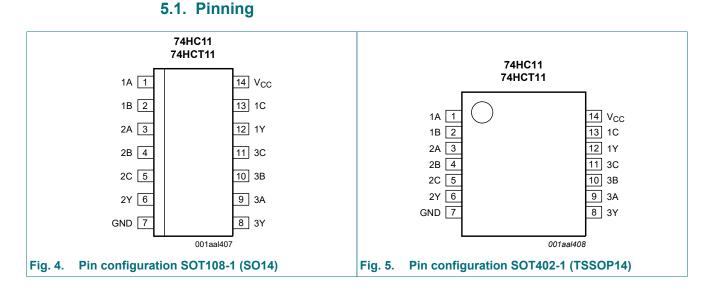
Table 1. Ordering in	formation			
Type number	Package			
	Temperature range	Name	Description	Version
74HC11D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74HCT11D-Q100	-		body width 3.9 mm	
74HC11PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package;	SOT402-1
74HCT11PW-Q100	-		14 leads; body width 4.4 mm	

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4. Functional diagram



5. Pinning information



5.2. Pin description

Table	2.	Pin	description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 9	data input
1B, 2B, 3B	2, 4, 10	data input
GND	7	ground (0 V)
1C, 2C, 3C	13, 5, 11	data input
1Y, 2Y, 3Y	12, 6, 8	data output
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input	iput			
nA	nB	nC	nY	
L	Х	Х	L	
Х	L	Х	L	
Х	Х	L	L	
Н	Н	Н	Н	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{\rm I}$ < -0.5 V or $V_{\rm I}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
Ι _{ΟΚ}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
lo	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter Conditions		74HC11-Q100			74HCT11-Q100			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	Unit	
			Min	Тур	Мах	Min	Мах	Min	Max	1
74HC11-	-Q100								-	
VIH	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0 V$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2.0	-	20	-	40	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	1-Q100									
V _{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
lı	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5 V$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	μA

Symbol	Parameter	Conditions	onditions 25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Мах	Min	Max	Min	Мах	1
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	100	360	-	450	-	490	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $C_L = 50 pF$; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Мах	Min	Max	Min	Max	
74HC11-	-Q100									
t _{pd}	propagation	nA, nB to nY; see Fig. 6 [1]								
	delay	V _{CC} = 2.0 V	-	32	100	-	125	-	150	ns
		V _{CC} = 4.5 V	-	12	20	-	25	-	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	10	17	-	21	-	26	ns
t _t	transition time	see <u>Fig. 6</u> [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per package; [3] $V_I = GND$ to V_{CC}	-	18	-	-	-	-	-	pF
74HCT1	1-Q100							·		
t _{pd}	propagation	nA, nB to nY; see Fig. 6 [1]								
	delay	V _{CC} = 4.5 V	-	16	24	-	30	-	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 6</u> [2]	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per package; [3] V _I = GND to V _{CC} - 1.5 V	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} . [2] t_t is the same as t_{THL} and t_{TLH} . [3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

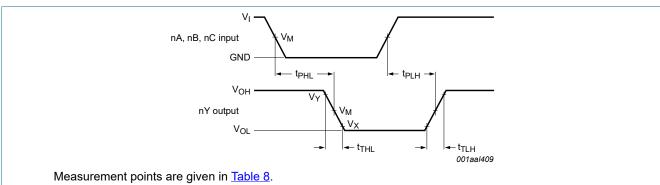
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

10.1. Waveforms and test circuit

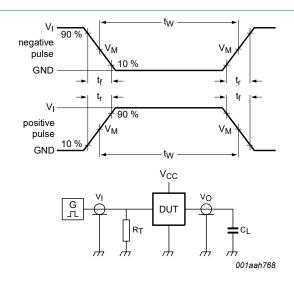


 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Dutput			
	V _M	V _M	V _X	V _Y	
74HC11-Q100	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}	
74HCT11-Q100	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}	



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data				
Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC11-Q100	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT11-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

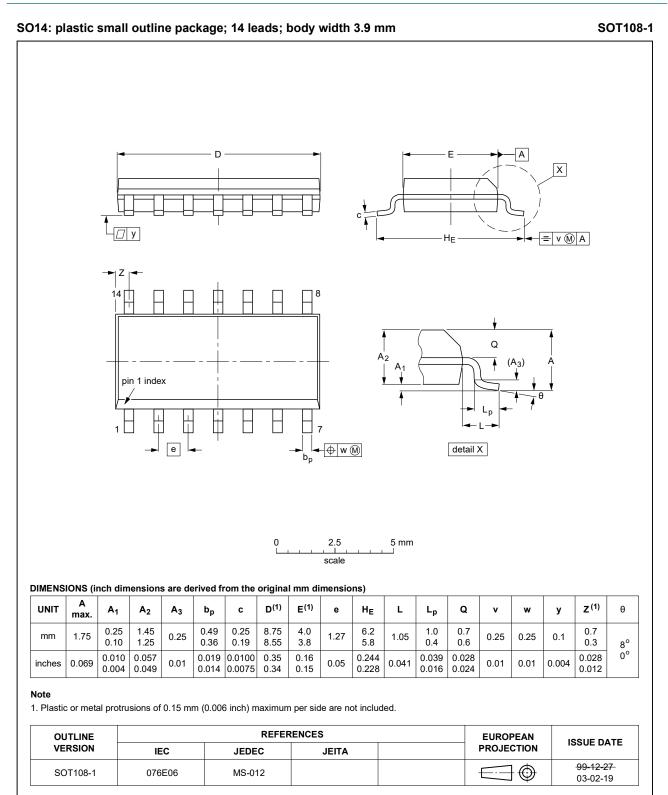


Fig. 8. Package outline SOT108-1 (SO14)

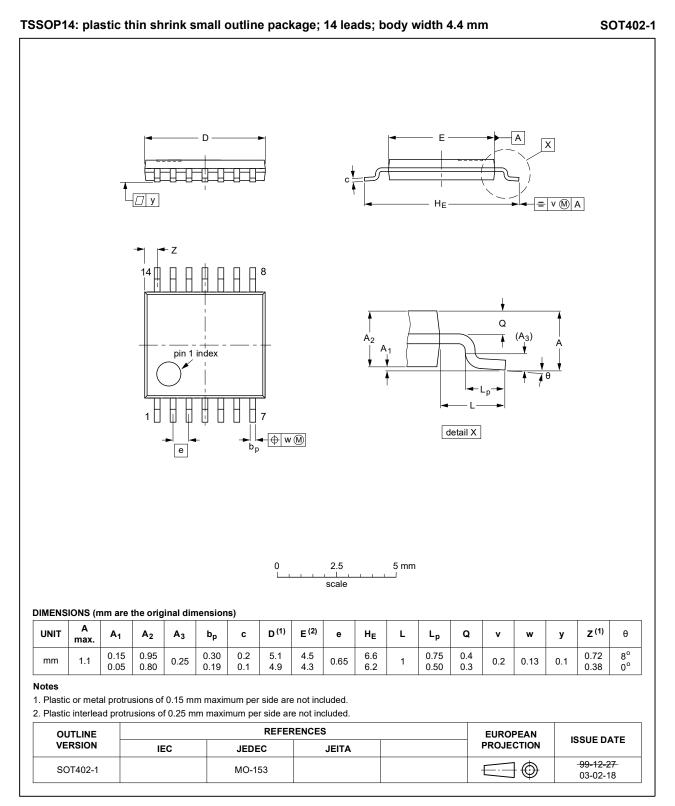


Fig. 9. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT11_Q100 v.4	20210811	Product data sheet	-	74HC_HCT11_Q100 v.3	
Modifications:	• <u>Section 2</u> updated.				
74HC_HCT11_Q100 v.3	20210108	Product data sheet	-	74HC_HCT11_Q100 v.2	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 7: Derating values for P_{tot} total power dissipation have been updated. 				
74HC_HCT11_Q100 v.2	20130322	Product data sheet	-	74HC_HCT11_Q100 v.1	
Modifications:	<u>Section 2</u> : Removed redundant temperature range.				
74HC_HCT11_Q100 v.1	20130228	Product data sheet	-	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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