MCP39F511N

Dual-Channel, Single-Phase Power-Monitoring IC with Calculation

Features

- Power Monitoring of Two Loads with accuracy of 0.5% across 4000:1 Dynamic Range
- Built-in Calculations on Fast 16-Bit Processing Core:
  - Active, Reactive, Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- 64-bit Wide Import and Export Active Energy Accumulation Registers Per Channel
- 64-bit Four Quadrant Reactive Energy Accumulation Registers Per Channel
- Signed Active and Reactive Power Outputs
- Dedicated Zero Crossing Detection (ZCD) Pin Output with Less than 200 µs Latency
- Dedicated PWM Output Pin with Programmable Frequency and Duty Cycle
- Automatic Event Pin Control through Fast Voltage Surge Detection
  - Less than 5 ms Delay
- Two-Wire Serial Protocol with Selectable Baud Rate up to 115.2 kbps using Universal Asynchronous Receiver/Transmitter (UART)
- Fast Calibration Routines and Simplified Command Protocol
- 512 Bytes User-Accessible EEPROM through Page Read/Write Commands
- Low-Drift Internal Voltage Reference, 10 ppm/°C Typical
- 28-lead 5x5 QFN Package
- Extended Temperature Range: -40°C to +125°C

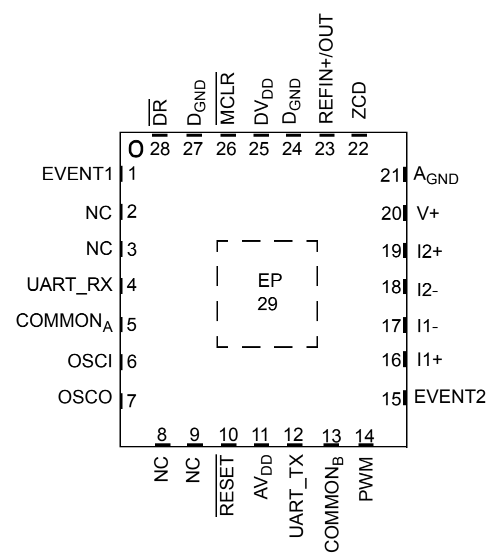
Applications

- Wall Socket (Dual Plug) Power Monitoring
- Power Monitoring for Home Automation
- Industrial Lighting Power Monitoring
- Real-Time Measurement of Input Power for AC/DC Supplies
- Intelligent Power Distribution Units

Description

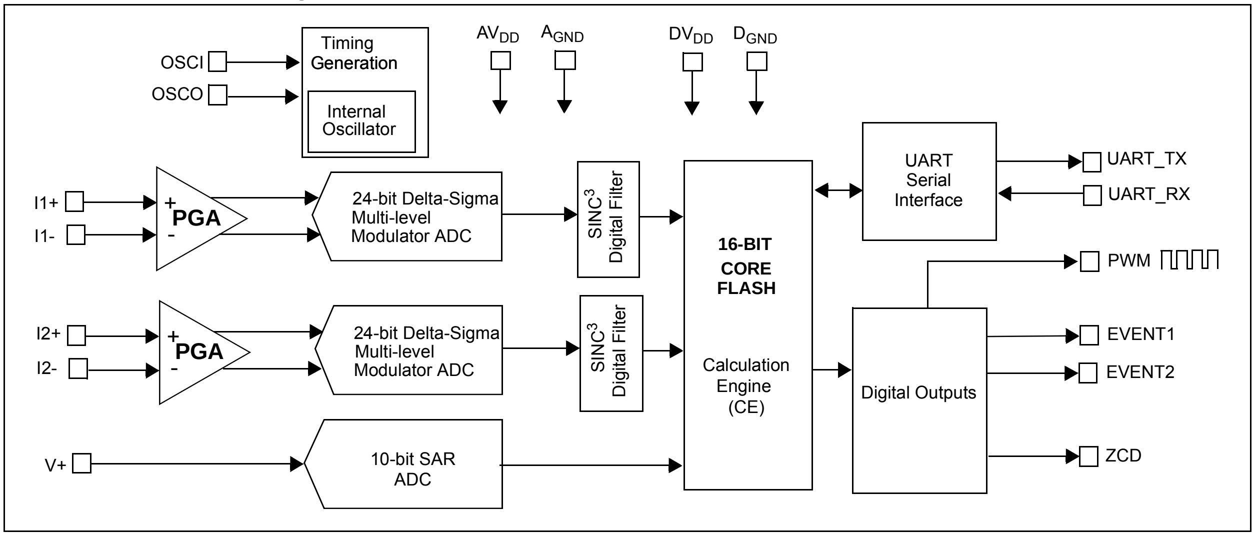
The MCP39F511N is a highly integrated, complete dual-channel single-phase power-monitoring IC designed for real-time measurement of input power for dual-socket wall outlets, power strips, and consumer and industrial applications. It includes dual-channel 24-bit Delta-Sigma ADCs for dual-current measurements, a 10-bit SAR ADC for voltage measurement, a 16-bit calculation engine, EEPROM and a flexible two-wire interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.5% accurate designs across a 4000:1 dynamic range.

Package Types

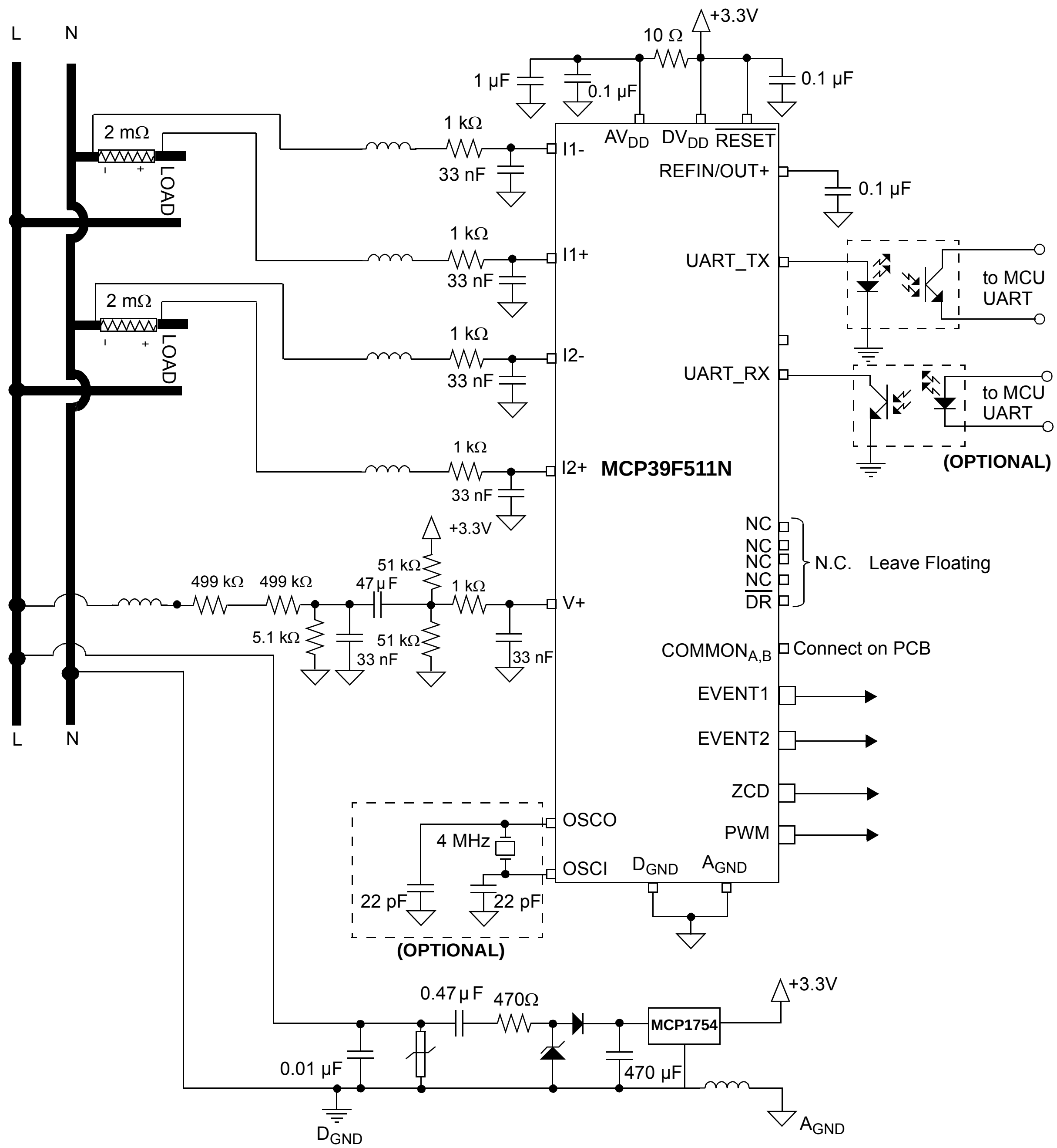


*Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



Typical Application



Note: The external sensing components shown here, the 2 mΩ shunts, two 499 kΩ and 5.1 kΩ resistor for the 200:1 voltage divider, are specifically chosen to match the default values for the calibration registers defined in **Section 6.0 "Register Descriptions"**. By choosing low-tolerance components of these values (e.g. 1% tolerance), measurement accuracy in the 2-3% range can be achieved with zero calibration. See **Section 9.0 "MCP39F511N Calibration"** for more information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} .... -0.3 to +4.5V
AV_{DD} .... -0.3 to +4.0V
Digital inputs and outputs w.r.t. A_{GND}..............-0.3V to +4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ....-2V to +2V
V_{REF} input w.r.t. A_{GND} ....-0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin.............................300 mA
Maximum Current into DV_{DD} pin................................250 mA
Maximum Output Current Sunk by Digital IO ....25 mA
Maximum Current Sourced by Digital IO......................25 mA
Storage temperature ....-65°C to +150°C
Ambient temperature with power applied......-40°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD on the analog inputs (HBM,MM)................4.0 kV, 200V
ESD on all other pins (HBM,MM).......................4.0 kV, 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Measurement						
Active Power (**Note 1**)	P	—	±0.5	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Reactive Power (**Note 1**)	Q	—	±0.5	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Apparent Power (**Note 1**)	S	—	±1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Current RMS (**Note 1**)	I_{RMS}	—	±1	—	%	4000:1 Dynamic Range on Current Channel (**Note 2**)
Voltage RMS (**Note 1**)	V_{RMS}	—	±1	—	%	4000:1 Dynamic Range on Voltage Channel (**Note 2**)
Power Factor (**Note 1**)	Φ	—	±1	—	%	
Line Frequency (**Note 1**)	LF	—	±1	—	%	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.
2: Specification by design and characterization; not production tested.
3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.
4: Applies to Voltage Sag and Voltage Surge events only.
5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.
7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	Note 3
Minimum Time for Voltage Surge/Sag Detection	t_{AC_SASU}	—	see Section 7.0	—	ms	Note 4
24-Bit Delta-Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (I2+ – I2-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	Note 5
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	Note 6
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	Note 6
Signal-to-Noise Ratio	SNR	92	95	—	dB	Note 6
Spurious Free Dynamic Range	SFDR	—	111	—	dB	Note 6
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + $0.6V_{PP}$, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
10-Bit SAR ADC Performance for Voltage Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	DV_{DD} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Nonlinearity	I_{NL}	—	±1	±2	LSb	
Differential Nonlinearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Clock and Timings						
UART Baud Rate	UDB	1.2	—	115.2	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	8	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40°C to +85°C only (**Note 7**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, V_{REFEXT} = 0
Output Impedance	$Z_{OUT}V_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.3V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across both channels at AV_{DD}, DV_{DD} = 2.7 to 3.6V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
DV_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-on Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power-on Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms
Operating Current	I_{DD}	—	15	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Calculated from reading the register values with no averaging, single computation cycle with accumulation interval of 16 line cycles, channel 1 or channel 2.

2: Specification by design and characterization; not production tested.

3: N = Value in the Accumulation Interval Parameter register. The default value of this register is 4 or T_{CAL} = 320 ms for 50 Hz line.

4: Applies to Voltage Sag and Voltage Surge events only.

5: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

6: V_{IN} = 1 V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

7: Variation applies to internal clock and UART only.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 DV_{DD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	Digital Output pins only (ZCD, PWM, EVENT1, EVENT2)

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistance						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	36.9	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz, channel 1 or channel 2.

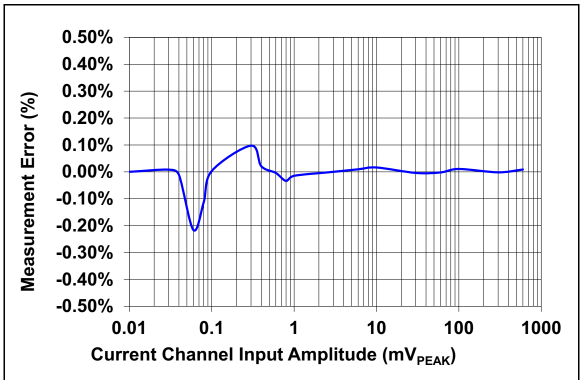


FIGURE 2-1: *Active Power, Gain = 1.*

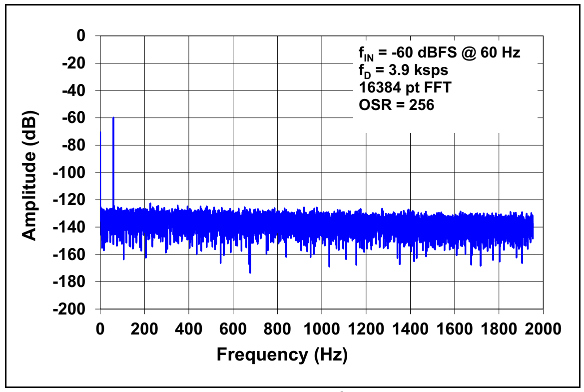


FIGURE 2-4: *Spectral Response.*

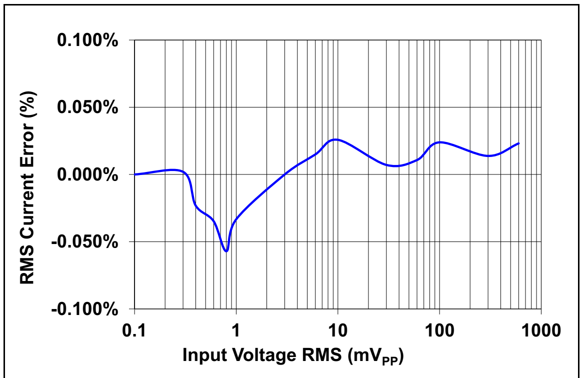


FIGURE 2-2: *RMS Current, Gain = 1.*

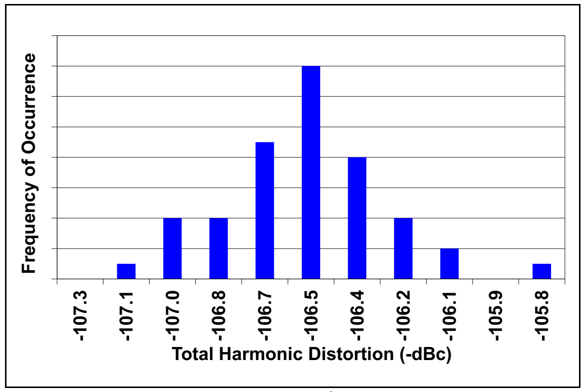


FIGURE 2-5: *THD Histogram.*

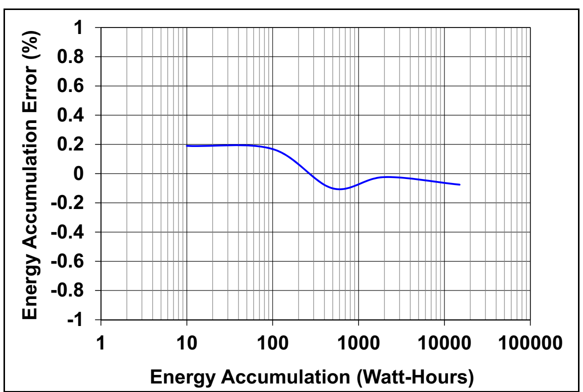


FIGURE 2-3: *Energy, Gain = 8.*

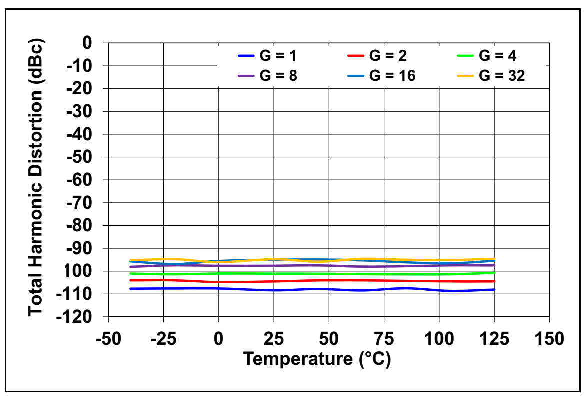


FIGURE 2-6: *THD vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz, channel 1 or channel 2.

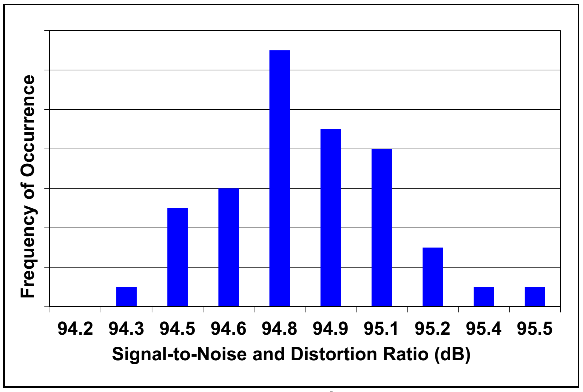


FIGURE 2-7: *SNR Histogram.*

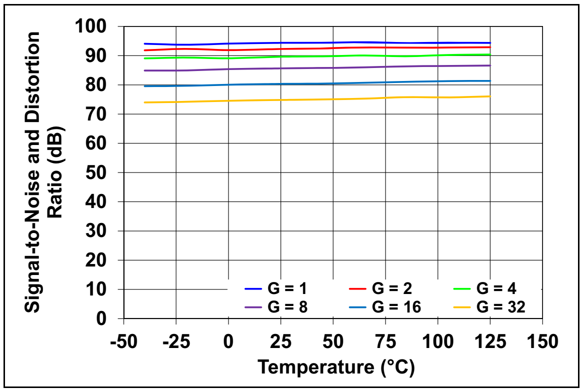


FIGURE 2-8: *SINAD vs. Temperature.*

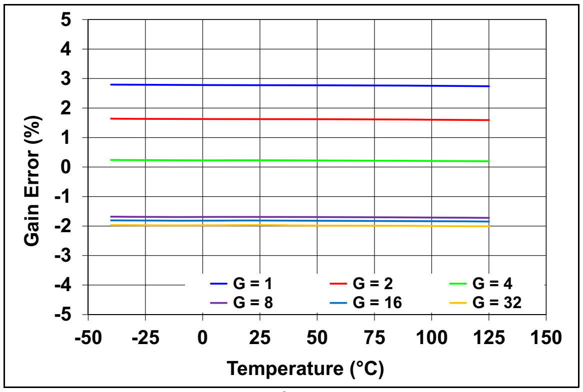


FIGURE 2-9: *Gain Error vs. Temperature.*

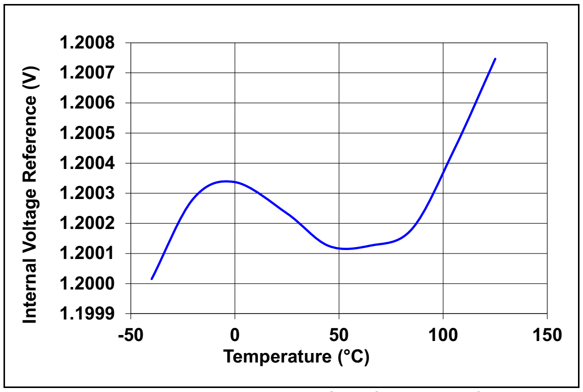


FIGURE 2-10: *Internal Voltage Reference vs. Temperature.*

3.0 PIN DESCRIPTION

The pin descriptions are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F511N 5x5 QFN	Symbol	Function
1	EVENT1	Event 1 Output pin
2, 3, 8, 9	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX pin
5	$COMMON_A$	Common pin A, to be connected to pin 13 ($COMMON_B$)
6	OSCI	Oscillator Crystal Connection pin or External Clock Input pin
7	OSCO	Oscillator Crystal Connection pin
10	$\overline{RESET}$	Reset pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply pin
12	UART_TX	UART Communication TX pin
13	$COMMON_B$	Common pin B, to be connected to pin 5 ($COMMON_A$)
14	PWM	Pulse-Width Modulation (PWM) Output pin
15	EVENT2	Event 2 Output pin
16	I1+	Non-Inverting Current Channel 1 Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel 1 Input for 24-bit ΔΣ ADC
18	I2-	Inverting Voltage Channel 2 Input for 24-bit ΔΣ ADC
19	I2+	Non-Inverting Current Channel 2 Input for 24-bit ΔΣ ADC
20	V+	Non-Inverting Voltage Channel Input for 10-bit SAR ADC
21	A_{GND}	Analog Ground pin, return path for internal analog circuitry
22	ZCD	Zero Crossing Detection Output
23	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output pin
24, 27	D_{GND}	Digital Ground pin, return path for internal digital circuitry
25	DV_{DD}	Digital Power Supply pin
26	$\overline{MCLR}$	Master Clear for device
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to pins 24 and 27 (D_{GND}))

3.1 Event Output Pins (EVENTn)

These digital output pins can be configured to act as output flags based on various internal raise conditions. Control is modified through the Event Configuration register.

3.2 UART Communication Pins (UART_RX, UART_TX)

The MCP39F511N device contains an asynchronous full-duplex UART. The UART communication is eight bits with the Start and Stop bits. See **Section 4.3 "UART Settings"** for more information.

3.3 Common Pins (COMMON A and B)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F511N. These two pins should be connected together in the application.

3.4 Oscillator Pins (OSCI/OSCO)

OSCI and OSCO provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 8 MHz crystal can be connected to these pins. If a crystal or external clock source is not detected, the device will clock from the internal 8 MHz oscillator.

3.5 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the Delta-Sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a Reset state when pulled low. This input is Schmitt-triggered.

3.6 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F511N.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.7 Pulse-Width Modulator (PWM)

This digital output is a dedicated PWM output that can be controlled through the PWM Frequency and PWM Duty-Cycle Registers. See **Section 8.0 "Pulse-Width modulation (PWM)"** for more information.

3.8 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-/I2+/I2-)

(I1-, I1+), (I2-, I2+) are the two fully-differential current-channel pair inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.9 Voltage Analog Input (V+)

This is the non-inverting input to the SAR ADC for voltage measurement input. This input is used as the voltage measurement for both channel 1 and channel 2. Care should be taken to limit the voltage input here to within 300 mV of D_{GND}. DC offset of $DV_{DD}/2$ and approximately 1 V_{RMS} AC input signal.

3.10 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.11 Zero Crossing Detection (ZCD)

This digital output pin is the output of the zero crossing detection circuit of the IC. The output here will be a logic output with edges that transition at each zero crossing of the voltage channel input. For more information see **Section 5.10 "Zero Crossing Detection (ZCD)"**.

3.12 Non-Inverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.13 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry components in the system.

3.14 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F511N. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.15 Data Ready Pin ($\overline{DR}$)

The Data Ready pin indicates if a new Delta-Sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with the line frequency to ensure an integer number of samples for each line cycle.

Note: This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.16 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

4.0 COMMUNICATION PROTOCOL

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, a command packet (or command packets) and a checksum. It is important to note that the maximum number of bytes in either a Receive or Transmit frame is 35.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

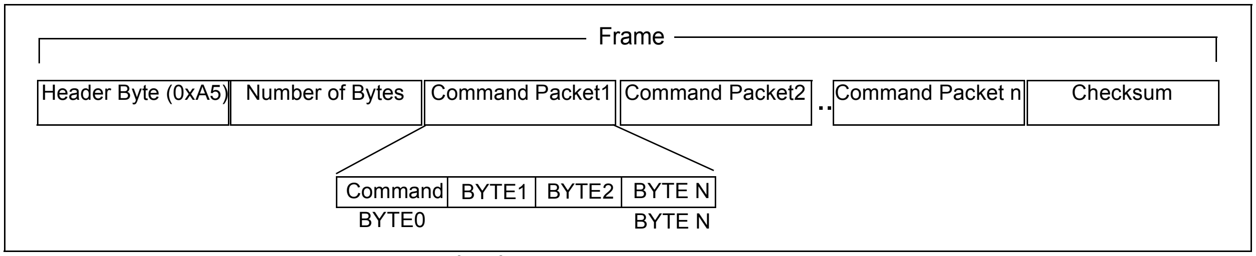


***FIGURE 4-1:** MCP39F511N Communication Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F511N with either a single command or multiple commands. No command in a frame is processed until the entire frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

4.1 Device Responses

After the reception of a communication frame, the MCP39F511N has three possible responses, which are returned with or without data, depending on the frame received. These responses are either:

- Acknowledge (ACK, 0x06): Frame received with success, commands understood and commands executed with success.
- Negative Acknowledge (NAK, 0x15): Frame received with success, however commands not executed with success, commands not understood or some other error in the command bytes.
- Checksum Fail (CSFAIL, 0x51): Frame received with success, however the checksum of the frame did not match the bytes in the frame.

Note: There is one unique device ID response which is used to determine which MCP39FXXX device is present: [NAK(0x15) + ID_BYTE].
If the device is interrogated with 0x5A, i.e. it receives 0x5A as the first byte instead of the standard 0xA5 first header byte, a special NAK is returned followed by an ID_BYTE. For the MCP39F511N the ID_BYTE is 0x03.

4.2 Checksum

The checksum is generated using simple byte addition and taking the modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and the number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F511N will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F511N, the frame and checksum are created in the same way, with the header byte becoming an Acknowledge (0x06). Communication examples are given in **Section 4.5 "Example Communication Frames and MCP39F511N Responses"**.

4.3 UART Settings

The default baud rate is 115.2 kbps and can be changed using the UART bits in the System Configuration Register. Note that the baud rate is changed only at system power-up, so when changing the baud rate, a `Save To Flash` command followed by a power-on cycle is required.

The UART operates in 8-bit mode, plus one start bit and one stop bit, for a total of 10 bits per byte, as shown in Figure 4-1.

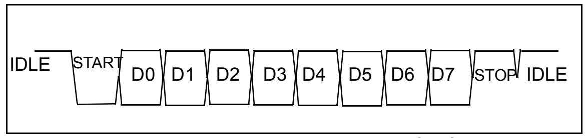


***FIGURE 4-1:** UART Transmission, N-8-1.*

4.4 Command List

The following table is a list of all accepted command bytes for the MCP39F511N. There are 10 possible accepted commands for the MCP39F511N.

TABLE 4-1: MCP39F511N INSTRUCTION SET

Command #	Command	Command ID	Instruction Parameter	Number of bytes	Successful Response UART_TX
1	`Register Read, N bytes`	0x4E	Number of bytes	2	ACK, Data, Checksum
2	`Register Write, N bytes`	0x4D	Number of bytes	1+N	ACK
3	`Set Address Pointer`	0x41	ADDRESS	3	ACK
4	`Save Registers To Flash`	0x53	None	1	ACK
5	`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, Checksum
6	`Page Write EEPROM`	0x50	PAGE	18	ACK
7	`Bulk Erase EEPROM`	0x4F	None	1	ACK
8	`Auto-Calibrate Gain`	0x5A	Channel Selection (1)	**Note 2**	
9	`Auto-Calibrate Reactive Gain`	0x7A	Channel Selection (1)	**Note 2**	
10	`Auto-Calibrate Frequency`	0x76	None	**Note 2**	

Note 1: Each bit in the instruction parameter byte refers to the corresponding channel that is being calibrated with the command. For example, if bits 0 and 1 are high, both channels 1 and 2 will be calibrated. A NAK or ACK will be returned. If a NAK is returned, refer to the Calibration Status bits in the Event Configuration Register for more information.

2: See **Section 9.0 "MCP39F511N Calibration"** for more information on calibration.

4.5 Example Communication Frames and MCP39F511N Responses

Tables 4-2 to 4-11 show exact hexadecimal communication frames as they are recommended to be sent to the MCP39F511N from the system MCU. The values here can be used as direct examples for writing the code to communicate to the MCP39F511N.

TABLE 4-2: REGISTER READ, N BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x08	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0x4E	Command (`Register Read, N Bytes`)	
7	0x20	Number of Bytes to Read (32)	
8	0x5E	Checksum	ACK + Number of Bytes (35) + 32 bytes + Checksum

Note 1: This example `Register Read, N bytes` frame, as it is written here, can be used to poll a subset of the output data, starting at the top, address 0x02, and reading 32 data bytes back or 35 bytes total in the frame.

TABLE 4-3: REGISTER WRITE, N- BYTES COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x17	Number of Bytes in Frame (23)	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0xB1	Address Low	
6	0x4D	Command (`Register Write, N Bytes`)	
7	0x0F	Number of Bytes to Write (15)	
8-22	*Data*	Data Bytes (15 total data bytes)	
23	Checksum	Checksum	ACK

Note 1: This `Register Write, N Bytes` frame, as shown here, is writing channel 1 range and calibration target values, starting at address 0xB1 (the second byte in the Channel 1 Range register) and then writing 15 bytes of data to consecutive addresses to complete the setup of channel 1 registers prior to calibration. Note these are not the calibration registers, but the calibration targets which need to be written prior to issuing the auto-calibration target commands. See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-4: SET ADDRESS POINTER COMMAND (Note 1)

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x06	Number of Bytes in Frame	
3	0x41	Command (`Set Address Pointer`)	
4	0x00	Address High	
5	0x02	Address Low	
6	0xEE	Checksum	ACK

Note 1: The `Set Address Pointer` command is typically included inside of a frame that includes a read or write command, as shown in Tables 4-2 and 4-3. There is typically no reason for this command to have its own frame, but is shown here as an example.

TABLE 4-5: SAVE TO FLASH COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x53	Command (`Save To Flash`)	
4	0xFC	Checksum	ACK

TABLE 4-6: PAGE READ EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x42	Command (`Page Read EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5	0xED	Checksum	ACK + EEPROM Page Data + Checksum

TABLE 4-7: PAGE WRITE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x15	Number of Bytes in Frame	
3	0x50	Command (`Page Write EEPROM`)	
4	0x01	Page Number (e.g. 1)	
5-20	*Data*	EEPROM Data (16 bytes/Page)	
21	Checksum	Checksum	ACK

TABLE 4-8: BULK ERASE EEPROM COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x4F	Command (`Bulk Erase EEPROM`)	
4	0xF8	Checksum	ACK

TABLE 4-9: AUTO-CALIBRATE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x5A	Command (`Auto-Calibrate Gain`)	
4	0x03	Instruction Parameter (Channel Instruction, calibrate both channels 1 and 2)	
5	0x07	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-10: AUTO-CALIBRATE REACTIVE GAIN COMMAND

Byte #	Value	Description	Response from MCP39F511N
1	0xA5	Header Byte	
2	0x05	Number of Bytes in Frame	
3	0x7A	Command (`Auto-Calibrate Reactive Gain`)	
4	0x01	Instruction Parameter (Channel Instruction, calibrate channel 1 only)	
5	0x25	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

TABLE 4-11: AUTO-CALIBRATE FREQUENCY COMMAND

Byte #	Value	Description	Response from
1	0xA5	Header Byte	
2	0x04	Number of Bytes in Frame	
3	0x76	Command (`Auto-Calibrate Frequency`)	
4	0x1F	Checksum	ACK (or NAK if unable to calibrate)(1)

Note 1: See **Section 9.0 "MCP39F511N Calibration"** for more information.

4.6 Command Descriptions

4.6.1 REGISTER READ, N BYTES (0x4E)

The `Register Read, N Bytes` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other read commands. An Acknowledge, Data and Checksum is the response for this command. The maximum number of bytes that can be read with this command is 32. If there are other read commands within a frame, the maximum number of bytes that can be read is 32 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.6.2 REGISTER WRITE, N BYTES (0x4D)

The `Register Write, N Bytes` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command and can be used in conjunction with other write commands. An Acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 32. If there are other write commands within a frame, the maximum number of bytes that can be written is 32 minus the number of bytes being written in the frame. With this command, the data is written LSB first.

4.6.3 SET ADDRESS POINTER (0x41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes: Address High Byte followed by Address Low Byte. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an Acknowledge will be returned.

4.6.4 SAVE REGISTERS TO FLASH (0x53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. The response to this command is an Acknowledge.

4.6.5 PAGE READ EEPROM (0x42)

The `Page Read EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F511N. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an Acknowledge, 16-bytes of data and CRC Checksum.

4.6.6 PAGE WRITE EEPROM (0x50)

The `Page Write EEPROM` command is expecting 17 additional bytes in the command parameters, which are the EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is an Acknowledge.

4.6.7 BULK ERASE EEPROM (0x4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. The response to this command is Acknowledge.

4.6.8 AUTO-CALIBRATE GAIN (0x5A)

The `Auto-Calibrate Gain` command initiates the single-point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and Active power based on the target values written in the corresponding registers. The instruction parameter for this command selects if you are calibrating channel 1, 2 or both. Bit 0 corresponds to channel 1 and bit 1 corresponds to channel 2. See **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration. The response to this command is Acknowledge.

4.6.9 AUTO-CALIBRATE REACTIVE POWER GAIN (0x7A)

The `Auto-Calibrate Reactive Gain` command initiates a single-point calibration to match the measured Reactive power to the target Reactive power. The instruction parameter for this command selects if you are calibrating channel 1, 2, or both. Bit 0 corresponds to channel 1 and bit 1 corresponds to channel 2. This is typically done at PF = 0.5. See section **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration.

4.6.10 AUTO-CALIBRATE FREQUENCY (0x76)

For applications not using an external crystal and running the MCP39F511N off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency register is set such that the frequency indication matches what is set in the Line Frequency Reference register. See **Section 9.0 "MCP39F511N Calibration"** for more information on device calibration.

4.7 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F511N:

TABLE 4-12: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u64	Unsigned, 64-bit register
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F511N uses a coherent sampling algorithm to phase lock the sampling rate to the line frequency on the voltage channel input with an integer number of samples per line cycle, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the power outputs.

There are two separate computation paths, using two currents from two separate channels (channel 1 and channel 2) referenced below as I_N and V. Therefore each current, power, and energy output is duplicated, one for each calculation channel.

In addition, there are duplicate calibration registers (offset, gain, phase, etc.) for each calculation channel.

5.1.1 LINE FREQUENCY

The coherent sampling algorithm is also used to calculate the Line Frequency Output register, which is updated every computation cycle. The correction factor for line frequency measurement is the Gain Line Frequency register which is used during the line frequency calibration (see section **Section 9.6.1 “Using the Auto-Calibrate Frequency Command”**. Note that the resolution of the Line Frequency Output register is fixed, and the resolution is 1 mHz.

5.2 Accumulation Interval Parameter

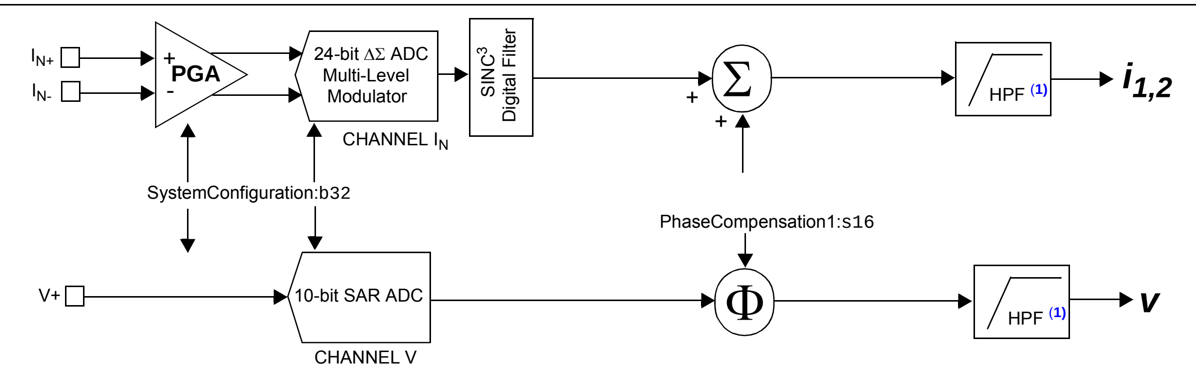
The accumulation interval is defined as a 2^N number of line cycles, where N is the value in the Accumulation Interval Parameter register. This is identical for both calculation channels.

5.3 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F511N is shown in Figure 5-1. All conditions set in this diagram affect all of the output registers (RMS current, RMS voltage, Active power, Reactive power, apparent power, etc.). The gain of the PGA, the Shutdown and Reset status of the 24-bit ADCs are all controlled through the System Configuration Register.

To compensate for any external phase error between the current and voltage channels, the Phase Compensation register can be used.

See **Section 9.0 “MCP39F511N Calibration”** for more information on device calibration.



Note 1: High-Pass Filters (HPFs) are automatically disabled in the absence of an AC signal on the voltage channel.

FIGURE 5-1: *Channels 1 or 2 (I_N and V) Input-Signal Flow.*

5.4 RMS Current, RMS Voltage and Apparent Power (S)

The MCP39F511N device provides true RMS measurements. The MCP39F511N device has two simultaneous sampling 24-bit A/D converters for the current measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1}(i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1}(v_n)^2}{2^N}}$$

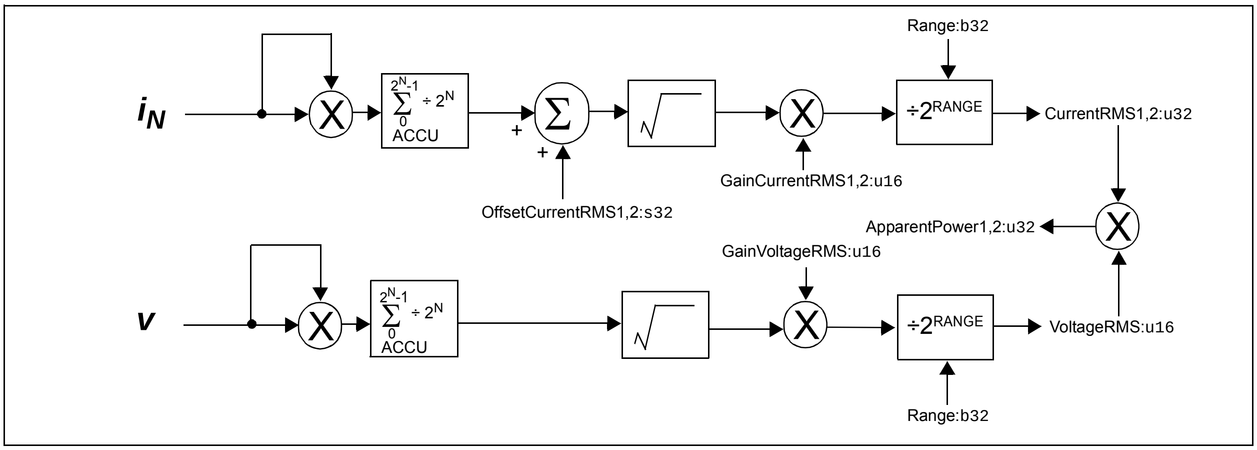


FIGURE 5-2: *RMS Current (Channel 1 or 2), Apparent Power (Channel 1 and 2) and Voltage Calculation Signal Flow.*

5.4.1 APPARENT POWER (S)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER (S)

$$S = I_{RMS} \times V_{RMS}$$

5.4.2 APPARENT POWER DIVISOR DIGITS

The registers AppPowerDivisorDigits1 and AppPowerDivisorDigits2 are configurable by the user depending on the precision of the RMS indications and the desired precision for ApparentPower1 or ApparentPower2.

Because AppPowerDivisorDigits registers can be higher than 4, it may result in a 32-bit divisor. To improve the speed of this part of the calculation engine, a method that uses only multiplications and right-bit shifts was implemented. Therefore the following equation applies:

EQUATION 5-3: APPARENT POWER (S)

$$ApparentPower = \frac{I_{RMS} \times V_{RMS}}{10^{AppPowerDivisorDigits}}$$

5.5 Power and Energy

The MCP39F511N offers signed power numbers for Active and Reactive power, import and export registers for active energy, and four-quadrant Reactive power measurement. For this device, import power or energy is considered positive (power or energy being consumed by the load), and export power or energy is considered negative (power or energy being delivered by the load). The following figure represents the measurements obtained by the MCP39F511N.

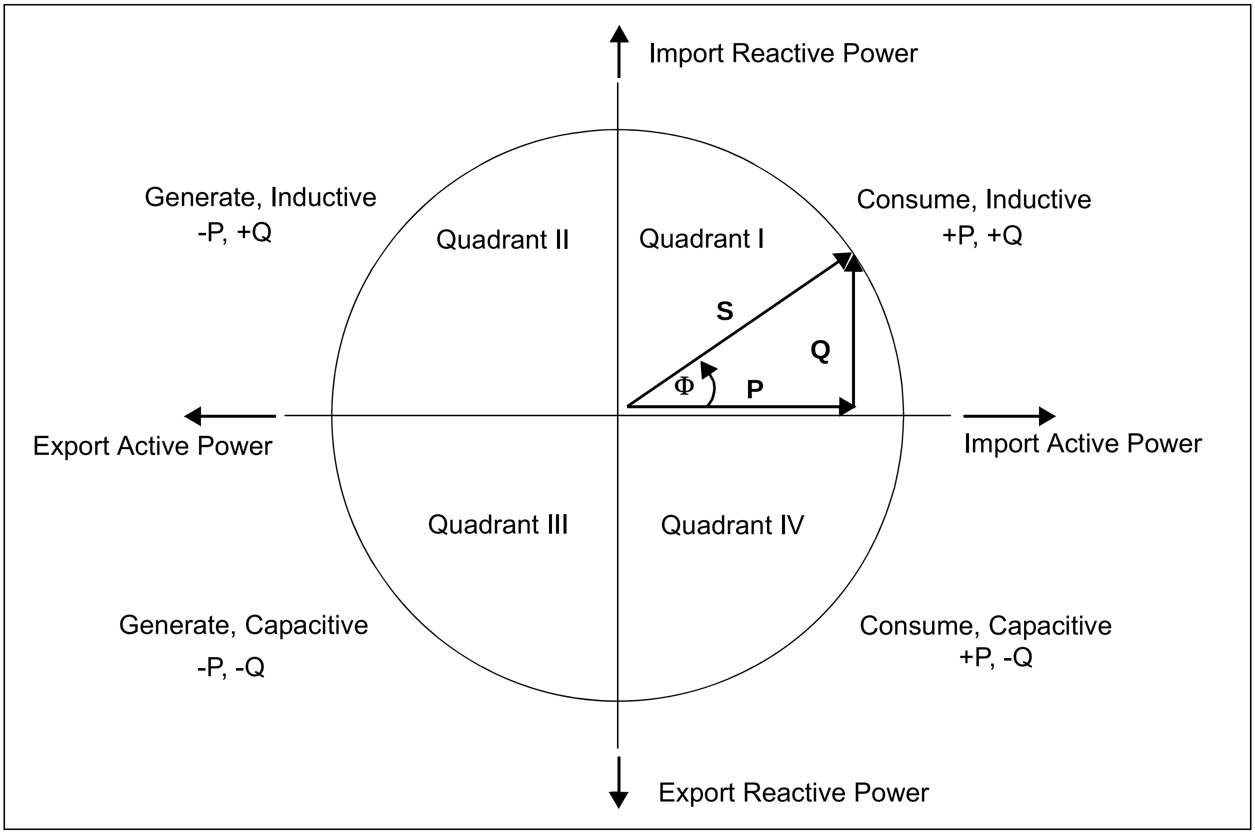


FIGURE 5-3: *The Power Circle and Triangle (S = Apparent, P = Active, Q = Reactive).*

5.6 Energy Accumulation

Energy accumulation for all four energy registers (import/export, active/reactive) occurs at the end of each computation cycle if the energy accumulation has been turned on. See **Section 6.5 "System Configuration Register"** for the energy-control bits. The accumulation of energy occurs in one of eight 64-bit energy counters, four for each channel (import and export counters for both Active and Reactive power).

5.6.1 NO-LOAD THRESHOLD

The no-load threshold is set by modifying the value in the No-Load Threshold register. The unit for this register is power with a default resolution of 0.01W. The default value is 100 or 1.00W. Any power that is below 1W will not be accumulated into any of the energy registers.

For scaling of the Apparent power indication, the calculation engine uses the Apparent Power Divisor register. This is described in the following register operations, per Equation 5-4.

EQUATION 5-4: APPARENT POWER (S)

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.7 Active Power (P)

The MCP39F511N has three simultaneous sampling A/D converters monitoring two individual currents and two individual active powers. For the Active Power calculations, the instantaneous currents and voltage are multiplied together to create instantaneous power. This instantaneous power is then converted to Active Power by averaging or calculating the DC component.

Equation 5-5 controls the number of samples used in this accumulation prior to updating the Active Power output register.

Please note that although this register is unsigned, the direction of the Active power (import or export) can be determined by the Active Power Sign bit located in the System Status Register.

EQUATION 5-5: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

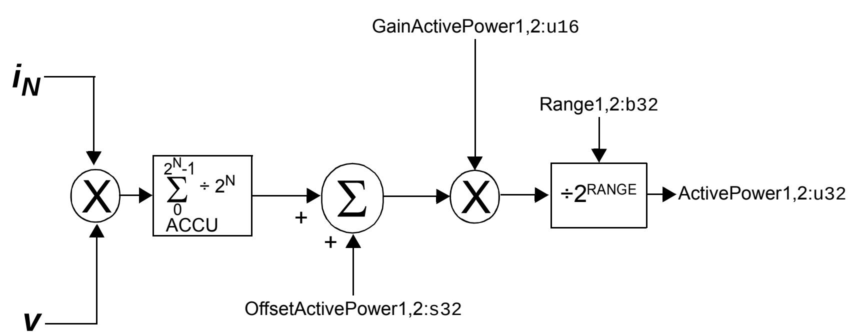


FIGURE 5-4: *Channel 1 or Channel 2 Active Power Calculation Signal Flow.*

5.8 Power Factor (PF)

Power factor is calculated by the ratio of P to S, or Active power divided by Apparent power.

EQUATION 5-6: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in two signed 16-bit registers (Power Factor), one for each channel. This register is a signed, two's complement register with the MSB representing the polarity of the power factor. Positive power factor means import power, negative power factor means export power. The sign of the Reactive power component can be used to determine if the load is inductive (positive) or capacitive (negative).

Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.9 Reactive Power (Q)

In the MCP39F511N, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with Active power where ACCU acts as the accumulator. Any light load or residual power can be removed by using the Offset Reactive Power register. Gain is corrected by the Gain Reactive Power register. The final output is an unsigned 32-bit value located in the Reactive Power register.

Please note that although this register is unsigned, the direction of the power can be determined by the Reactive Power Sign bit in the System Status Register.

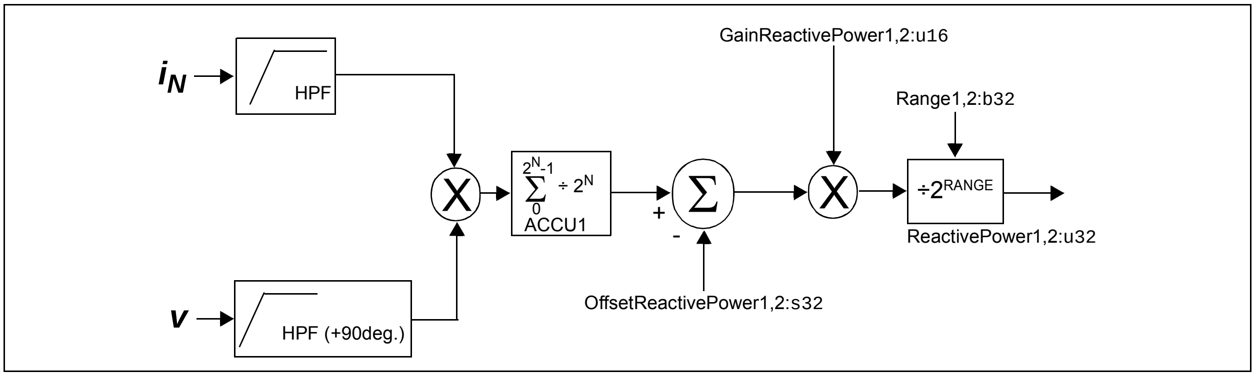


FIGURE 5-5: *Channel 1 or Channel 2 Reactive Power Calculation Signal Flow.*

5.10 Zero Crossing Detection (ZCD)

The zero crossing detection block generates a logic pulse output on the ZCD pin that is coherent with the zero crossing of the input AC signal present on voltage input pin (V+). The ZCD pin can be enabled and disabled by the corresponding bit in the System Configuration Register. When enabled, this produces a square wave with a frequency that is the same as the AC signal present on the voltage input. Figure 5-6 represents the signal on the ZCD pin superimposed with the AC signal present on the voltage input in this mode.

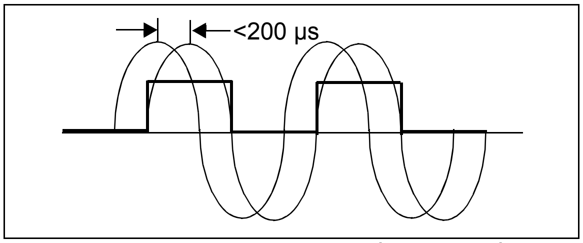


FIGURE 5-6: *Zero Crossing Detection Operation (Non-Inverted, Non-Pulse).*

A second mode is available that produces a 100 µs pulse, the frequency here is twice that of the AC signal on the voltage channel input, at each zero crossing, as shown in Figure 5-7.

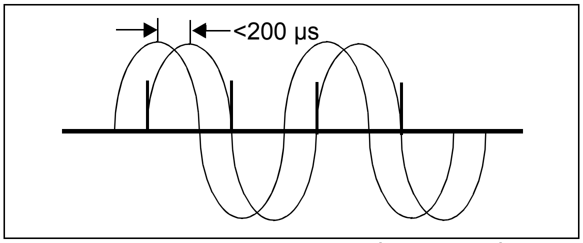


FIGURE 5-7: *Zero Crossing Detection Operation (Non-Inverted, Pulsed).*

Switching modes is done by setting the corresponding bit in the System Configuration Register.

In addition, either the toggling of this pin, or the pulse, can be inverted. The ZCD Inversion bit is also in the System Configuration register.

There are two bits in the System Configuration register that can be used to modify the zero crossing. The zero crossing output can be inverted by setting the inversion bit, or the zero crossing can be a 100 µs pulse at each zero crossing by setting the pulse bit.

Note that a low-pass filter is included in the signal path that allows the zero crossing detection circuit to filter out the fundamental frequency. An internal compensation circuit is then used to gain back the phase delay introduced by the low-pass filter resulting in a latency of less than ±200 µs.

6.0 REGISTER DESCRIPTIONS

6.1 Complete Register Map

The following table describes the registers for the MCP39F511N device.

TABLE 6-1: MCP39F511N REGISTER MAP

Address	Register Name	Section Number	Read/ Write	Data type	Description
Output Registers					
0x0000	Instruction Pointer	6.2	R	u16	Address pointer for read or write commands
0x0002	System Status	6.3	R	b16	System Status Register
0x0004	System Version	6.4	R	u16	System version date code information for MCP39F511N, set at the Microchip factory; format YMDD
0x0006	Voltage RMS	5.4	R	u16	RMS Voltage output
0x0008	Line Frequency	5.1.1	R	u16	Line Frequency output
0x000A	Power Factor1	5.8	R	s16	Power Factor output from channel 1
0x000C	Power Factor2	5.8	R	s16	Power Factor output from channel 2
0x000E	Current RMS1	5.4	R	u32	RMS Current output from channel 1
0x0012	Current RMS2	5.4	R	u32	RMS Current output from channel 2
0x0016	Active Power1	5.7	R	u32	Active Power output from channel 1
0x001A	Active Power2	5.7	R	u32	Active Power output from channel 2
0x001E	Reactive Power1	5.9	R	u32	Reactive Power output from channel 1
0x0022	Reactive Power2	5.9	R	u32	Reactive Power output from channel 2
0x0026	Apparent Power1	5.4	R	u32	Apparent Power output from channel 1
0x002A	Apparent Power2	5.4	R	u32	Apparent Power output from channel 2
0x002E	Import Energy Active Counter 1	5.6	R	u64	Accumulator for Active Energy, Import, channel 1
0x0036	Import Energy Active Counter 2	5.6	R	u64	Accumulator for Active Energy, Import, channel 2
0x003E	Export Energy Active Counter 1	5.6	R	u64	Accumulator for Active Energy, Export, channel 1
0x0046	Export Energy Active Counter 2	5.6	R	u64	Accumulator for Active Energy, Export, channel 2
0x004E	Import Energy Reactive Counter 1	5.6	R	u64	Accumulator for Reactive Energy, Import, channel 1
0x0056	Import Energy Reactive Counter 2	5.6	R	u64	Accumulator for Reactive Energy, Import, channel 2
0x005E	Export Energy Reactive Counter 1	5.6	R	u64	Accumulator for Reactive Energy, Export channel 1
0x0066	Export Energy Reactive Counter 2	5.6	R	u64	Accumulator for Reactive Energy, Export, channel 2
Calibration Registers					
0x006E	Calibration Registers Delimiter	9.7	R/W	u16	May be used to initiate loading of the default factory calibration coefficients at start-up
0x0070	Gain Current RMS1	5.4	R/W	u16	Gain Calibration Factor for RMS Current channel 1
0x0072	Gain Current RMS2	5.4	R/W	u16	Gain Calibration Factor for RMS Current channel 2
0x0074	Gain Voltage RMS	5.4	R/W	u16	Gain Calibration Factor for RMS Voltage

TABLE 6-1: MCP39F511N REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x0076	Gain Active Power1	5.7	R/W	u16	Gain Calibration Factor for Active Power, channel 1
0x0078	Gain Active Power2	5.7	R/W	u16	Gain Calibration Factor for Active Power, channel 2
0x007A	Gain Reactive Power1	5.9	R/W	u16	Gain Calibration Factor for Reactive Power, channel 1
0x007C	Gain Reactive Power2	5.9	R/W	u16	Gain Calibration Factor for Reactive Power, channel 2
0x007E	Gain Line Frequency	5.1.1	R/W	u16	Gain Calibration Factor for the Line Frequency
0x0080	Offset Current RMS1	5.4	R/W	s32	Offset Calibration Factor for RMS Current, channel 1
0x0084	Offset Current RMS2	5.4	R/W	s32	Offset Calibration Factor for RMS Current, channel 2
0x0088	Offset Active Power1	5.7	R/W	s32	Offset Calibration Factor for Active Power, channel 1
0x008C	Offset Active Power2	5.7	R/W	s32	Offset Calibration Factor for Active Power, channel 2
0x0090	Offset Reactive Power1	5.9	R/W	s32	Offset Calibration Factor for Reactive Power, channel 1
0x0094	Offset Reactive Power2	5.9	R/W	s32	Offset Calibration Factor for Reactive Power, channel 2
0x0098	Phase Compensation1	5.3	R/W	s16	Phase Compensation, channel 1
0x009A	Phase Compensation2	5.3	R/W	s16	Phase Compensation, channel 2
0x009C	Apparent Power Divisor1	5.4.2	R/W	u16	Number of Digits for apparent power divisor to match I_{RMS} and V_{RMS} resolution, channel 1
0x009E	Apparent Power Divisor2	5.4.2	R/W	u16	Number of Digits for apparent power divisor to match I_{RMS} and V_{RMS} resolution, channel 2
Design Configuration Registers					
0x00A0	System Configuration	6.5	R/W	b32	Control for device configuration, including ADC configuration
0x00A4	Event Configuration	7.5	R/W	b32	Settings for the Event pins including Relay Control
0x00A8	Accumulation Interval Parameter	5.2	R/W	u16	N for 2^N number of line cycles to be used during a single computation cycle
0x00AA	Calibration Voltage	9.3.1	R/W	u16	Target Voltage to be used during single-point calibration
0x00AC	Calibration Line Frequency	9.6.1	R/W	u16	Reference Value for the nominal line frequency
0x00AE	Range1	6.6	R/W	b32	Scaling factor for Outputs, channel 1
0x00B2	Calibration Current1	9.3.1	R/W	u32	Target Current to be used during single-point calibration, channel 1
0x00B6	Calibration Power Active1	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration, channel 1
0x00BA	Calibration Power Reactive1	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration, channel 1
0x00BE	Range2	6.6	R/W	b32	Scaling factor for Outputs, channel 2

TABLE 6-1: MCP39F511N REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x00C2	Calibration Current2	9.3.1	R/W	u32	Target Current to be used during single-point calibration, channel 2
0x00C6	Calibration Power Active2	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration Channel 2
0x00CA	Calibration Power Reactive2	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration, channel 2
0x00CE	Voltage Sag Limit	7.2	R/W	u16	RMS Voltage Sag threshold at which an event flag is recorded
0x00D0	Voltage Surge Limit	7.2	R/W	u16	RMS Voltage Surge threshold at which an event flag is recorded
0x00D2	Over Current1 Limit	7.2	R/W	u32	RMS Over Current threshold for channel 1 at which an event flag is recorded
0x00D6	Over Current2 Limit	7.2	R/W	u32	RMS Over Current threshold for channel 2 at which an event flag is recorded
0x00DA	OverPower1 Limit	7.2	R/W	u32	Over Power threshold for channel 1 at which an event flag is recorded
0x00DE	OverPower2 Limit	7.2	R/W	u32	Over Power threshold for channel 2 at which an event flag is recorded
Control Registers for Peripherals					
0x00E2	PWM Period	8.2	R/W	u16	Input register controlling PWM Frequency
0x00E4	PWM Duty Cycle	8.3	R/W	u16	Input register controlling PWM Duty Cycle
0x00E6	Reserved	—	—	u16	Reserved
0x00E8	Reserved	—	—	u16	Reserved
0x00EA	VoltagePhaseCompFreqCoef	—	—	u16	Phase Compensation Frequency Coefficient
0x00EC	RangeVoltageChPhaseComp-Freq	—	—	u16	Voltage Channel Phase Frequency Compensation Range
0x00EE	GainActivePowerCompFre-qCoef	—	—	u16	Active Power Gain Frequency Compensation Coefficient
0x00F0	RangeGainActivePowerComp-Freq	—	—	u16	Active Power Gain Frequency Compensation Range
0x00F2	GainReactivePowerCompFreq	—	—	u16	Reactive Power Gain Frequency Compensation Coefficient
0x00F4	RangeGainReactivePower-CompFreq	—	—	u16	Reactive Power Gain Frequency Compensation Range
0x00F6	GainVoltageRMSCompFre-qCoef	—	—	u16	RMS Voltage Gain Frequency Compensation Coefficient
0x00F8	RangeGainVoltageRMSComp-Freq	—	—	u16	RMS Voltage Gain Frequency Compensation Range
0x00FA	GainCurrentRMSCompFre-qCoef	—	—	u16	RMS Current Gain Frequency Compensation Coefficient
0x00FC	RangeGainCurrentRMSComp-Freq	—	—	u16	RMS Current Gain Frequency Compensation Range
0x00FE	No Load Threshold	5.6.1	R/W	u16	No Load Threshold for Energy Counting (both channels, all registers)

6.2 Address Pointer Register

This unsigned 16-bit register contains the address to which all read and write instructions occur. This register is only written through the `Set Address Pointer` command and is otherwise outside the writable range of register addresses.

6.3 System Status Register

The System Status register is a read-only register and can be used to detect the various states of pin levels as defined in Register 6-1.

REGISTER 6-1: SYSTEM STATUS REGISTER

U-0	U-0	U-0	R-x	R-n	R-n	R-x	R-n
—	—	—	AC_STATUS	EVENT2	EVENT1	OVER-POW2	OVERCURR2
bit 15							bit 8

R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n
SIGN_PR_CH2	SIGN_PA_CH2	SIGN_PR_CH1	SIGN_PA_CH1	OVERPOW1	OVER-CURR1	VSURGE	VSAG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **AC_STATUS:** AC Detection Status
1 = AC Detection failed.
0 = AC Detection successful.

bit 11 **EVENT2:** State of Event2 Detection algorithm. This bit is latched and must be cleared.
1 = Event 2 has occurred.
0 = Event 2 has not occurred.

bit 10 **EVENT1:** State of Event1 Detection algorithm. This bit is latched and must be cleared.
1 = Event 1 has occurred.
0 = Event 1 has not occurred.

bit 9 **OVERPOW2:** Over Power, channel 2. An over power event has occurred on channel 2.
1 = Over Power threshold has been broken
0 = Over Power threshold has not been broken

bit 8 **OVERCURR2:** Over Current, channel 2. An over current event has occurred on channel 2.
1 = Over current threshold has been broken
0 = Over current threshold has not been broken

bit 7 **SIGN_PR_CH2:** Sign of Reactive Power Channel 2 (inductive/capacitive state of the reactive power)
1 = Reactive Power is inductive and is in quadrants 1,2
0 = Reactive Power is capacitive and is in quadrants 3,4

bit 6 **SIGN_PA_CH2:** Sign of Active Power Channel 2 (import/export sign of active power)
1 = Active Power is positive (import) and is in quadrants 1,4
0 = Active Power is negative (export) and is in quadrants 2,3

REGISTER 6-1: SYSTEM STATUS REGISTER (CONTINUED)

bit 5 **SIGN_PR_CH1:** Sign of Reactive Power Channel 1 (inductive/capacitive state of the reactive power)
1 = Reactive Power is inductive and is in quadrants 1,2
0 = Reactive Power is capacitive and is in quadrants 3,4

bit 4 **SIGN_PA_CH1:** Sign of Active Power Channel 1 (import/export sign of active power)
1 = Active Power is positive (import) and is in quadrants 1,4
0 = Active Power is negative (export) and is in quadrants 2,3

bit 3 **OVERPOW1:** Over Power, channel 1. An over power event has occurred on channel 1.
1 = Over Power threshold has been broken
0 = Over Power threshold has not been broken

bit 2 **OVERCURR1:** Over Current, channel 1. An over current event has occurred on channel 1.
1 = Over current threshold has been broken
0 = Over current threshold has not been broken

bit 1 **VSURGE:** Voltage Surge. State of Voltage Surge Detection algorithm. This bit is latched and must be cleared
1 = Surge threshold has been broken
0 = Surge threshold has not been broken

bit 0 **VSAG:** Voltage Sag.State of Voltage Sag Detection algorithm. This bit is latched and must be cleared
1 = Sag threshold has been broken
0 = Sag threshold has not been broken

6.4 System Version Register

The System Version register is hard-coded by Microchip Technology Incorporated and contains calculation-engine date-code information. The System Version register is a date code in the YMDD format, with year and month in hex, day in decimal (e.g. 0xFB20 = 2015, Nov. 20th).

6.5 System Configuration Register

The System Configuration register contains bits for the following control:

- PGA setting
- ADC Reset State
- ADC Shutdown State
- Voltage Reference Trim
- Single Wire Auto-Transmission

These options are described in the following sections.

6.5.1 PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front-end of each 24-bit Delta-Sigma ADC. They have two functions:

- translate the common mode of the input from A_{GND} to an internal level between A_{GND} and A_{VDD}
- amplify the input differential signal

The translation of the common mode does not change the differential signal, but enters the common mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in Register 6-2: the System Configuration register. Table 6-2 represents the gain settings for the PGAs.

TABLE 6-2: PGA CONFIGURATION SETTING (Note 1)

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.6
0	0	1	2	6	±0.3
0	1	0	4	12	±0.15
0	1	1	8	18	±0.075
1	0	0	16	24	±0.0375
1	0	1	32	30	±0.01875

Note 1: This table is defined with V_{REF} = 1.2V. The two undefined settings, 110 and 111 are G = 1.

6.5.2 24-BIT ADC RESET MODE (SOFT RESET MODE)

24-bit ADC Reset mode (also called Soft Reset) can only be entered by setting high the RESET<1:0> bits in the System Status Register. This mode is defined as the condition where the converters are active but their output is forced to '0'.

6.5.3 ADC SHUTDOWN MODE

ADC Shutdown mode is defined as a state where the converters and their biases are OFF, consuming only leakage current. When the Shutdown bit is reset to '0', the analog biases will be enabled, as well as the clock and the digital circuitry.

Each converter can be placed in Shutdown mode independently. This mode is only available through programming of the SHUTDOWN<1:0> bits in the System Status Register.

6.5.4 V_{REF} TEMPERATURE COMPENSATION

The internal voltage reference comprises a proprietary circuit and algorithm to compensate first-order and second-order temperature coefficients. The compensation allows very low temperature coefficients (typically 10 ppm/°C) on the entire range of temperatures from -40°C to +125°C. This temperature coefficient varies from part to part.

The default value of this register is set to 0x42. The typical variation of the temperature coefficient of the internal voltage reference, with respect to VREFCAL register code, is shown in Figure 6-1.

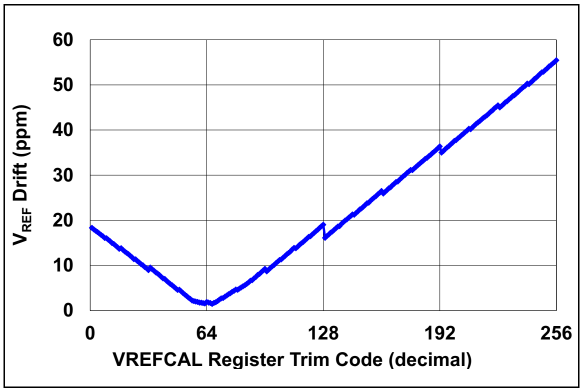


FIGURE 6-1: *V_{REF} Tempco vs. VREFCAL Trimcode Chart.*

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER

U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1
—	—	PGA_CH2<2:0>			PGA_CH1<2:0>		
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UART<2:0>			ZCD_INV	ZCD_PULS	ZCD_OUTPUT_DIS	ENERGY2	ENERGY1
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PWM	RESET<1:0>		SHUTDOWN<1:0>		VREFEXT	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented**: Read as ‘0’

bit 29-27 **PGA_CH2 <2:0>:** PGA Setting for channel 2
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8 **(Default)**
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1

bit 26-24 **PGA_CH1 <2:0>:** PGA Setting for channel 1
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8 **(Default)**
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1

bit 23-16 **Unimplemented**: Read as ‘0’

bit 15-13 **UART<2:0>:** UART Baud Rate bits
111 = 1200
110 = 2400
101 = 4800
100 = 9600
011 = 19200
010 = 38400
001 = 57600
000 = 115200 **(Default)**

bit 12 **ZCD_INV:** Zero Crossing Detection Output Inverse
1 = ZCD is inverted
0 = ZCD is not inverted **(Default)**

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER (CONTINUED)

bit 11	**ZCD_PULS:** Zero Crossing Detection Pulse mode 1 = ZCD output is 200 µs pulses on zero crossings 0 = ZCD output changes logic state on zero crossings **(Default)**
bit 10	**ZCD_OUTPUT_DIS:** Disable the Zero Crossing output pin 1 = ZCD output is disabled 0 = ZCD output is enabled (**Default**)
bit 9	**ENERGY2:** Energy counting control, channel 2 1 = Energy Counting for channel 2 is enabled 0 = Energy Counting for channel 2 is reset and disabled **(Default)**
bit 8	**ENERGY1:** Energy counting control, channel 1 1 = Energy Counting for channel 1 is enabled 0 = Energy Counting for channel 1 is reset and disabled **(Default)**
bit 7	**PWM:** PWM Control 1 = PWM Output is enabled 0 = PWM Output is disabled **(Default)**
bit 6-5	**RESET <1:0>:** Reset mode setting for current measurement ADCs 11 = Both I1 and I2 are in Reset mode 10 = I2 ADC is in Reset mode 01 = I1 ADC is in Reset mode 00 = Neither ADC is in Reset mode **(Default)**
bit 4-3	**SHUTDOWN <1:0>:** Shutdown mode setting for current measurement ADCs 11 = Both I1 and I2 are in Shutdown 10 = I2 ADC is in Shutdown 01 = I1 ADC is in Shutdown 00 = Neither ADC is in Shutdown **(Default)**
bit 2	**VREFEXT:** Internal Voltage Reference Shutdown Control 1 = Internal Voltage Reference Disabled 0 = Internal Voltage Reference Enabled **(Default)**
bit 1-0	**Unimplemented:** Read as ‘0’

6.6 Range Registers

The range registers are 32-bit registers that contain the number of right-bit shifts for the following outputs, divided into separate bytes defined below across the two registers:

- RMS Voltage
- RMS Current, Channel 1
- Power, Channel 1
- RMS Current, Channel 2
- Power, Channel 2

Note that the Power Range byte operates across both the active and reactive output registers and sets the same scale.

The purpose of this register is two-fold: the number of right-bit shifting (division by 2^{RANGE}) must be:

- high enough to prevent overflow in the output register
- low enough to allow for the desired output resolution.

It is the user's responsibility to set this register correctly to ensure proper output operation for a given meter design.

For further information and example usage, see **Section 9.3 "Single-Point Gain Calibrations at Unity Power Factor"**.

REGISTER 6-3: RANGE1 REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POWER1[7]	POWER1[6]	POWER1[5]	POWER1[4]	POWER1[3]	POWER1[2]	POWER1[1]	POWER1[0]
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CUR-RENT1[7]	CUR-RENT1[6]	CUR-RENT1[5]	CUR-RENT1[4]	CUR-RENT1[3]	CUR-RENT1[2]	CUR-RENT1[1]	CUR-RENT[0]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VOLTAGE[7]	VOLTAGE[6]	VOLTAGE[5]	VOLTAGE[4]	VOLTAGE[3]	VOLTAGE[2]	VOLTAGE[1]	VOLTAGE[0]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24	**Unimplemented:** Read as '0'
bit 23-16	**POWER1[7:0]:** Sets the number of right-bit shifts for the Active and Reactive Power output registers, channel 1.
bit 15-8	**CURRENT1[7:0]:** Sets the number of right-bit shifts for the Current RMS output register, channel 1.
bit 7-0	**VOLTAGE[7:0]:** Sets the number of right-bit shifts for the Voltage RMS output register.

REGISTER 6-4: RANGE2 REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POWER2[7]	POWER2[6]	POWER2[5]	POWER2[4]	POWER2[3]	POWER2[2]	POWER2[1]	POWER2[0]
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CUR-RENT2[7]	CUR-RENT2[6]	CUR-RENT2[5]	CUR-RENT2[4]	CUR-RENT2[3]	CUR-RENT2[2]	CUR-RENT2[1]	CUR-RENT2[0]
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24	**Unimplemented:** Read as ‘0‘
bit 23-16	**POWER2[7:0]:** Sets the number of right-bit shifts for the Active and Reactive Power output registers, channel 2
bit 15-8	**CURRENT2[7:0]:** Sets the number of right-bit shifts for the Current RMS output register, channel 2.
bit 7-0	**Unimplemented:** Read as ‘0‘

7.0 EVENT OUTPUT PINS/EVENT CONFIGURATION REGISTER

7.1 Event Pins

The MCP39F511N device has two event pins that can be configured in three possible configurations. These configurations are:

1. No event is mapped to the pin
2. Voltage Surge, Voltage Sag, Over Current or Over Power event is mapped to the pin. More than one event can be mapped to the same pin.
3. Manual control of two pins, independently. Possible only when no event is mapped to the pin.

These three configurations allow for the control of external interrupts or hardware that is dependent on the measured power, current or voltage. The Event Configuration Register below describes how these events and pins can be configured.

7.2 Limits

There are 6 limit registers associated with these events:

- Voltage Sag Limit
- Voltage Surge Limit
- Over Current Limit, channel 1
- Over Power Limit, channel 1
- Over Current Limit, channel 2
- Over Power Limit, channel 2

Each of these limits are compared to the respective output registers of voltage, current and power, and should have the same unit, e.g. 0.1V, 0.01W, etc.

7.3 Voltage Sag and Voltage Surge Detection

The event alarms for Voltage Sag and Voltage Surge work differently compared to the Over Current and Over Power events, which are tested against every computation cycle. These two event alarms are designed to provide a much faster interrupt if the condition occurs. Note that neither of these two events have a respective Hold register associated with them, since the detection time is less than one line cycle.

The calculation engine keeps track of a trailing mean square of the input voltage, as defined by Equation 7-1:

EQUATION 7-1:

$$V_{SA} = \frac{2 \times f_{LINE}}{f_{SAMPLE}} \times \left[\sum_{n = -\frac{f_{SAMPLE}}{2 \times f_{LINE}} - 1}^{0} V_n \right]^2$$

Therefore, at each data-ready occurrence, the value of V_{SA} is compared to the programmable threshold set in the Voltage Sag Limit register and Voltage Surge Limit register to determine if a flag should be set. If either of these events are masked to either the Event1 or Event2 pin, a logic-high interrupt will be given on these pins.

The Sag or Surge events can be used to quickly determine if a power failure has occurred in the system.

7.4 Calibration Status Events

The Event register contains eight bits that correspond to the pass/fail of a calibration attempt issued through the `Auto-Calibrate Gain` commands.

These commands can be used to calibrate all single-point calibration outputs for both channels:

- Line Frequency
- Voltage
- Channel 1 Current
- Channel 1 Active Power
- Channel 1 Reactive Power
- Channel 2 Current
- Channel 2 Active Power
- Channel 2 Reactive Power

Bits 31-24 are status bits with a `1` representing a calibration fail. These bits are reset to `0` when a calibration command is successful for whichever channel (or both) is being calibrated. For more information on calibration, see **Section 9.3 "Single-Point Gain Calibrations at Unity Power Factor"**.

7.5 Event Configuration Register

The Event Configuration register is used to control the event operations and the event pins and to give event and calibration status.

REGISTER 7-1: EVENT CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL_PR2	CAL_PR1	CAL_PA2	CAL_PA1	CAL_CURR2	CAL_CURR1	CAL_VOLT	CAL_LF
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVER-POW_PIN2	OVER-CUR_PIN2	VSURGE_PIN2	VSAG_PIN2	OVER-POW_PIN1	OVER-CUR_PIN1	VSURGE_PIN1	VSAG_PIN1
bit 23							bit 16

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EVENT2_MANU	EVENT1_MANU	—	—	OVER-CUR_CL	OVER-POW_CL	VSURGE_CL	VSAG_CL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VSUR_LA	VSAG_LA	OVER-POW_LA	OVER-CUR_LA	VSUR_TST	VSAG_TST	OVER-POW_TST	OVER-CUR_TST
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CAL_PR2:** Single-Point Calibration Result for Reactive Power, channel 2
1 = Calibration Failed
0 = Calibration Successful

bit 30 **CAL_PR1:** Single-Point Calibration Result for Reactive Power, channel 1
1 = Calibration Failed
0 = Calibration Successful

bit 29 **CAL_PA2:** Single-Point Calibration Result for Active Power, channel 2
1 = Calibration Failed
0 = Calibration Successful

bit 28 **CAL_PA1:** Single-Point Calibration Result for Active Power, channel 1
1 = Calibration Failed
0 = Calibration Successful

bit 27 **CAL_CURR2:** Single-Point Calibration Result for RMS Current, channel 2
1 = Calibration Failed
0 = Calibration Successful

bit 26 **CAL_CURR1:** Single-Point Calibration Result for RMS Current, channel 1
1 = Calibration Failed
0 = Calibration Successful

bit 25 **CAL_VOLT:** Single-Point Calibration Result for RMS Voltage
1 = Calibration Failed
0 = Calibration Successful

REGISTER 7-1: EVENT CONFIGURATION REGISTER (CONTINUED)

bit 24	**CAL_LF:** Single-Point Calibration Result for Line Frequency 1 = Calibration Failed 0 = Calibration Successful
bit 23	**OVERPOW_PIN2:** Event pin 2 operation for the Over Power event 1 = Event mapped to Event pin 2 only 0 = Event not mapped to a pin **(Default)**
bit 22	**OVERCUR_PIN2:** Event pin 2 operation for the Over Current event 1 = Event mapped to Event pin 2 only 0 = Event not mapped to a pin **(Default)**
bit 21	**VSURGE_PIN2:** Event pin 2 operation for the Voltage Surge event 1 = Event mapped to Event pin 2 only 0 = Event not mapped to a pin **(Default)**
bit 20	**VSAG_PIN2:** Event pin 2 operation for the Voltage Sag event 1 = Event mapped to Event pin 2 only 0 = Event not mapped to a pin **(Default)**
bit 19	**OVERPOW_PIN1:** Event pin 1 operation for the Over Power event 1 = Event mapped to Event pin 1 only 0 = Event not mapped to a pin **(Default)**
bit 18	**OVERCUR_PIN1:** Event pin 1 operation for the Over Current event 1 = Event mapped to Event pin 1 only 0 = Event not mapped to a pin **(Default)**
bit 17	**VSURGE_PIN1:** Event pin 1 operation for the Voltage Surge event 1 = Event mapped to Event pin 1 only 0 = Event not mapped to a pin **(Default)**
bit 16	**VSAG_PIN1:** Event pin 1 operation for the Voltage Sag event 1 = Event mapped to Event pin 1 only 0 = Event not mapped to a pin **(Default)**
bit 15	**EVENT2_MANU** Manual control of the Event2 pin 1 = Pin is logic high 0 = Pin is logic low **(Default)**
bit 14	**EVENT1_MANU** Manual control of the Event1 pin 1 = Pin is logic high 0 = Pin is logic low **(Default)**
bit 13-12	**Unimplemented:** Read as ‘0‘
bit 11	**OVERCUR_CL:** Reset or clear bit for the Over Current event 1 = Event is cleared 0 = Event is not cleared **(Default)**
bit 10	**OVERPOW_CL:** Reset or clear bit for the Over Power event 1 = Event is cleared 0 = Event is not cleared **(Default)**
bit 9	**VSURGE_CL:** Reset or clear bit for the Voltage Surge event 1 = Event is cleared 0 = Event is not cleared **(Default)**
bit 8	**VSAG_CL:** Reset or clear bit for the Voltage Sag event 1 = Event is cleared 0 = Event is not cleared **(Default)**
bit 7	**VSUR_LA:** Latching control of the Voltage Surge event 1 = Event is latched and needs to be cleared 0 = Event is not latched **(Default)**
bit 6	**VSAG_LA:** Latching control of the Voltage Sag event 1 = Event is latched and needs to be cleared 0 = Event is not latched **(Default)**

REGISTER 7-1: EVENT CONFIGURATION REGISTER (CONTINUED)

bit 5	**OVERPOW_LA:** Latching control of the Over Power event 1 = Event is latched and needs to be cleared 0 = Event is not latched **(Default)**
bit 4	**OVERCUR_LA:** Latching control of the Over Current event 1 = Event is latched and needs to be cleared 0 = Event is not latched **(Default)**
bit 3	**VSUR_TST:** Test control of the Voltage Surge event 1 = Simulated event is turned on 0 = Simulated event is turned off **(Default)**
bit 2	**VSAG_TST:** Test control of the Voltage Sag event 1 = Simulated event is turned on 0 = Simulated event is turned off **(Default)**
bit 1	**OVERPOW_TST:** Test control of the Over Power event 1 = Simulated event is turned on 0 = Simulated event is turned off **(Default)**
bit 0	**OVERCUR_TST:** Test control of the Over Current event 1 = Simulated event is turned on 0 = Simulated event is turned off **(Default)**

8.0 PULSE-WIDTH MODULATION (PWM)

8.1 Overview

The PWM output pin gives up to a 10-bit resolution of a pulse-width modulated signal. The PWM output is controlled by an internal timer inside the MCP39F511N, F_{TIMER} described in this section, with a base frequency of 32 MHz.

The base period is defined as P_{TIMER} and is 1/[32 MHz]. This 32 MHz time base is fixed due to the 8 MHz internal oscillator or 8 MHz external crystal.

The output of the PWM is active only when the PWM Control register has a value of 0x0001. The PWM output is turned off when the register has a value of 0x0000.

The PWM output (see Figure 8-1) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

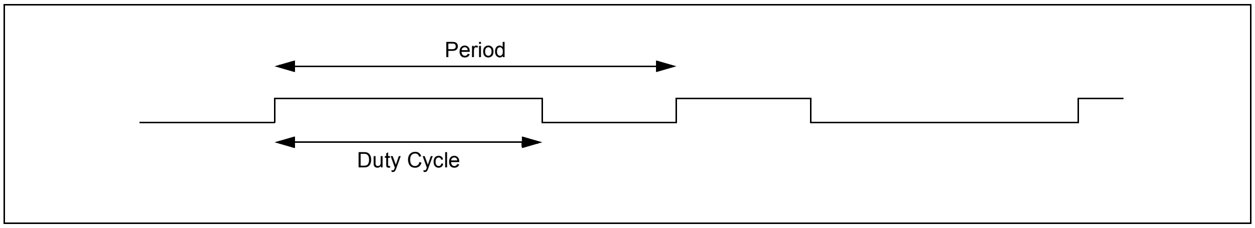


FIGURE 8-1: *PWM Output.*

There are two registers that control the PWM output, PWM Period and PWM Duty Cycle.

The 8-bit PWM Period is controlled by a 16-bit register that contains the period bits and also the prescaler bits. The PWM period bits are the most significant eight bits in the register, and the prescaler value is represented by the two least significant bits. These two values together create the PWM Period (see Figure 8-2).

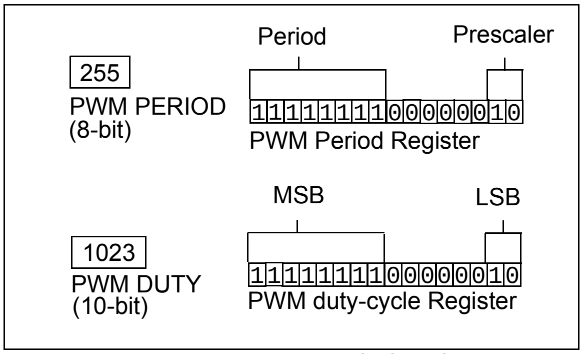


FIGURE 8-2: *PWM Period and Duty-Cycle Registers.*

The 10-bit PWM Duty Cycle is controlled by a 16-bit register where the eight most significant bits are the 8 MSB and the 2 LSB, corresponding to the 2 LSBs of the 10-bit value.

An example of the register's values are shown in Figure 8-2 with 255 for PWM Frequency (8-bit value) and 1023 for the Duty cycle (10-bit value), with the prescaler set to divide by 16 (1:0).

8.2 PWM Period

The PWM period is specified by writing the PWM Period bits of the PWM Period register. The PWM period can be calculated using the following formula:

Equation 8-1:

$$PWM\ Period = [(PWM\_Frequency) + 1] \times 2 \times P_{TIMER} \times (Prescale\ Value)$$

The PWM Period is defined as 1/[PWM frequency]. When P_{TIMER} is equal to PWM Period, the following two events occur on the next increment cycle:

- the PWM timer is cleared
- the PWM pin is set. Exception: If the PWM Duty Cycle equals 0%, the PWM pin will not be set.

8.3 PWM Duty Cycle

The PWM duty cycle is specified by writing to the PWM Duty-Cycle register. Up to 10-bit resolution is available. The PWM Duty-Cycle register contains the eight MSbs and the two LSbs. The following equations are used to calculate the PWM duty cycle as a percentage or as time:

EQUATION 8-1:

$$PWM\ Duty\ Cycle\ (\%) = (PWM\_DUTY\ CYCLE>)/(4 \times PWM\_FREQUENCY)$$

$$PWM\ Duty\ Cycle\ (time\ in\ s) = (PWM\_DUTY\_CYCLE) \times PWM\_TIMER\_PERIOD/2 \times (Prescale\ Value)$$

The PWM Duty-Cycle register can be written to at any time, but the duty-cycle value is not latched until after a period is complete.

The PWM registers and a two-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitch-less PWM operation.

The maximum PWM resolution (bits) for a given PWM frequency is shown in Equation 8-2.

EQUATION 8-2: MAXIMUM PWM RESOLUTION BASED ON A FUNCTION OF PWM FREQUENCY

$$PWM\ Resolution\ (max) = \frac{\log\left(\frac{2 \cdot F_{TIMER}}{F_{PWM}}\right)}{\log(2)}\ bits$$

Note: If the PWM duty-cycle value is longer than the PWM period, the PWM pin will not be cleared.

TABLE 8-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS WITH PWM_TIMER_FREQ = 32 MHz (DEFAULT)

PWM Frequency	1.95 kHz	31.25 kHz	62.5 kHz	125 kHz	2.67 MHz	4 MHz
Timer Prescaler	16	1	1	1	1	1
PWM Frequency Value	FFh	FFh	7Fh	3Fh	02h	01h
Maximum Resolution (bits)	10	10	9	4	3	2

REGISTER 8-1: PWM PERIOD REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PWM_P<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PRE<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **PWM_P<7:0>:** 8-bit PWM period value

bit 7-2 **Unimplemented:** Read as ‘0‘

bit 1-0 **PRE<1:0>:** PWM Prescaler
11 = Unused
10 = 1:16
01 = 1:4
00 = 1:1 **(Default)**

REGISTER 8-2: PWM DUTY-CYCLE REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DUTY<9:2>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	DUTY<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **DUTY<9:2>:** Upper 8 bits of 10-bit duty-cycle value

bit 7-2 **Unimplemented:** Read as ‘0‘

bit 1-0 **DUTY<1:0>:** Lower 2 bits of 10-bit duty-cycle value

NOTES:

9.0 MCP39F511N CALIBRATION

9.1 Overview

Calibration compensates for ADC gain error, component tolerances and overall noise in the system. The device provides an on-chip calibration algorithm that allows simple system calibration to be performed quickly. The excellent analog performance of the A/D converters on the MCP39F511N allows for a single-point calibration and a single calibration command to achieve accurate measurements.

Calibration can be done by either using the predefined auto-calibration commands, or by writing directly to the calibration registers. If additional calibration points are required (AC offset, Phase Compensation, DC offset), the corresponding calibration registers are available to the user and will be described separately in this section.

9.2 Calibration Order

The proper steps for calibration need to be maintained.

If the device runs on the internal oscillator, the line frequency should be calibrated first using the `Auto-Calibrate Frequency` command.

The single-point Gain Calibration at Unity Power Factor should be performed next. This can be done for an individual channel or for both channels at the same time, depending on the user's calibration setup.

If non-unity displacement power factor measurements are a concern, then the next step should be Phase calibration followed by Reactive power gain calibration.

Here is a summary on the order of calibration steps:

1. Line Frequency Calibration
2. Gain Calibration at PF = 1 for a single channel or both
3. Phase Calibration at PF ≠ 1 for a single channel or both (optional)
4. Reactive Gain Calibration at PF ≠ 1 for a single channel or both (optional)

If calibrating a single channel at a time, repeat steps 2-4 for the second channel.

9.3 Single-Point Gain Calibrations at Unity Power Factor

When using the device in AC mode with the high-pass filters turned on, most offset errors are removed and only a single-point gain calibration is required.

Setting the gain registers to properly produce the desired outputs can be done manually by writing to the appropriate register. The alternative method is to use the auto-calibration commands described in this section.

9.3.1 USING THE AUTO-CALIBRATION GAIN COMMAND

By applying stable reference voltages and currents that are equivalent to the values that reside in the target Calibration Current, Calibration Voltage and Calibration Active Power registers, the `Auto-Calibration Gain` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following registers are set when the `Auto-Calibration Gain` command is issued:

- Gain Current RMS Channel 1
- Gain Current RMS Channel 2
- Gain Voltage RMS
- Gain Active Power Channel 1
- Gain Active Power Channel 2

The channels can be calibrated individually or simultaneously depending on the instruction parameter byte following the command byte.

When this command is issued, the MCP39F511N attempts to match the expected values to the measured values for all three output quantities by changing the gain register based on the following formula:

EQUATION 9-1:

$$GAIN_{NEW} = GAIN_{OLD} \bullet \frac{Expected}{Measured}$$

The same formula applies for Voltage RMS, Current RMS and Active power. Since the gain registers for all three quantities are 16-bit numbers, the ratio of the expected value to the measured value (which can be modified by changing the Range register) and the previous gain must be such that the equation yields a valid number. Here the limits are set to be from 25,000 to 65,535. A new gain within this range for all three limits will return an ACK for a successful calibration, otherwise the command returns a NAK for a failed calibration attempt.

It is the user's responsibility to ensure that the proper range settings, PGA settings and hardware design settings are correct to allow for successful calibration using this command.

9.3.2 EXAMPLE OF RANGE SELECTION FOR VALID CALIBRATION

In this example, the user applies a calibration current of 1A to an uncalibrated system. The indicated value in the Current RMS register is 2300 with the system's specific shunt value, PGA gain, etc. The user expects to see a value of 1000 in the Current RMS register when 1A current is applied, meaning 1.000A with 1 mA resolution. Other given values are:

- the existing value for Gain Current RMS is 33480
- the existing value for Range is 12

By using Equation 9-1, the calculation for $Gain_{NEW}$ yields:

EQUATION 9-2:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{2300} = 14556$$

$$14556 < 25,000$$

When using the `Auto-Calibration Gain` command, the result is a failed calibration or a NAK returned form the MCP39F511N, because the resulting $Gain_{NEW}$ is less than 25,000.

The solution is to use the Range register to bring the measured value closer to the expected value, such that a new gain value can be calculated within the limits specified above.

The Range register specifies the number of right-bit shifts (equivalent to divisions by 2) after the multiplication with the Gain Current RMS register. Refer to **Section 5.0 “Calculation Engine (CE) Description”** for information on the Range register.

Incrementing the Range register by 1 unit, performing an additional right-bit shift or dividing in half is included in the calculation. Increasing the current range from 12 to 13 yields the new measured Current RMS register value of 2300/2 = 1150. The expected (1000) and measured (1150) values are much closer now, so the expected new gain should be within the limits:

EQUATION 9-3:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{1150} = 29113$$

$$25,000 < 29113 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates Current RMS and returns an ACK.

Notice that the range can be set to 14 and the resulting new gain will still be within limits ($Gain_{NEW}$ = 58226). However, since this gain value is close to the limit of the 16-bit Gain register, variations from system to system (component tolerances, etc.) might create a scenario where the calibration is not successful on some units and there would be a yield issue. The best approach is to choose a range value that places the new gain in the middle of the bounds of the gain registers described above.

In a second example, when applying 1A, the user expects an output of 1.0000A with 0.1 mA resolution. The example is starting with the same initial values:

EQUATION 9-4:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{2300} = 145565$$

$$145565 > 65535$$

The $Gain_{NEW}$ is much larger than the 16-bit limit of 65535, so fewer right-bit shifts must be introduced to get the measured value closer to the expected value. The user needs to compute the number of bit shifts that will give a value lower than 65535. To estimate this number:

EQUATION 9-5:

$$\frac{145565}{65535} = 2.2$$

2.2 rounds to the closest integer value of 2. The range value changes to 12 – 2 = 10; there are two less right-bit shifts.

The new measured value will be 2300 x 2^2 = 9200.

EQUATION 9-6:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{9200} = 36391$$

$$25,000 < 36391 < 65535$$

The resulting new gain is within the limits, and the device successfully calibrates Current RMS and returns an ACK.

9.4 Calibrating the Phase Compensation Register

Phase compensation is provided to adjust for any phase delay between the current and voltage paths. Channel 1 and channel 2 both have independent phase compensation registers. This procedure requires sinusoidal current and voltage waveforms with a significant phase shift between them, and significant amplitudes. The recommended displacement power factor for calibration is 0.5. The procedure for calculating the phase compensation register is as follows:

1. Determine what the difference is between the angle corresponding to the measured power factor (PF_{MEAS}) and the angle corresponding to the expected power factor (PF_{EXP}), in degrees.

EQUATION 9-7:

$$PF_{MEAS} = \frac{Value\ in\ PowerFactor\ Register}{32768}$$

$$ANGLE_{MEAS}(°) = acos(PF_{MEAS}) \times \frac{180}{\Pi}$$

$$ANGLE_{EXP}(°) = acos(PF_{EXP}) \times \frac{180}{\Pi}$$

2. Convert this from degrees to the resolution provided in Equation 9-8:

EQUATION 9-8:

$$\Phi = (ANGLE_{MEAS} - ANGLE_{EXP}) \times 40$$

3. Combine this additional phase compensation to whatever value is currently in the phase compensation and update the register. It is recommended that Equation 9-9 be computed in terms of an 8-bit two's complement-signed value. The 8-bit result is placed in the least significant byte of the 16-bit Phase Compensation register.

EQUATION 9-9:

$$PhaseCompensation_{NEW} = PhaseCompensation_{OLD} + \Phi$$

Based on Equation 9-9, the maximum angle in degrees that can be compensated is ±3.2 degrees. If a larger phase shift is required, contact your local Microchip sales office.

9.5 Offset/No-Load Calibrations

During offset calibrations, it is recommended that no line voltage or current be applied to the system. The system should be in a no-load condition.

9.5.1 AC OFFSET CALIBRATION

There are three registers associated with the AC Offset Calibration:

- Offset Current RMS Channel 1
- Offset Current RMS Channel 2
- Offset Active Power Channel 1
- Offset Active Power Channel 2
- Offset Reactive Power Channel 1
- Offset Reactive Power Channel 2

When computing the AC offset values, the respective gain and range registers should be taken into consideration according to the block diagrams in Figures 5-2 and 5-4.

After a successful offset calibration, a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

9.5.2 DC OFFSET CALIBRATION

In DC applications, the high-pass filter on the current and voltage channels is turned off. To remove any residual DC value on the current, the DCOffsetCurrent Channel 1 and Channel 2 registers add to the A/D conversion immediately after the ADC and prior to any other function.

9.6 Calibrating the Line Frequency Register

The Line Frequency register contains a 16-bit number with a value equivalent to the input-line frequency as it is measured on the voltage channel. When in DC mode, this calculation is turned off and the register will be equal to zero.

The measurement of the line frequency is only valid from 45 to 65 Hz.

9.6.1 USING THE AUTO-CALIBRATE FREQUENCY COMMAND

By applying a stable reference voltage with a constant line frequency that is equivalent to the value that resides in the LineFrequencyRef register, the `Auto-Calibrate Frequency` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following register is set when the `Auto-Calibrate Frequency` command is issued:

- Gain Line Frequency

The formula used to calculate the new gain is shown in Equation 9-1.

9.7 Retrieving Factory-Default Calibration Values

After user calibration and a `Save to Flash` command has been issued, it is possible to retrieve the factory-default calibration values. This can be done by writing 0xA5A5 to the Calibration Delimiter register, issuing a `Save to Flash`, and then resetting the part. This procedure will retrieve all factory default-calibration values and will remain in this state until calibration has been performed again, and a `Save to Flash` command has been issued.

10.0 EEPROM

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable across the entire V_{DD} range. The MCP39F511N has 256 16-bit words of EEPROM that is organized in 32 pages for a total of 512 bytes.

There are three commands that support access to the EEPROM array.

- `EEPROM Page Read` (0x42)
- `EEPROM Page Write` (0x50)
- `EEPROM Bulk Erase` (0x4F)

TABLE 10-1: EXAMPLE EEPROM COMMANDS AND DEVICE RESPONSE

Command	Command ID BYTE 0	BYTE 1-N	# Bytes	Successful Response
`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, Checksum
`Page Write EEPROM`	0x50	PAGE + 16 BYTES OF DATA	18	ACK
`Bulk Erase EEPROM`	0x4F	None	1	ACK

TABLE 10-2: MCP39F511N EEPROM ORGANIZATION

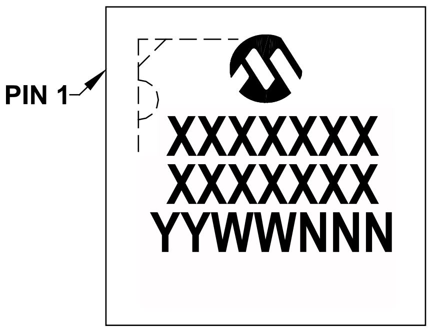
Page		00	02	04	06	08	0A	0C	0E
0	0000	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
1	0010	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
2	0020	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
3	0030	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
4	0040	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
5	0050	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
6	0060	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
7	0070	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
8	0080	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
9	0090	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
10	00A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
11	00B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
12	00C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
13	00D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
14	00E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
15	00F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
16	0100	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
17	0110	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
18	0120	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
19	0130	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
20	0140	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
21	0150	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
22	0160	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
23	0170	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
24	0180	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
25	0190	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
26	01A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
27	01B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
28	01C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
29	01D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
30	01E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
31	01F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF

NOTES:

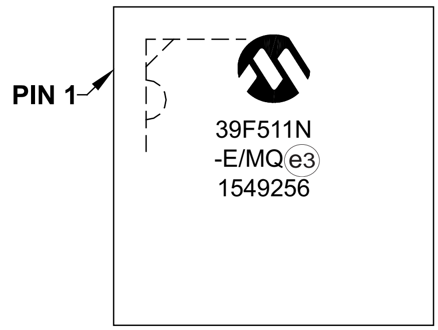
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

28-Lead QFN (5x5x0.9 mm)



Example

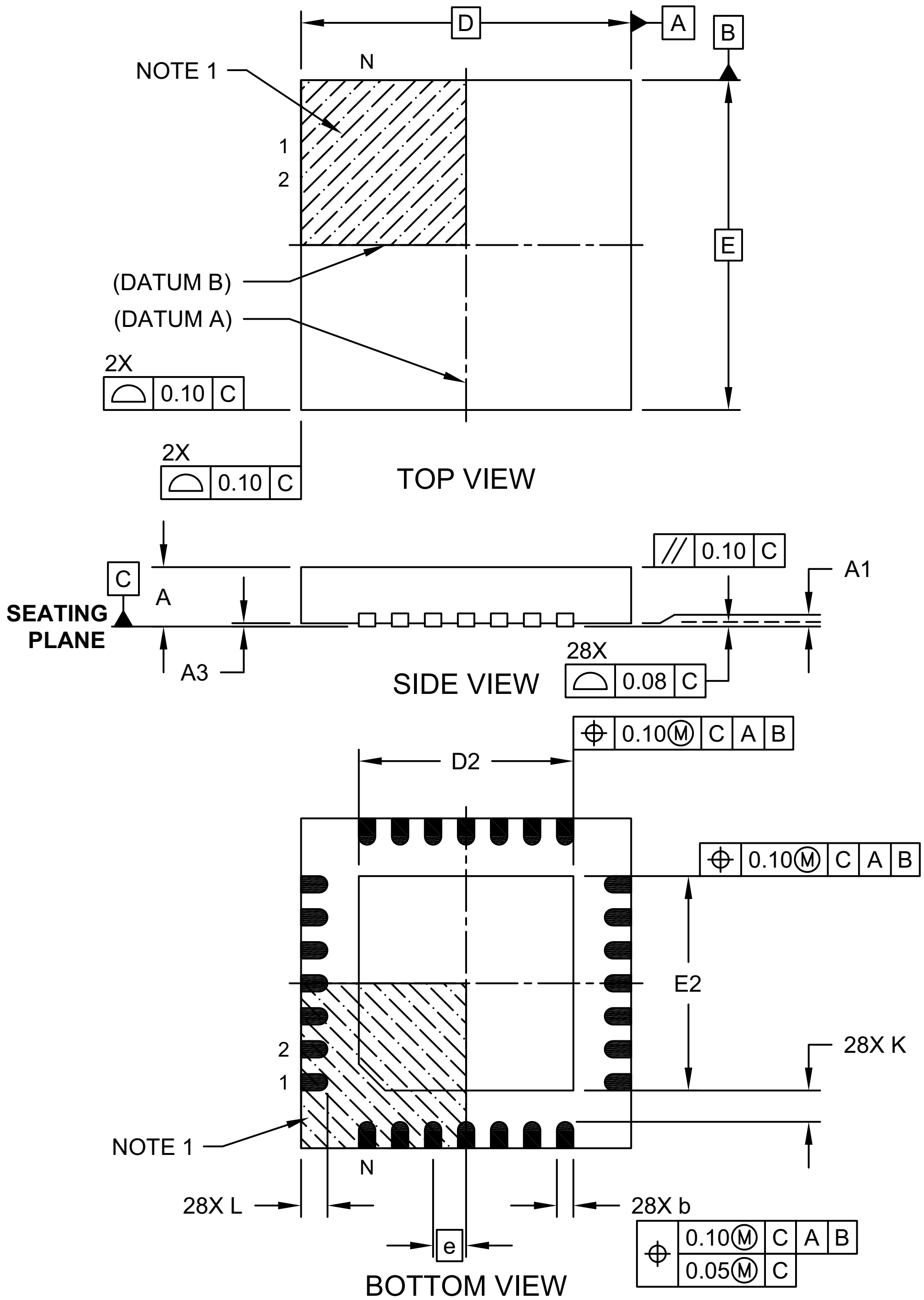


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

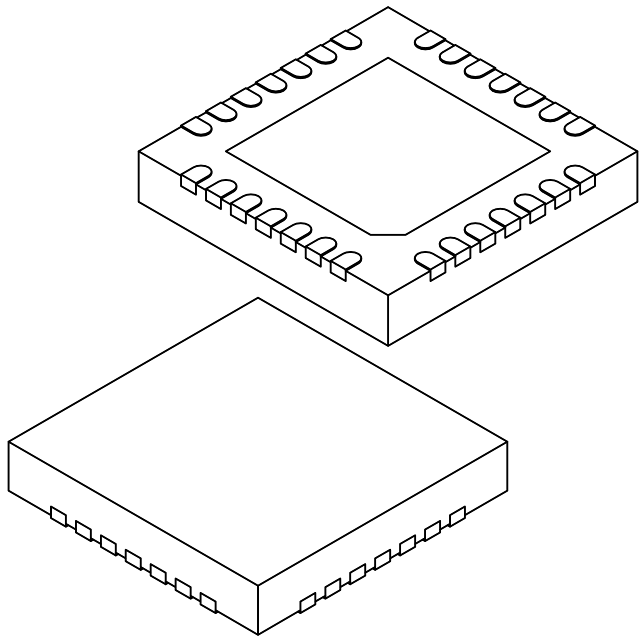
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

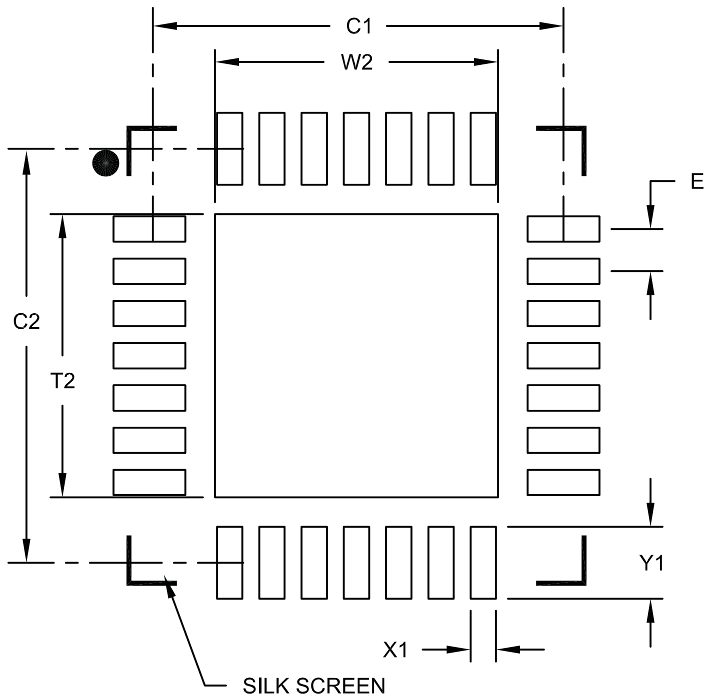
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-140C Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5 mm Body [QFN] Land Pattern With 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2140A

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP39F511N: Dual-Channel Single-Phase Power-Monitoring IC with Calculation		
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel [(1)]
Temperature Range:	E	=	-40°C to +125°C
Package:	MQ	=	Plastic Quad Flat, No Lead Package 5x5x0.9 mm body (QFN), 28-lead

Examples:

a) MCP39F511N-E/MQ: Extended temperature, 28LD 5x5 QFN package

b) MCP39F511NT-E/MQ: Tape and Reel, Extended temperature, 28LD 5x5 QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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ISO/TS 16949

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