MCP14A0301/2

3.0A MOSFET Driver with Low Threshold Input and Enable

Features

- High Peak Output Current: 3.0A (typical)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - 1800 pF in 13 ns (typical)
- Short Delay Times: 15 ns (t_{D1}), 18 ns (t_{D2}) (typical)
- Low Supply Current: 360 µA (typical)
- Low-Voltage Threshold Input and Enable with Hysteresis
- Latch-Up Protected: Withstands 500 mA Reverse Current
- Space-Saving Packages:
  - 8-Lead MSOP
  - 8-Lead SOIC
  - 8-Lead 2 x 2 WDFN

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Level Translator
- Motor and Solenoid Drive

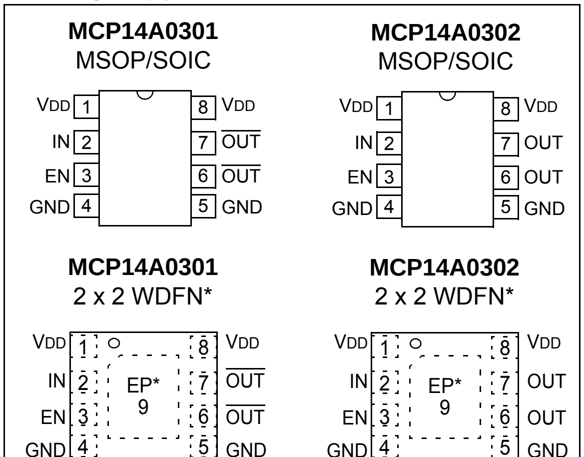
General Description

The MCP14A0301/2 devices are high-speed MOSFET drivers that are capable of providing up to 3.0A of peak current while operating from a single 4.5V to 18V supply. There are two output configurations available; inverting (MCP14A0301) and noninverting (MCP14A0302). These devices feature low shoot-through current, fast rise and fall times, and short propagation delays, which make them ideal for high switching frequency applications.

The MCP14A0301/2 family of devices offers enhanced control with Enable functionality. The active-high Enable pin can be driven low to drive the output of the MCP14A0301/2 low, regardless of the status of the Input pin. An integrated pull-up resistor allows the user to leave the Enable pin floating for standard operation.

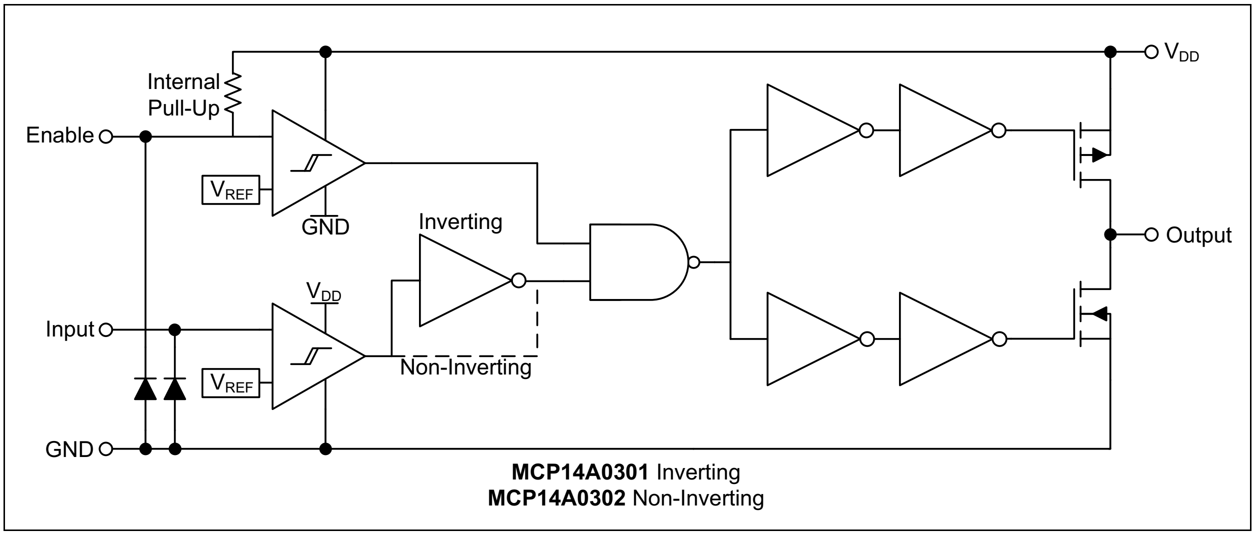
These devices are highly latch-up resistant under any condition within their power and voltage ratings. They can accept up to 500 mA of reverse current being forced back into their outputs without damage or logic upset. All terminals are fully protected against electrostatic discharge (ESD) up to 2 kV (HBM) and 200V (MM).

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings †

V_{DD}, Supply Voltage .... +20V

V_{IN}, Input Voltage .... (V_{DD} + 0.3V) to (GND – 0.3V)

V_{EN}, Enable Voltage .... (V_{DD} + 0.3V) to (GND – 0.3V)

Package Power Dissipation (T_A = +50°C)

- 8L MSOP 0.58W
- 8L SOIC 0.90W
- 8L 2 X 2 WDFN 1.63W

ESD protection on all pins .... 2 kV (HBM)

ESD protection on all pins .... 200V (MM)

† **Notice:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input						
Input Voltage Range	V_{IN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.3	—	V	
Input Current	I_{IN}	-1	—	+1	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.3	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.3	—	V	
Enable Pin Pull-Up Resistance	R_{ENBL}	—	1.5	—	MΩ	V_{DD} = 18V, ENB = A_{GND}
Enable Input Current	I_{EN}	—	12	—	µA	V_{DD} = 18V, ENB = A_{GND}
Propagation Delay	t_{D3}	—	15	22	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3, (**Note 1**)
Propagation Delay	t_{D4}	—	18	25	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3, (**Note 1**)
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	I_{OUT} = 0A
Low Output Voltage	V_{OL}	—	—	0.025	V	I_{OUT} = 0A
Output Resistance, High	R_{OH}	—	2.2	3.3	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	1.5	2.3	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	3.0	—	A	V_{DD} = 18V (**Note 1**)
Latch-Up Protection Withstand Reverse Current	I_{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 µs (**Note 1**)
Switching Time (Note 1)						
Rise Time	t_R	—	13	18	ns	V_{DD} = 18V, C_L = 1800 pF, see Figure 4-1, Figure 4-2
Fall Time	t_F	—	12	17	ns	V_{DD} = 18V, C_L = 1800 pF, see Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	15	22	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1, Figure 4-2
	t_{D2}	—	18	25	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1, Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	360	580	µA	V_{IN} = 3V, V_{EN} = 3V
	I_{DD}	—	360	580	µA	V_{IN} = 0V, V_{EN} = 3V
	I_{DD}	—	360	580	µA	V_{IN} = 3V, V_{EN} = 0V
	I_{DD}	—	360	580	µA	V_{IN} = 0V, V_{EN} = 0V

Note 1: Tested during characterization, not production tested.

TABLE 1-2: DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.						
Input						
Input Voltage Range	V_{IN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.3	—	V	
Input Current	I_{IN}	–10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND – 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.3	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.3	—	V	
Enable Input Current	I_{EN}	—	12	—	µA	V_{DD} = 18V, ENB = A_{GND}
Propagation Delay	t_{D3}	—	20	27	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3
Propagation Delay	t_{D4}	—	24	31	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	4.1	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	—	3.3	Ω	I_{OUT} = 10 mA, V_{DD} = 18V

Note 1: Tested during characterization, not production tested.

TABLE 1-2: DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE) (CONTINUED)

Electrical Specifications: Unless otherwise indicated, over the operating range with $4.5V \le V_{DD} \le 18V$.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Switching Time (Note 1)						
Rise Time	t_R	—	15	20	ns	V_{DD} = 18V, C_L = 1800 pF, T_A = +125°C, see Figure 4-1, Figure 4-2
Fall Time	t_F	—	13	18	ns	V_{DD} = 18V, C_L = 1800 pF, T_A = +125°C, see Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	20	27	ns	V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1, Figure 4-2
	t_{D2}	—	24	31		V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1, Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	—	800	uA	V_{IN} = 3V, V_{EN} = 3V
	I_{DD}	—	—	800	uA	V_{IN} = 0V, V_{EN} = 3V
	I_{DD}	—	—	800	uA	V_{IN} = 3V, V_{EN} = 0V
	I_{DD}	—	—	800	uA	V_{IN} = 0V, V_{EN} = 0V

Note 1: Tested during characterization, not production tested.

1.2 Temperature Characteristics

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \le V_{DD} \le 18V$						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Junction-to-Ambient Thermal Resistance, 8LD MSOP	θ_{JA}	—	172	—	°C/W	Note 1
Junction-to-Ambient Thermal Resistance, 8LD SOIC	θ_{JA}	—	111	—	°C/W	Note 1
Junction-to-Ambient Thermal Resistance, 8LD WDFN	θ_{JA}	—	61	—	°C/W	Note 1
Junction-to-Top Characterization Parameter, 8LD MSOP	Ψ_{JT}	—	7	—	°C/W	Note 1
Junction-to-Top Characterization Parameter, 8LD SOIC	Ψ_{JT}	—	12	—	°C/W	Note 1
Junction-to-Top Characterization Parameter, 8LD WDFN	Ψ_{JT}	—	1.6	—	°C/W	Note 1
Junction-to-Board Characterization Parameter, 8LD MSOP	Ψ_{JB}	—	130	—	°C/W	Note 1
Junction-to-Board Characterization Parameter, 8LD SOIC	Ψ_{JB}	—	76	—	°C/W	Note 1
Junction-to-Board Characterization Parameter, 8LD WDFN	Ψ_{JB}	—	29	—	°C/W	Note 1

Note 1: Parameter is determined using High K 2S2P 4-Layer board as described in JESD 51-7, as well as JESD 51-5 for packages with exposed pads

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

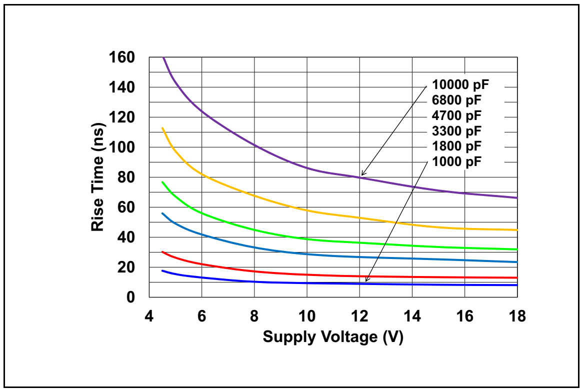


FIGURE 2-1: Rise Time vs. Supply Voltage.

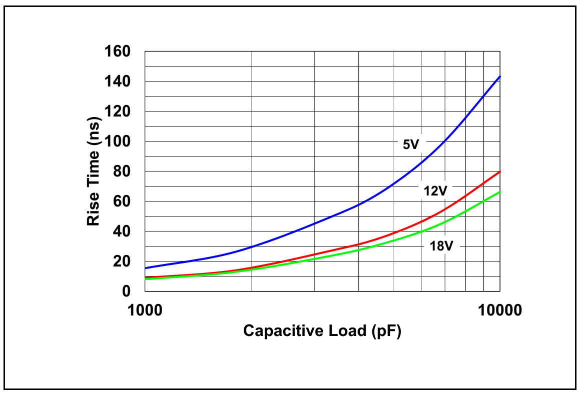


FIGURE 2-2: Rise Time vs. Capacitive Load.

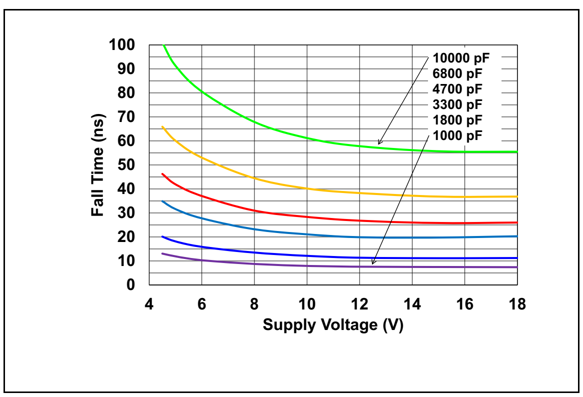


FIGURE 2-3: Fall Time vs. Supply Voltage.

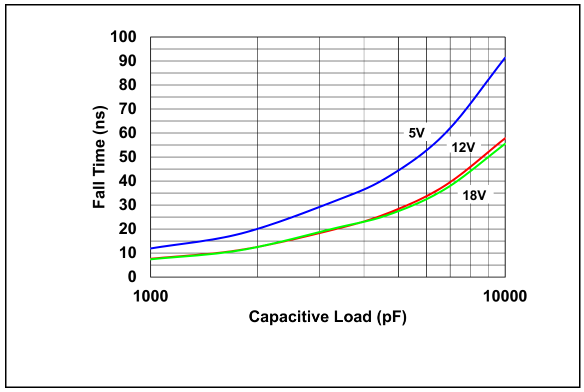


FIGURE 2-4: Fall Time vs. Capacitive Load.

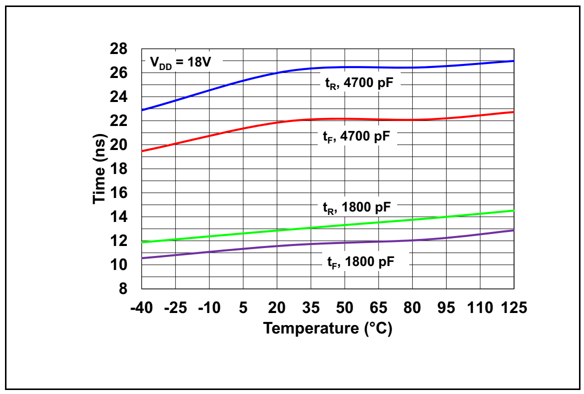


FIGURE 2-5: Rise and Fall Time vs. Temperature.

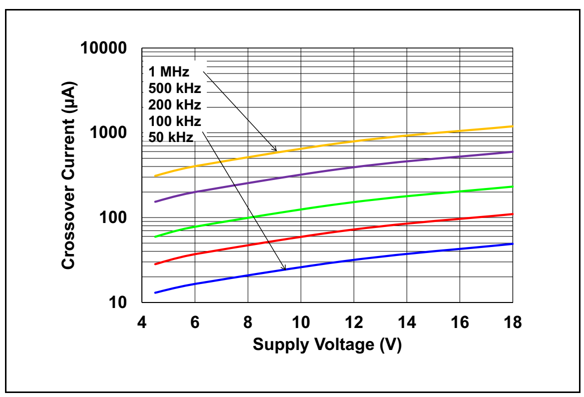


FIGURE 2-6: Crossover Current vs. Supply Voltage.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

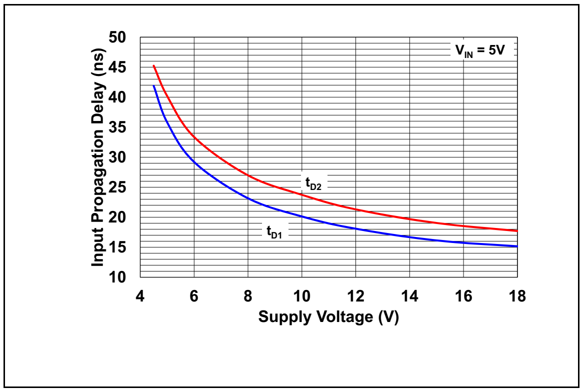


FIGURE 2-7: *Input Propagation Delay vs. Supply Voltage.*

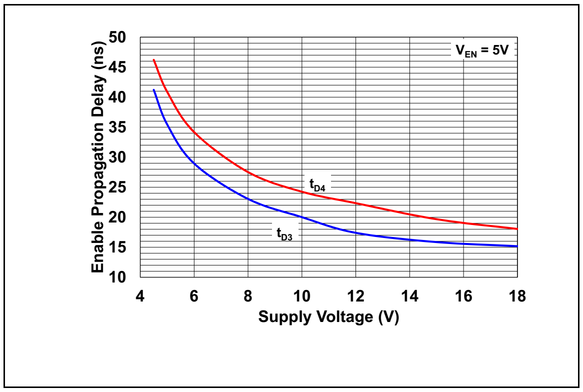


FIGURE 2-10: *Enable Propagation Delay vs. Supply Voltage.*

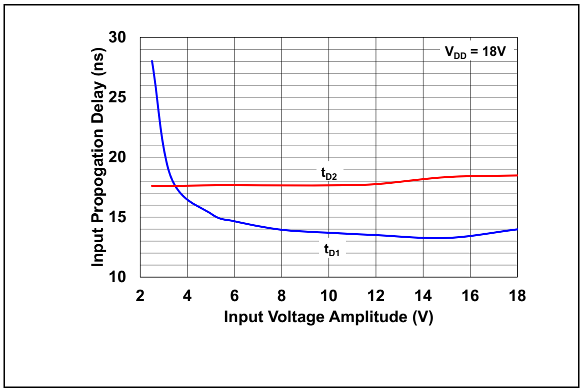


FIGURE 2-8: *Input Propagation Delay Time vs. Input Amplitude.*

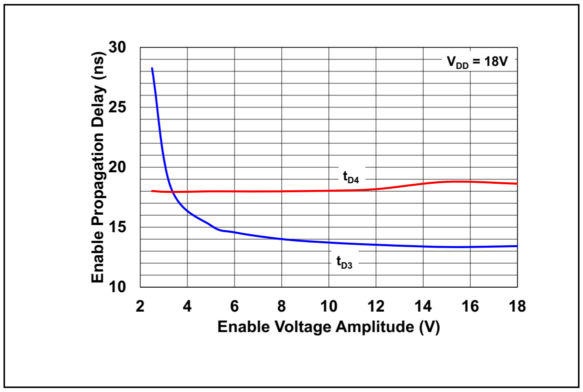


FIGURE 2-11: *Enable Propagation Delay Time vs. Enable Voltage Amplitude.*

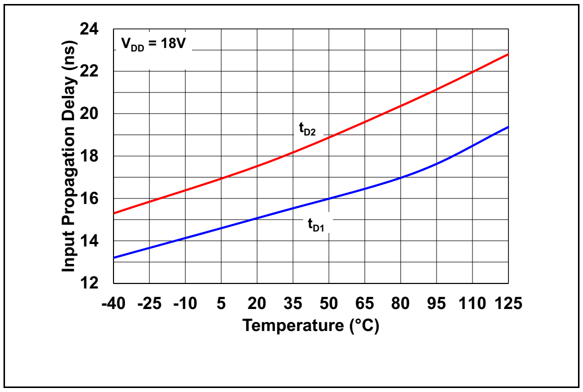


FIGURE 2-9: *Input Propagation Delay vs. Temperature.*

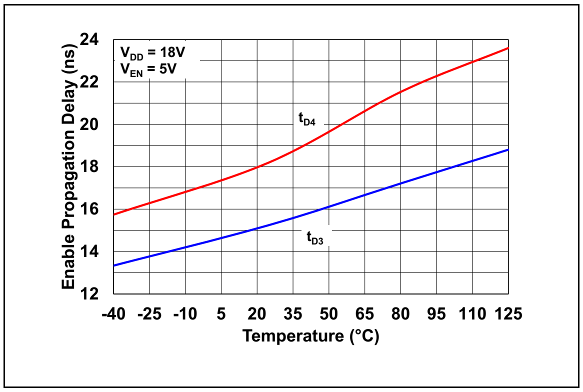


FIGURE 2-12: *Enable Propagation Delay vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

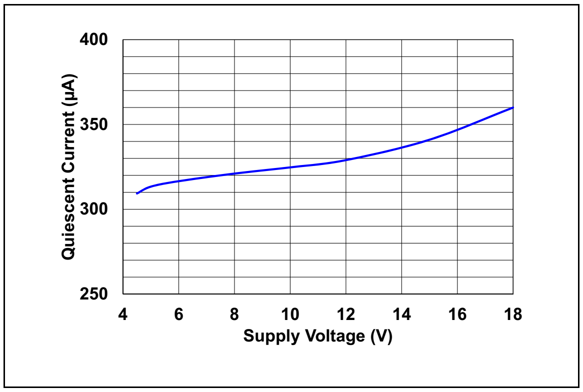


FIGURE 2-13: *Quiescent Supply Current vs. Supply Voltage.*

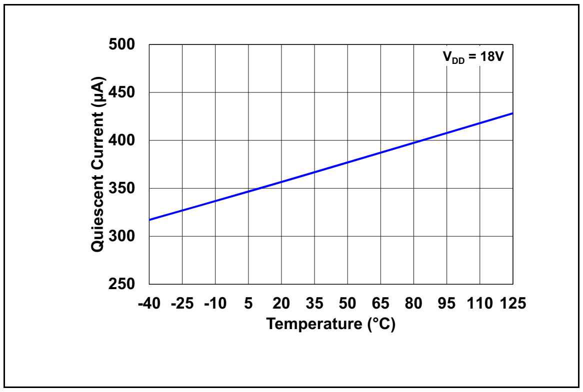


FIGURE 2-14: *Quiescent Supply Current vs. Temperature.*

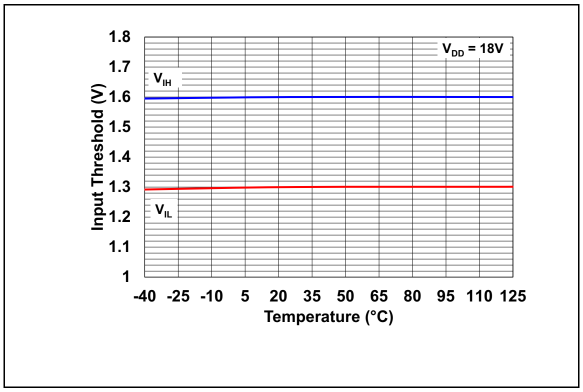


FIGURE 2-15: *Input Threshold vs. Temperature.*

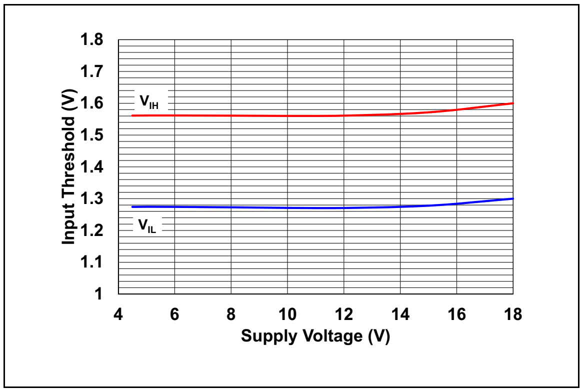


FIGURE 2-16: *Input Threshold vs Supply Voltage.*

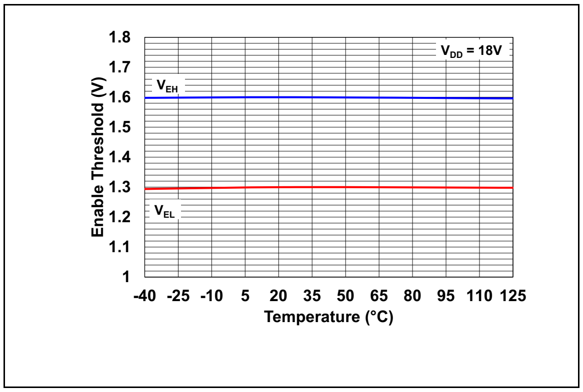


FIGURE 2-17: *Enable Threshold vs. Temperature.*

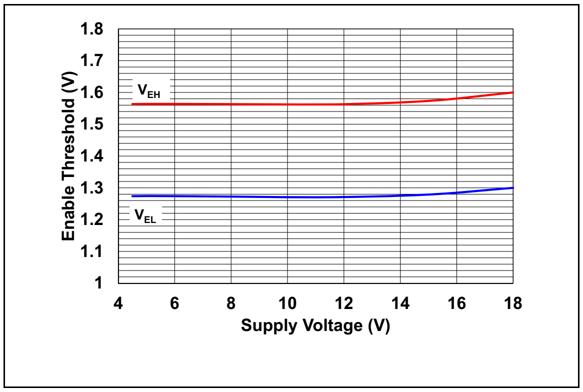


FIGURE 2-18: *Enable Threshold vs Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

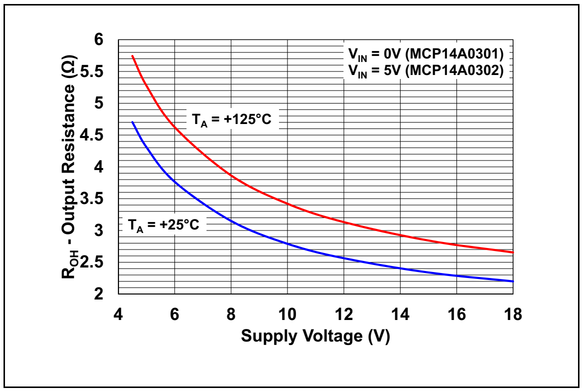


FIGURE 2-19: *Output Resistance (Output High) vs. Supply Voltage.*

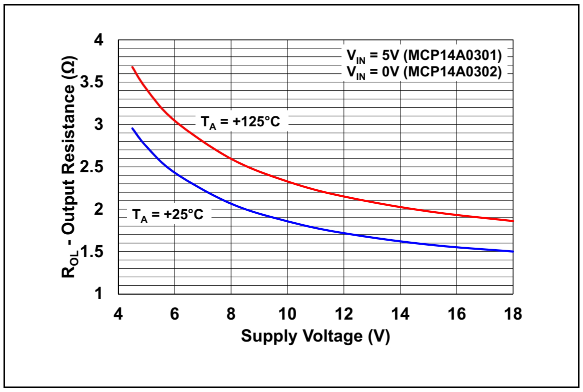


FIGURE 2-20: *Output Resistance (Output Low) vs. Supply Voltage.*

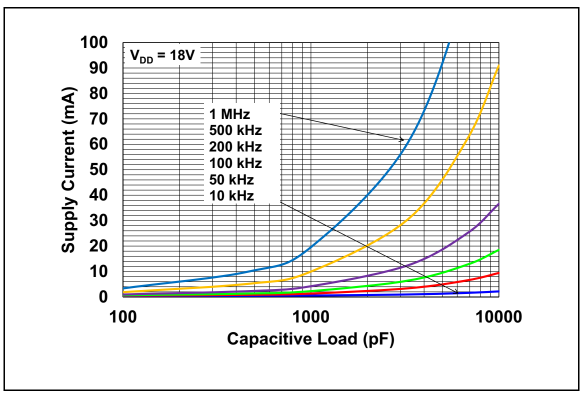


FIGURE 2-21: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

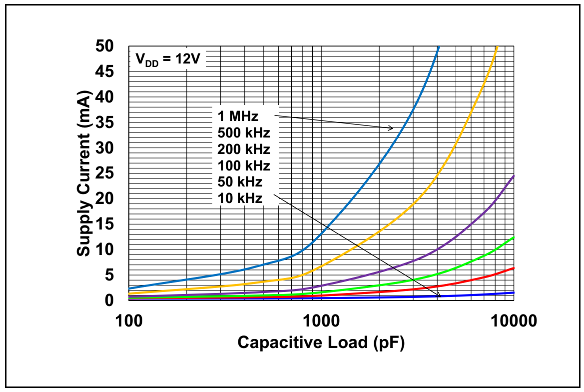


FIGURE 2-22: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

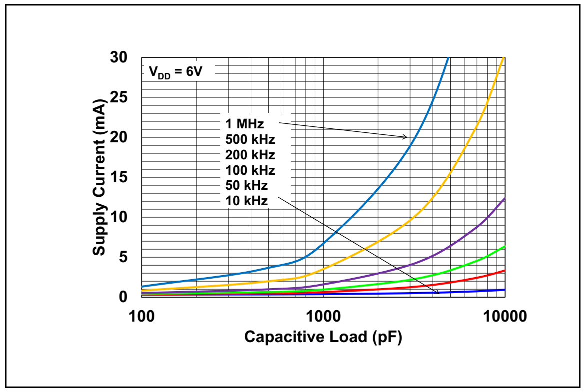


FIGURE 2-23: *Supply Current vs. Capacitive Load (V_{DD} = 6V).*

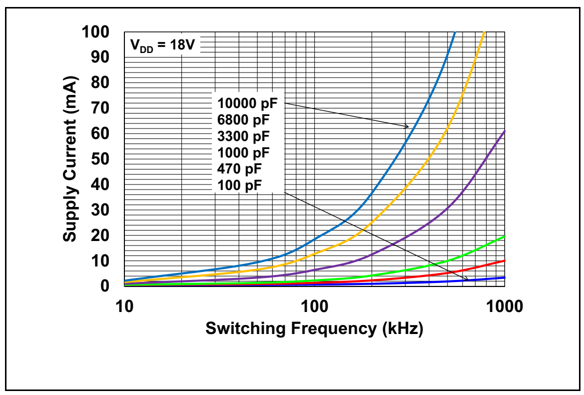


FIGURE 2-24: *Supply Current vs. Frequency (V_{DD} = 18V).*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

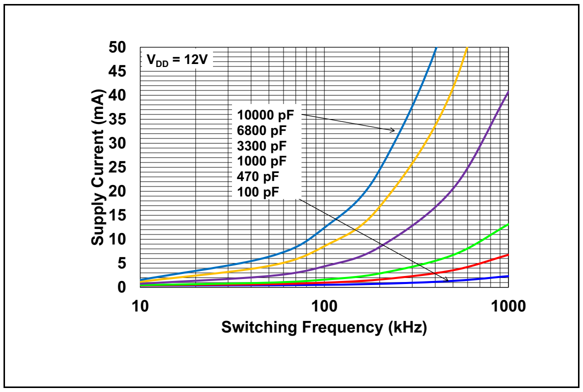


FIGURE 2-25: *Supply Current vs. Frequency (V_{DD} = 12V).*

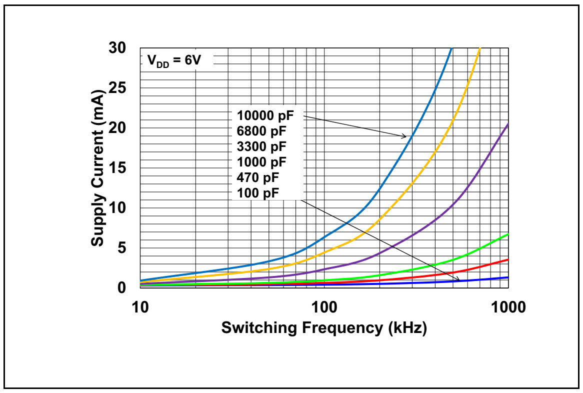


FIGURE 2-26: *Supply Current vs. Frequency (V_{DD} = 6V).*

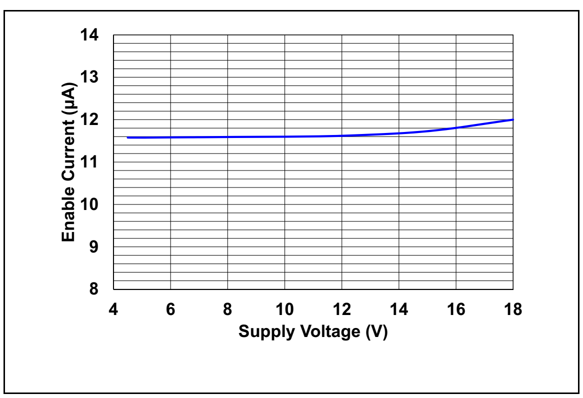


FIGURE 2-27: *Enable Current vs. Supply Voltage.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP14A0301/2		Symbol	Description
8L 2 x 2 WDFN	8L MSOP/SOIC		
1	1	V_{DD}	Supply Input
2	2	IN	Control Input
3	3	EN	Device Enable
4	4	GND	Power Ground
5	5	GND	Power Ground
6	6	$\overline{OUT}$/OUT	Push-Pull Output
7	7	$\overline{OUT}$/OUT	Push-Pull Output
8	8	V_{DD}	Supply Input
EP	—	EP	Exposed Thermal Pad (GND)

3.1 Supply Input Pin (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.2 Control Input Pin (IN)

The MOSFET driver Control Input is a high-impedance input featuring low threshold levels. The Input also has hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.3 Device Enable Pin (EN)

The MOSFET driver Device Enable is a high-impedance input featuring low threshold levels. The Enable input also has hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity. Driving the Enable pin below the threshold will disable the output of the device, pulling $\overline{OUT}$/OUT low, regardless of the status of the Input pin. Driving the Enable pin above the threshold allows normal operation of the $\overline{OUT}$/OUT pin based on the status of the Input pin. The Enable pin utilizes an internal pull up resistor, allowing the pin to be left floating for standard driver operation.

3.4 Power Ground Pin (GND)

GND is the device return pin for the input and output stages. The GND pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow out of the ground pin.

3.5 Output Pin ($\overline{OUT}$, OUT)

The Output is a CMOS push-pull output that is capable of sourcing and sinking 3.0A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET stays in the intended state even during large transients. This output also has a reverse current latch-up rating of 500 mA.

3.6 Exposed Metal Pad Pin (EP)

The exposed metal pad of the WDFN package is internally connected to GND. Therefore, this pad should be connected to a Ground plane to aid in heat removal from the package.

NOTES:

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices that are intended to source/sink high-peak currents to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver such as the MCP14A0301/2 family can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14A0301/2 timing.

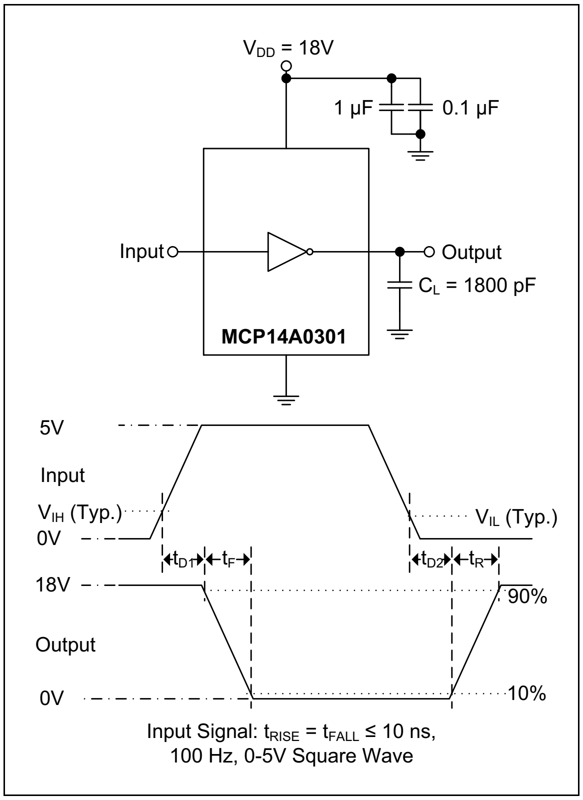


FIGURE 4-1: Inverting Driver Timing Waveform.

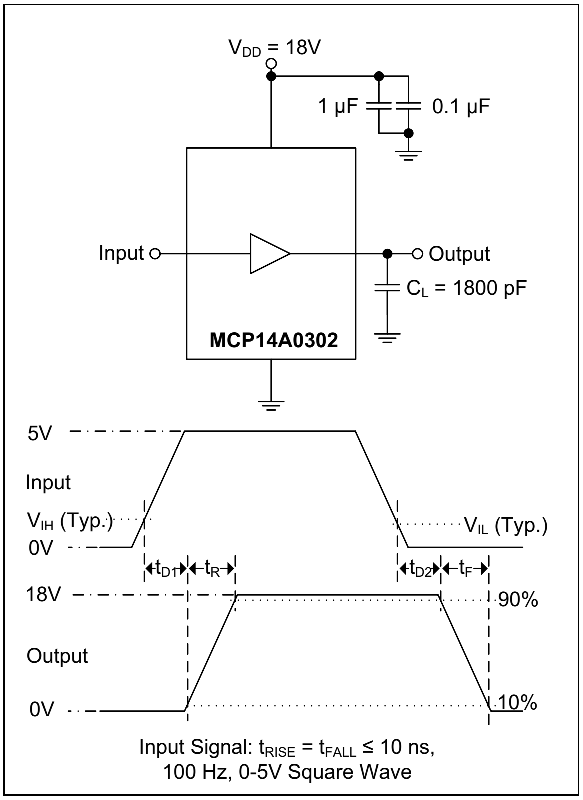


FIGURE 4-2: Noninverting Driver Timing Waveform.

4.3 Enable Function

The enable pin (EN) provides additional control of the output pin (OUT). This pin is active high and is internally pulled up to V_{DD} so that the pin can be left floating to provide standard MOSFET driver operation.

When the enable pin's input voltage is above the enable pin high voltage threshold, (V_{EN_H}), the output is enabled and allowed to react to the status of the Input pin. However, when the voltage applied to the Enable pin falls below the low threshold voltage (V_{EN_L}), the driver's output is disabled and doesn't respond to changes in the status of the Input pin. When the driver is disabled, the output is pulled down to a low state. Refer to Table 4-1 for enable pin logic. The threshold voltage levels for the Enable pin are similar to the threshold voltage levels of the Input pin. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4}, are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

ENB	IN	MCP14A0301 OUT	MCP14A0302 OUT
H	H	L	H
H	L	H	L
L	X	L	L

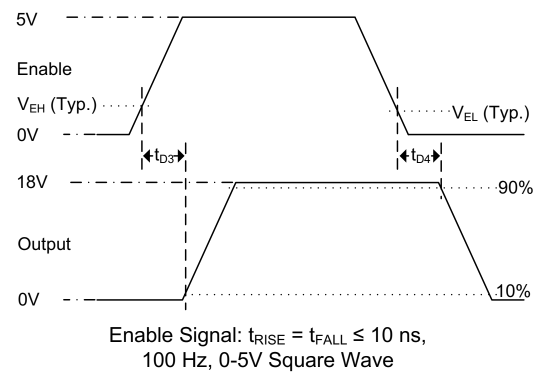


FIGURE 4-3: *Enable Timing Waveform.*

4.4 Decoupling Capacitors

Careful Printed Circuit Board (PCB) layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place 1.0 µF and 0.1 µF low ESR ceramic capacitors in parallel between the driver V_{DD} and GND. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper PCB layout is important in high-current, fast-switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. The PCB trace loop length and inductance should be minimized by the use of ground planes or traces under the MOSFET gate drive signal. Separate analog and power grounds and local driver decoupling should also be used.

Placing a ground plane beneath the MCP14A0301/2 devices will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements, as shown in Equation 4-1.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

P_T	=	Total power dissipation
P_L	=	Load power dissipation
P_Q	=	Quiescent power dissipation
P_{CC}	=	Operating power dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

f	=	Switching frequency
C_T	=	Total load capacitance
V_{DD}	=	MOSFET driver supply voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the Input and Enable pins. See **Section 1.0 "Electrical Characteristics"** for typical quiescent current draw values in different operating states. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

I_{QH}	=	Quiescent current in the High state
D	=	Duty cycle
I_{QL}	=	Quiescent current in the Low state
V_{DD}	=	MOSFET driver supply voltage

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation described in Equation 4-4.

EQUATION 4-4:

$$P_{CC} = V_{DD} \times I_{CO}$$

Where:

I_{CO}	=	Crossover Current
V_{DD}	=	MOSFET driver supply voltage

NOTES:

5.0 PACKAGING INFORMATION

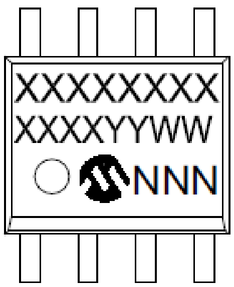
5.1 Package Marking Information

8-Lead MSOP

Part Number	Code
MCP14A0301-E/MS	A0301
MCP14A0301T-E/MS	A0301
MCP14A0302-E/MS	A0302
MCP14A0302T-E/MS	A0302

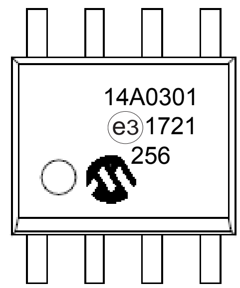
Example:

8-Lead SOIC

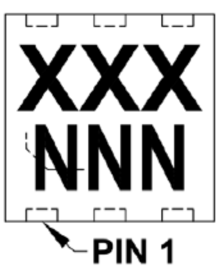


Part Number	Code
MCP14A0301-E/SN	14A0301
MCP14A0301T-E/SN	14A0301
MCP14A0302-E/SN	14A0302
MCP14A0302T-E/SN	14A0302

Example:

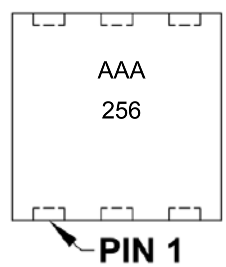


8-Lead WDFN



Part Number	Code
MCP14A0301T-E/KBA	AAA
MCP14A0302T-E/KBA	AAB

Example:



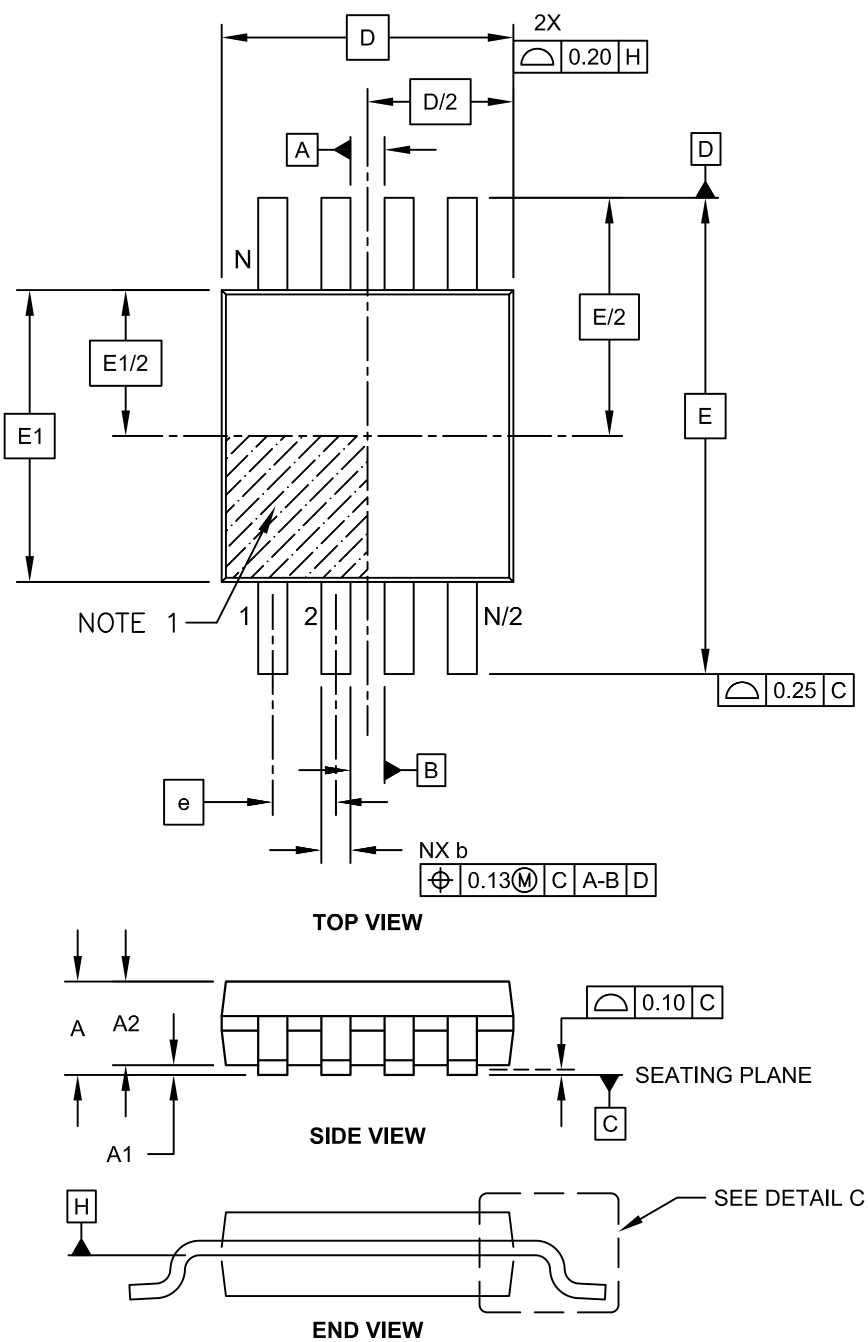
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

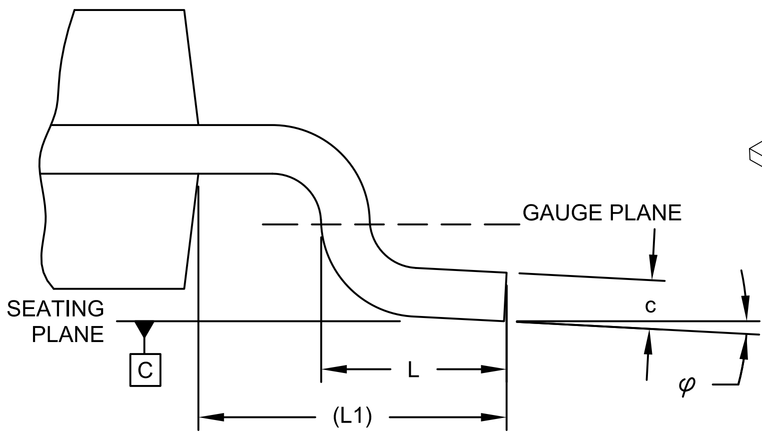
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



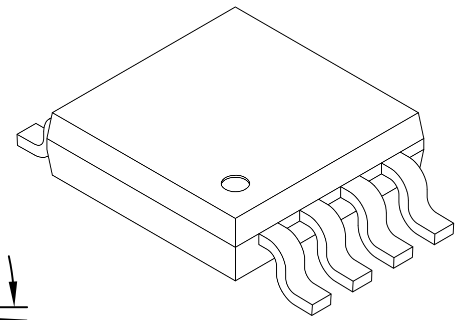
Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C



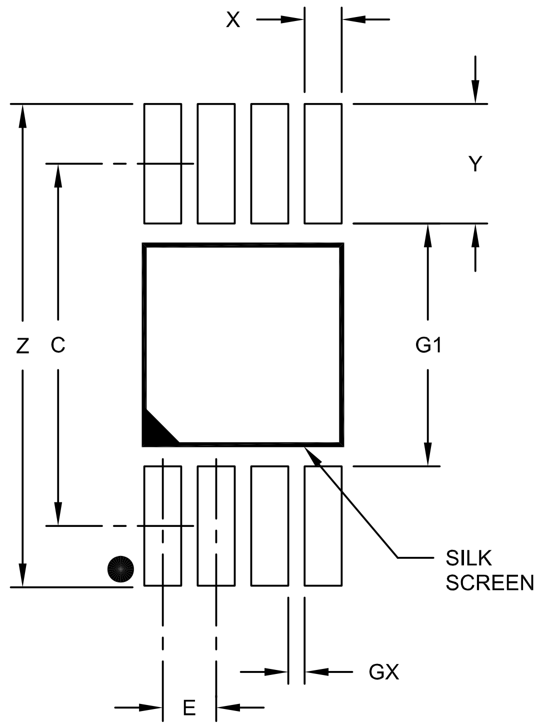
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

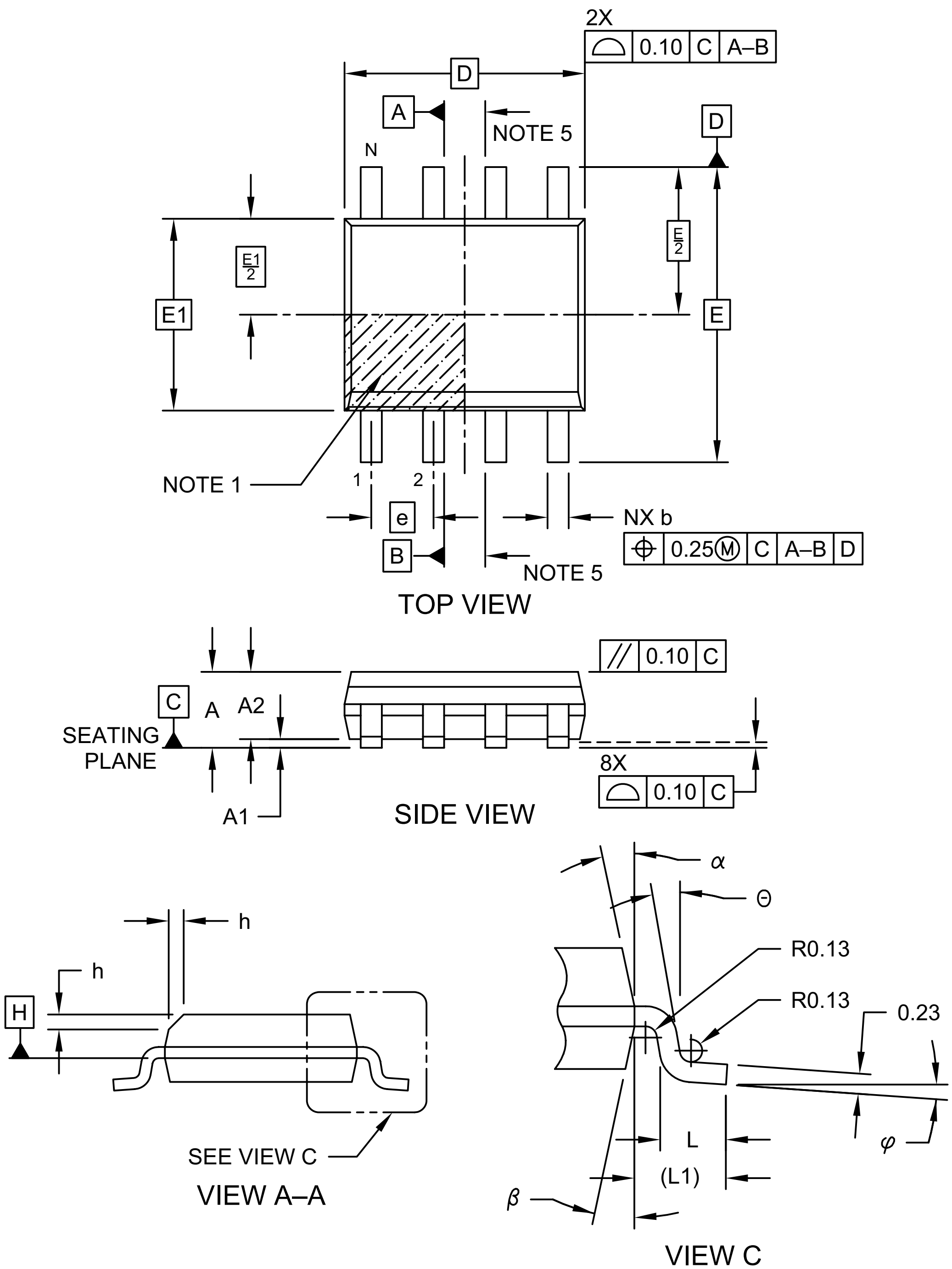
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

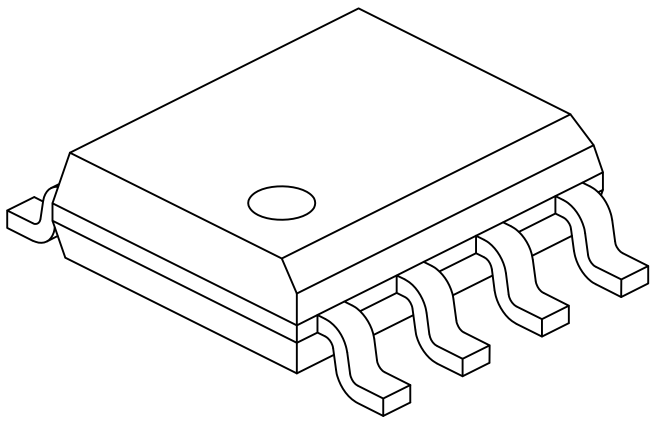
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

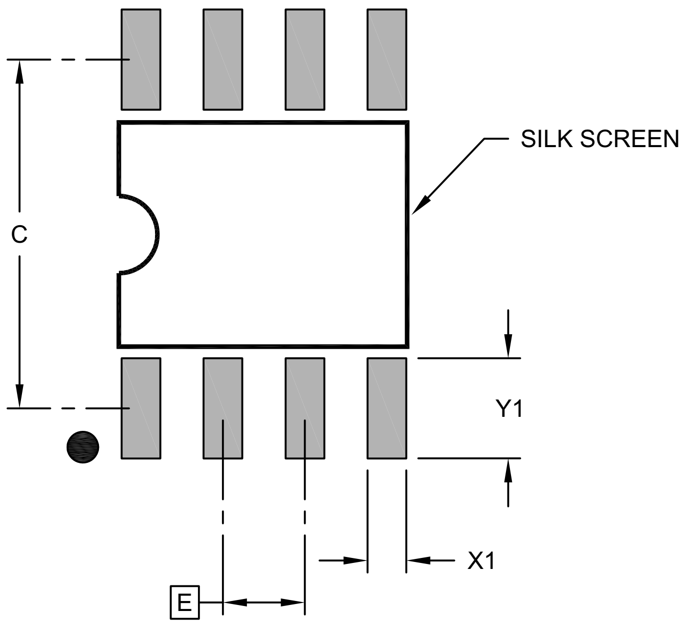
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

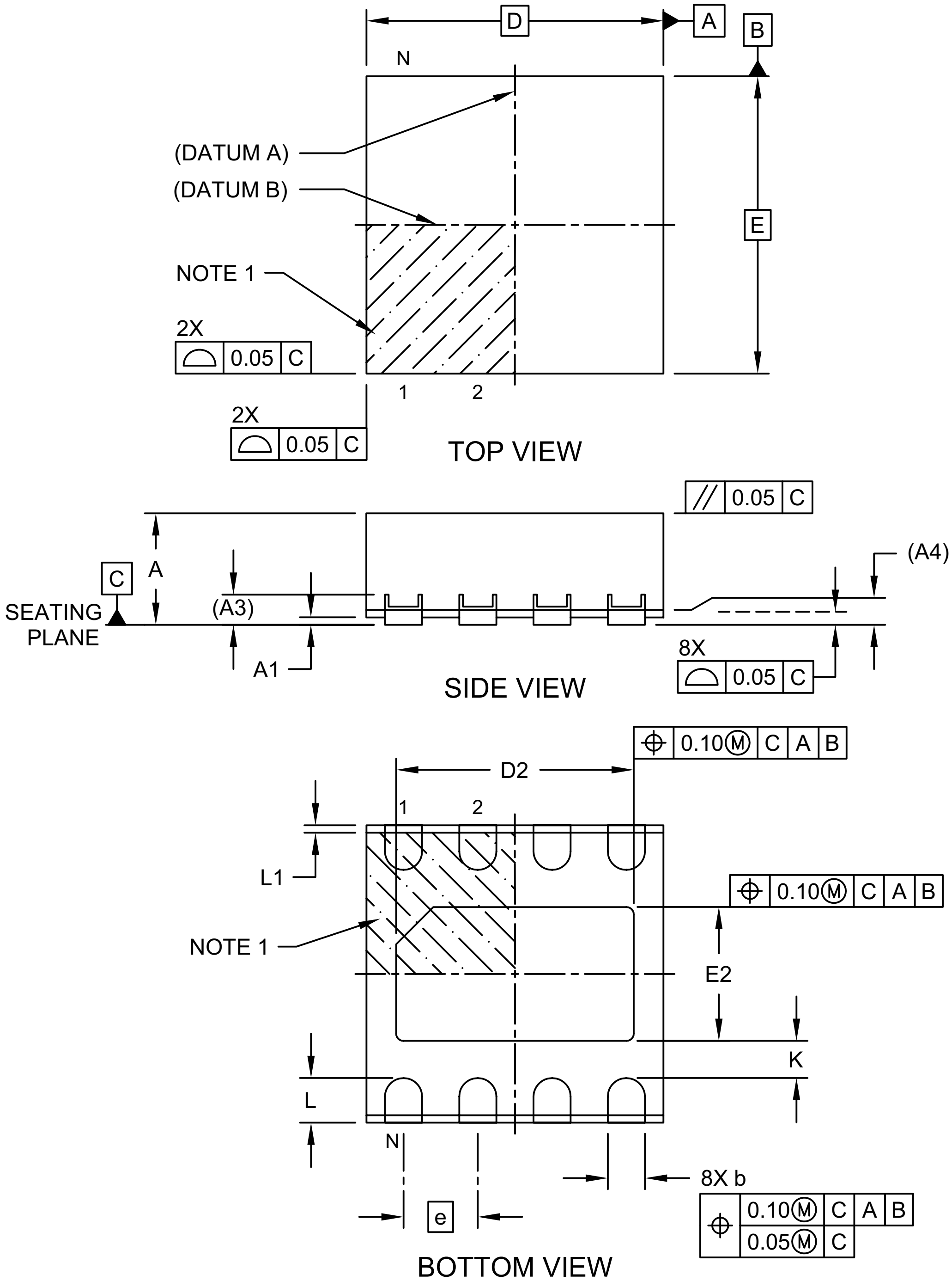
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Very, Very Thin Dual FlatPack, No Lead Package (KBA) - 2x2 mm Body [WDFN] Wettable Flanks (Stepped); Saw Singulated

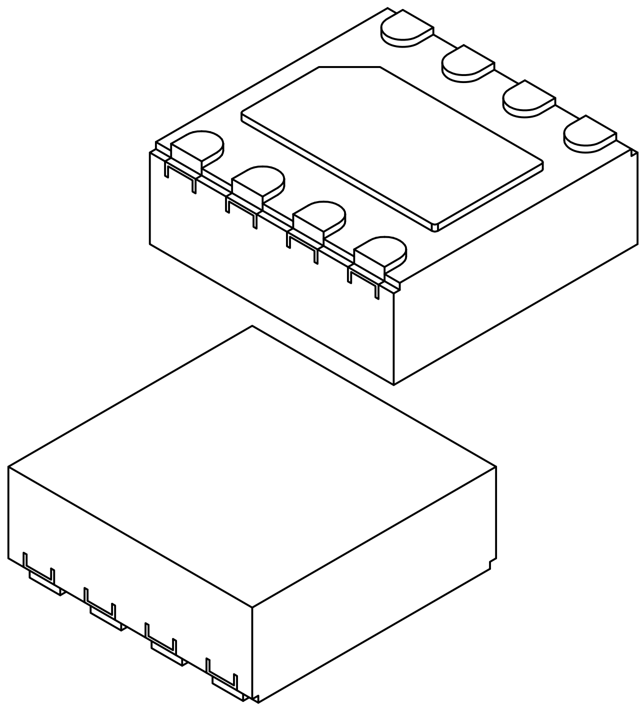
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1218A Sheet 1 of 2

8-Lead Very, Very Thin Dual FlatPack, No Lead Package (KBA) - 2x2 mm Body [WDFN] Wettable Flanks (Stepped); Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Step Height	A4		0.100 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.50	1.60	1.70
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.80	0.90	1.00
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Step Length	L1		0.050 REF	
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

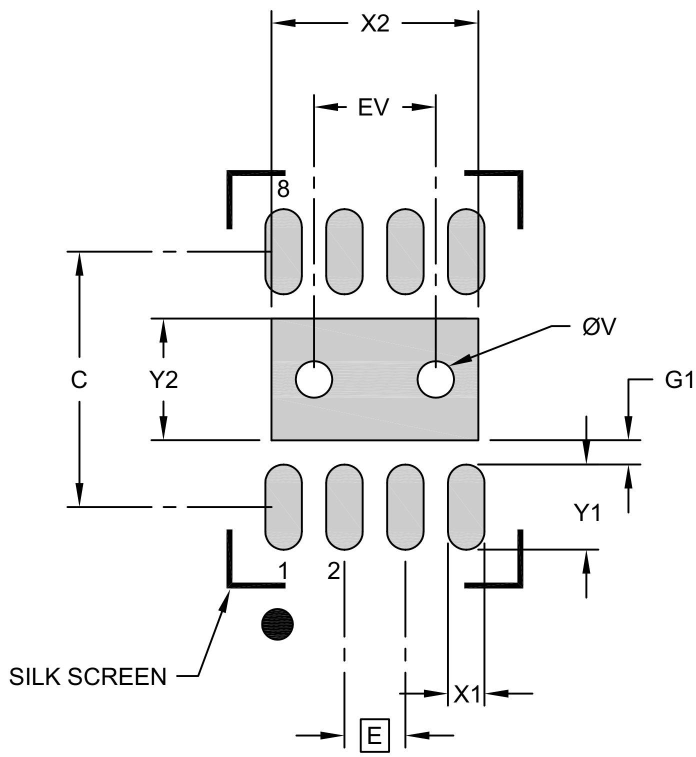
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1218A Sheet 2 of 2

8-Lead Very, Very Thin Dual FlatPack, No Lead Package (KBA) - 2x2 mm Body [WDFN] Wettable Flanks (Stepped); Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	Y2			1.00
Optional Center Pad Length	X2			1.70
Contact Pad Spacing	C		2.10	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.70
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21218A

APPENDIX A: REVISION HISTORY

Revision A (July 2017)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	–X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP14A0301T: High-Speed MOSFET Driver (Tape and Reel) MCP14A0302T: High-Speed MOSFET Driver (Tape and Reel)
Temperature Range:	E = -40°C to +125°C (Extended)
Package:	MS = Plastic Micro Small Outline Package (MSOP),8-lead 8-lead SN = Plastic Small Outline Package (SOIC), 8-lead KBA = Plastic Dual Flat, No Lead Package, Wettable Flanks 2 x 2 mm Body (WDFN) 8-lead

Examples:

a) MCP14A0301T-E/MS: Tape and Reel, Extended temperature, 8LD MSOP package

b) MCP14A0302T-E/SN: Tape and Reel, Extended temperature, 8LD SOIC package

c) MCP14A0302T-E/KBA: Tape and Reel Extended temperature, 8LD WDFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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