NISSHINBO

# RP131x SERIES

## LOW ON RESISTANCE / LOW VOLTAGE 1A LDO

NO.EA-174-230419

## OUTLINE

The RP131x Series are voltage-regulators with a built-in low ON-resistance transistor and output current is 1A capability. These ICs are capable of the low input voltage (Min.1.6V) and also the minimum output voltage can be set from 0.8V. (The output voltage is fixed in the IC.)

Each of these ICs consists of a voltage reference unit, an error amplifier, a resistor net for setting output voltage, a chip enable circuit, current limit circuits for over-current and short, and a thermal-shutdown circuit.

A standby mode with ultra low supply current can be realized with the chip enable function.

The packages for these ICs are DFN1616-6B and DFN(PL)1820-6 which are suitable for high density mounting of the ICs on boards. SOT-89-5, HSOP-6J and TO-252-5-P2 with high power dissipation are also available.

## FEATURES

- Output Current ..... Min. 1A
- Supply Current ..... Typ. 65μA
- Standby Current ..... Typ. 0.15μA
- Input Voltage Range ..... 1.6V to 6.5V
- Output Voltage Range ..... 0.8V to 5.5V [(1)](0.1V steps)
- Dropout Voltage ..... Typ. 0.5V ($V_{OUT}$=2.8V, $I_{OUT}$=1A)
- Ripple Rejection ..... Typ. 70dB (f=1kHz, $V_{OUT}$=2.8V)
- Output Voltage Accuracy ..... ±1.0%
- Temperature-Drift Coefficient of Output Voltage ..... Typ. ±100ppm/°C
- Line Regulation ..... Typ. 0.05%/V
- Load Regulation ..... Typ. 20mV at $I_{OUT}$=300mA, Typ. 80mV at $I_{OUT}$=1A
- Packages ..... DFN1616-6B, DFN(PL)1820-6, SOT-89-5, HSOP-6J, TO-252-5-P2
- Built-in Inrush current limit circuit ..... Typ. 500mA
- Built-in Fold-Back Protection Circuit ..... Typ. 250mA (Current at short mode)
- Built-in Thermal Shutdown Circuit ..... Thermal Shutdown Temperature ; Typ. 165°C
  Released Temperature ; Typ. 135°C
- Built-in Auto Discharge Function ..... D version
- Ceramic capacitors are recommended to be used with this IC .... 2.2μF or more ($V_{OUT}$≤3.6V)
  4.7μF or more ($V_{OUT}$>3.6V)

## APPLICATIONS

- Power source for battery-powered equipment.
- Power source for portable communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for Notebook PC.
- Power source for home appliances.

(1) For other voltages, please refer to MARK INFORMATIONS.

# SELECTION GUIDE

The output voltage, auto discharge function, package for the ICs can be selected at the user's request.

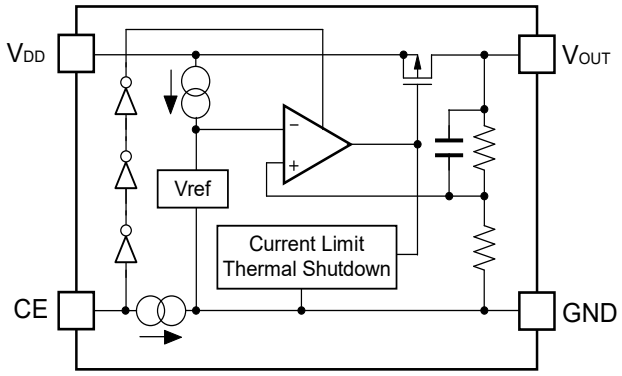
| Product Name | Package | Quantity per Reel | Pb Free | Halogen Free |
|---|---|---|---|---|
| RP131Lxx1∗-TR | DFN1616-6B | 5,000 pcs | Yes | Yes |
| RP131Kxx1∗-TR | DFN(PL)1820-6 | 5,000 pcs | Yes | Yes |
| RP131Hxx1∗-T1-FE | SOT-89-5 | 1,000 pcs | Yes | Yes |
| RP131Sxx1∗-E2-FE | HSOP-6J | 1,000 pcs | Yes | Yes |
| RP131Jxx1∗-T1-FE | TO-252-5-P2 | 3,000 pcs | Yes | Yes |

xx : The output voltage can be designated in the range from 0.8V(08) to 5.5V(55) in 0.1V steps.
(For other voltages, please refer to MARK INFORMATIONS.)

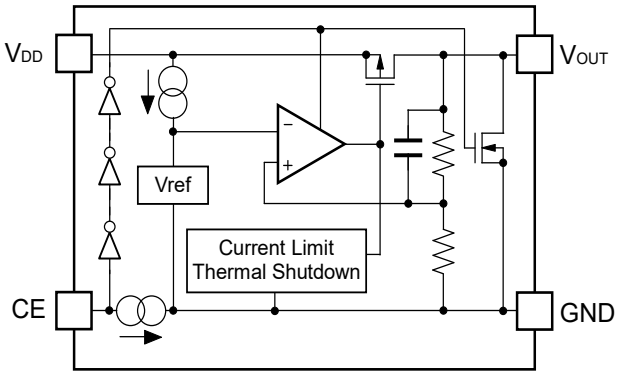
∗ : The auto discharge function at off state are options as follows.(1)
(B) without auto discharge function at off state
(D) with auto discharge function at off state

# BLOCK DIAGRAMS

**RP131xxx1B**



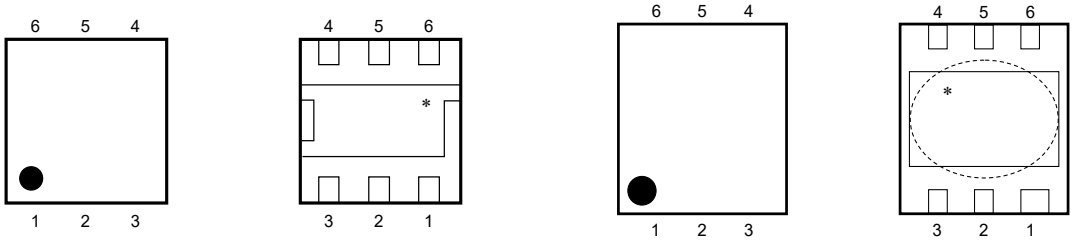

**RP131xxx1D**



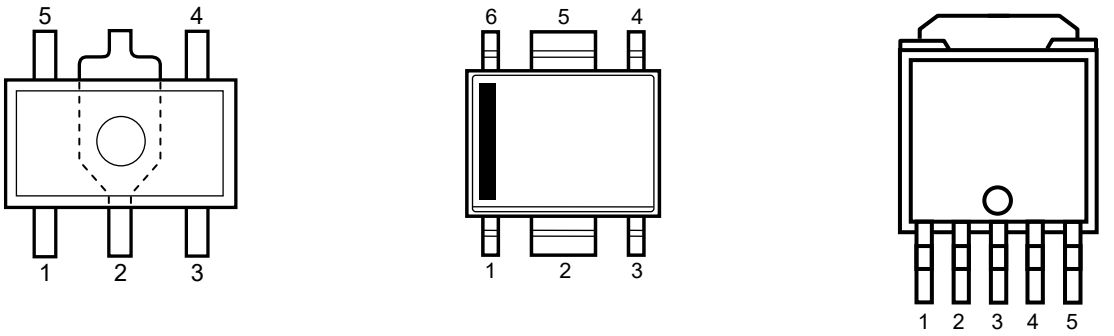

(1) Auto-discharge function quickly lowers the output voltage to 0V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

# PIN DESCRIPTIONS

**Top View** **Bottom View** **Top View** **Bottom View**




**DFN1616-6B** **DFN(PL)1820-6**




**SOT-89-5** **HSOP-6J** **TO-252-5-P2**

∗Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

### RP131L (DFN1616-6B) Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | VOUT | Output Pin(1) |
| 2 | VOUt | Output Pin(1) |
| 3 | GND | Ground Pin |
| 4 | CE | Chip Enable Pin ("H" Active) |
| 5 | VDD | Input Pin(1) |
| 6 | VDD | Input Pin(1) |

(1) When you use this IC, please make sure be wired with 1pin with 2pin and 5pin with 6pin.

### RP131K (DFN(PL)1820-6) Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | VOUT | Output Pin(1) |
| 2 | VOUT | Output Pin(1) |
| 3 | GND | Ground Pin |
| 4 | CE | Chip Enable Pin ("H" Active) |
| 5 | VDD | Input Pin(1) |
| 6 | VDD | Input Pin(1) |

### RP131H (SOT-89-5) Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | NC | No Connection |
| 2 | GND | Ground Pin |
| 3 | CE | Chip Enable Pin ("H" Active) |
| 4 | VDD | Input Pin |
| 5 | VOUT | Output Pin |

### RP131S (HSOP-6J) Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | VOUT | Output Pin |
| 2 | GND | Ground Pin(2) |
| 3 | NC | No Connection |
| 4 | CE | Chip Enable Pin ("H" Active) |
| 5 | GND | Ground Pin(2) |
| 6 | VDD | Input Pin |

### RP131J (TO-252-5-P2) Pin Description

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | $V_{OUT}$ | Output Pin |
| 2 | GND | Ground Pin(3) |
| 3 | GND | Ground Pin(3) |
| 4 | CE | Chip Enable Pin ("H" Active) |
| 5 | $V_{DD}$ | Input Pin |

(1) When you use this IC, please make sure be wired with 1pin with 2pin and 5pin with 6pin.
(2) When you use this IC, please make sure be wired with 2pin and 5pin.
(3) When you use this IC, please make sure be wired with 2pin and 3pin.

# ABSOLUTE MAXIMUM RATINGS

| Symbol | Item | | Rating | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | | 7.0 | V |
| $V_{CE}$ | Input Voltage (CE Pin) | | −0.3 to 7.0 | V |
| $V_{OUT}$ | Output Voltage | | −0.3 to $V_{IN}$+0.3 | V |
| $P_D$ | Power Dissipation(1) | DFN1616-6B, JEDEC STD.51-7 | 2400 | mW |
| | | DFN(PL)1820-6, JEDEC STD.51-7 | 2200 | |
| | | SOT-89-5, JEDEC STD.51-7 | 2600 | |
| | | HSOP-6J, JEDEC STD.51-7 | 2700 | |
| | | TO-252-5-P2, JEDEC STD.51-7 | 3800 | |
| Tj | Junction Temperature Range | | −40 to 125 | °C |
| Tstg | Storage Temperature Range | | −55 to 125 | °C |

**ABSOLUTE MAXIMUM RATINGS**

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings is not assured.

# RECOMMENDED OPERATING CONDITIONS

| Symbol | Item | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Voltage | 1.6 to 6.5 | V |
| Ta | Operating Temperature Range | −40 to 85 | °C |

**RECOMMENDED OPERATING CONDITIONS**

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to POWER DISSIPATION for detailed information.

# ELECTRICAL CHARACTERISTICS

$V_{IN}$=Set $V_{OUT}$+1V, $I_{OUT}$=1mA
The specification in ☐ is checked and guaranteed by design engineering at −40°C≤Ta≤85°C, unless otherwise noted.

## RP131xxx1B/D

(Ta = 25°C)

| Symbol | Item | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage | Ta = 25°C | $V_{OUT}$>1.5V | ×0.99 | | ×1.01 | V |
| | | | $V_{OUT}$≤1.5V | −15 | | 15 | mV |
| | | −40°C ≤ Ta t≤ 85°C | $V_{OUT}$>1.5V | ☐×0.974 | | ☐×1.018 | V |
| | | | $V_{OUT}$≤1.5V | ☐−40 | | ☐27 | mV |
| $\Delta V_{OUT}$/ $\Delta I_{OUT}$ | Load Regulation | 0.1mA ≤ $I_{OUT}$ ≤ 300mA | | | 20 | ☐40 | mV |
| | | 0.1mA ≤ $I_{OUT}$ ≤ 1A | | | 80 | ☐120 | |
| $V_{DIF}$ | Dropout Voltage | Refer to the following table | | | | | |
| $I_{SS}$ | Supply Current | $I_{OUT}$=0mA ($V_{IN}$=6.5V) | | | 65 | ☐90 | µA |
| Istandby | Standby Current | $V_{CE}$=0V, $V_{IN}$=6.5V | | | 0.15 | 0.60 | µA |
| $\Delta V_{OUT}$/ $\Delta V_{IN}$ | Line Regulation | Set $V_{OUT}$+0.5V ≤ $V_{IN}$ ≤ 6.5V<br>∗However, $V_{IN}$ ≥ 1.6V | | | 0.05 | ☐0.1 | %/V |
| RR | Ripple Rejection | f=1kHz<br>Ripple 0.2Vp-p<br>$I_{OUT}$=100mA | $V_{OUT}$≤3.3V | | 70 | | dB |
| | | | $V_{OUT}$>3.3V | | 60 | | |
| $V_{IN}$ | Input Voltage | | | ☐1.6 | | ☐6.5 | V |
| $I_{LIM}$ | Output Current Limit | | | ☐1 | | | A |
| $\Delta V_{OUT}$/ $\Delta Ta$ | Output Voltage Temperature Coefficient | −40°C≤Ta≤85°C | | | ±100 | | ppm /°C |
| $I_{SC}$ | Short Current Limit | $V_{OUT}$=0V | | | 250 | | mA |
| $I_{PD}$ | CE Pull-down Current | | | | 0.3 | | µA |
| $V_{CEH}$ | CE Input Voltage "H" | | | ☐1.0 | | | V |
| $V_{CEL}$ | CE Input Voltage "L" | | | | | ☐0.4 | V |
| en | Output Noise | BW=10Hz to 100kHz, $I_{OUT}$=1mA | | | 45 | | µVrms |
| $T_{TSD}$ | Thermal Shutdown Temperature | Junction Temperature | | | 165 | | °C |
| $T_{TSR}$ | Thermal Shutdown Released Temperature | Junction Temperature | | | 135 | | °C |
| $R_{LOW}$ | Low Output Nch Tr. ON Resistance (of D version) | $V_{IN}$=4.0V, $V_{CE}$=0V | | | 30 | | Ω |

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj≈Ta = 25°C) except for Output Noise, Ripple Rejection, Output Voltage Temperature Coefficient, Dropout Voltage at 1A Output Current and Thermal Shutdown items.

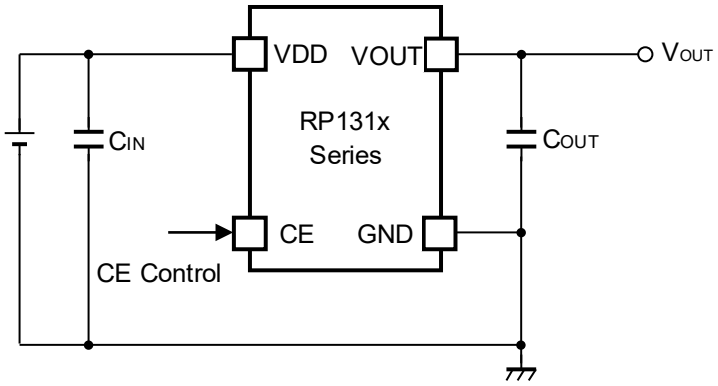
The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C, unless otherwise noted.

**Dropout Voltage** **(Ta = 25°C)**

| Output Voltage $V_{OUT}$ (V) | Dropout Voltage $V_{DIF}$ (V) | | | | | |
|---|---|---|---|---|---|---|
| | Condition | Typ. | Max. | Condition | Typ. | Max. |
| 0.8 ≤ $V_{OUT}$ < 0.9 | $I_{OUT}$=300mA | 0.600 | 0.780 | $I_{OUT}$=1A | 1.100 | 1.650 |
| 0.9 ≤ $V_{OUT}$ < 1.0 | | 0.550 | 0.690 | | 1.050 | 1.500 |
| 1.0 ≤ $V_{OUT}$ < 1.1 | | 0.450 | 0.610 | | 1.000 | 1.450 |
| 1.1 ≤ $V_{OUT}$ < 1.2 | | 0.340 | 0.540 | | 0.930 | 1.420 |
| 1.2 ≤ $V_{OUT}$ < 1.5 | | 0.290 | 0.500 | | 0.900 | 1.380 |
| 1.5 ≤ $V_{OUT}$ < 2.6 | | 0.230 | 0.310 | | 0.700 | 1.100 |
| 2.6 ≤ $V_{OUT}$ < 3.3 | | 0.150 | 0.180 | | 0.500 | 0.750 |
| 3.3 ≤ $V_{OUT}$ ≤ 5.5 | | 0.140 | 0.170 | | 0.450 | 0.650 |

# APPLICATION INFORMATION

## Typical Application Circuits




**Recommendation value of the external capacitors**

| $V_{OUT}$ | Capacitors | | |
|---|---|---|---|
| $V_{OUT} \leq 3.6V$ | $C_{IN}$ | Kyocera 2.2μF (size:1005) | [CM05X5R225M06AB] |
| | $C_{OUT}$ | Kyocera 2.2μF (size:1608) | [CM105X5R225K06AB] |
| $V_{OUT} > 3.6V$ | $C_{IN}$ | Kyocera 2.2μF (size:1608) | [CM105X5R225K06AB] |
| | $C_{OUT}$ | Kyocera 4.7μF (size:1608) | [CM105X5R475M06AB] |

## Technical Notes on the External Components

When using this IC, consider following points:

### Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor $C_{OUT}$ with good frequency characteristics and ESR (Equivalent Series Resistance).

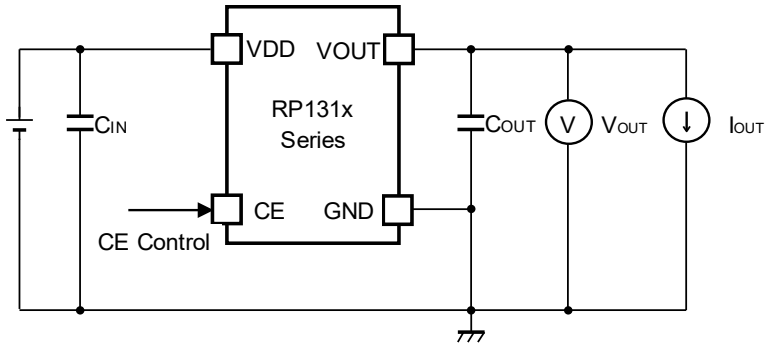
If a tantalum capacitor is used, and its ESR of $C_{OUT}$ is large, the loop oscillation may result. Because of this, select $C_{OUT}$ carefully considering its frequency characteristics.

### PCB Layout

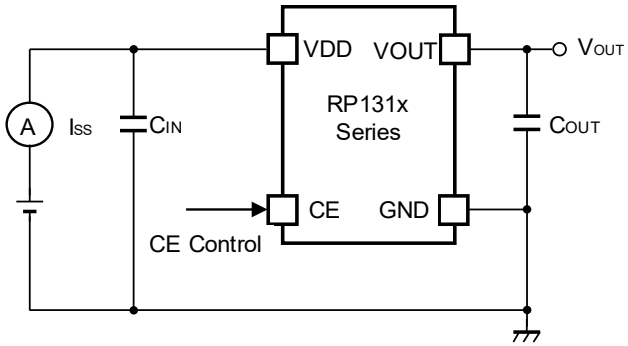
Make $V_{DD}$ and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor $C_{IN}$ between $V_{DD}$ and GND pin with a capacitance value as "Recommendation value of the external capacitors" above or more, and as close as possible to the pins.

Set external components, especially the output capacitor $C_{OUT}$, as close as possible to the ICs, and make wiring as short as possible.

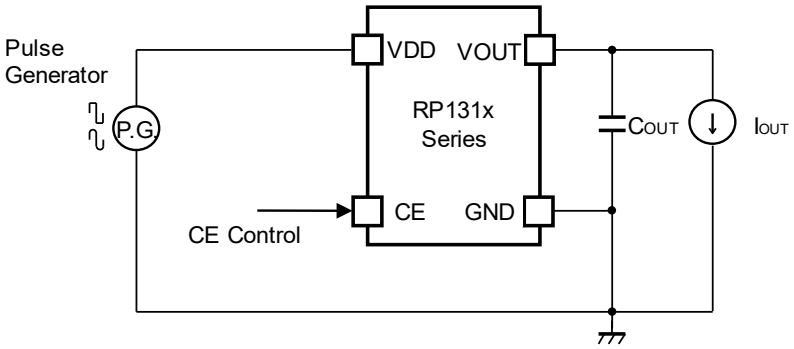
## TEST CIRCUITS



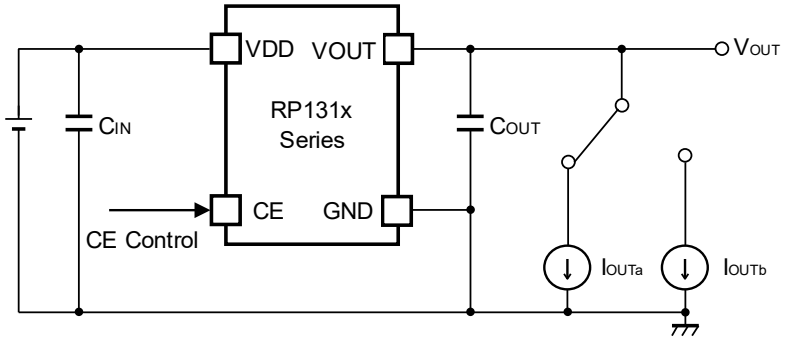

**Basic Test Circuit**




**Test Circuit for Supply Current**




**Test Circuit for Ripple Rejection**



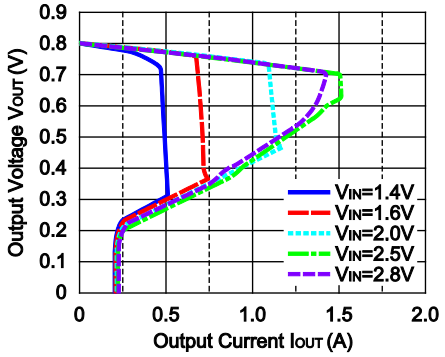

**Test Circuit for Load Transient Response**

# TYPICAL CHARACTERISTICS

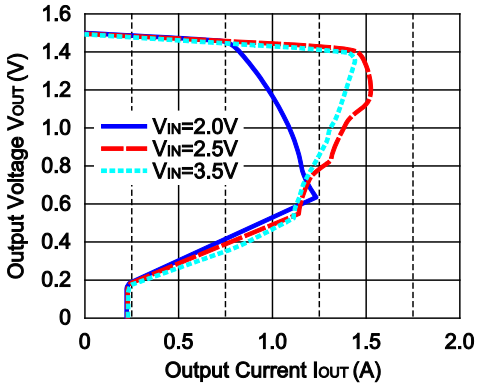
Typical Characteristics are intended to be used as reference data; they are not guaranteed.

## 1) Output Voltage vs. Output Current (Ta = 25°C)

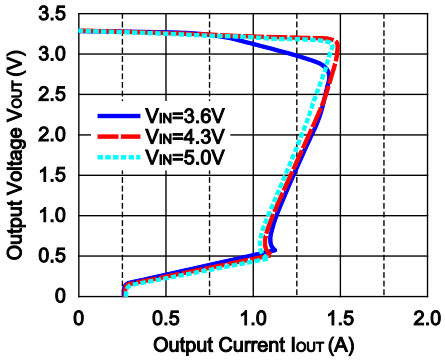
### RP131x081x



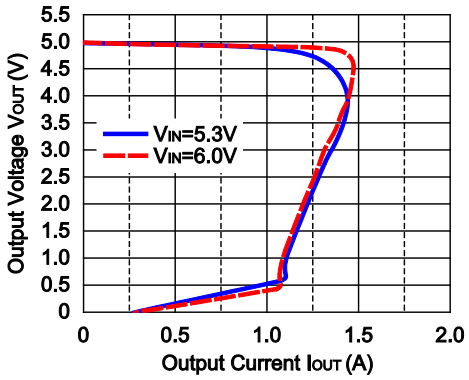

### RP131x151x




### RP131x331x

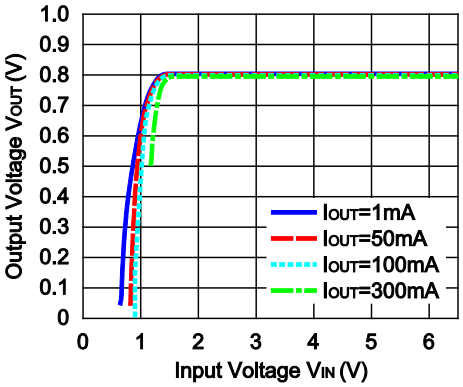



### RP131x501x

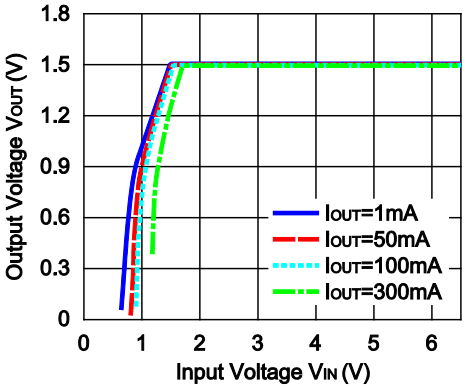



## 2) Output Voltage vs. Input Voltage (Ta=25°C)

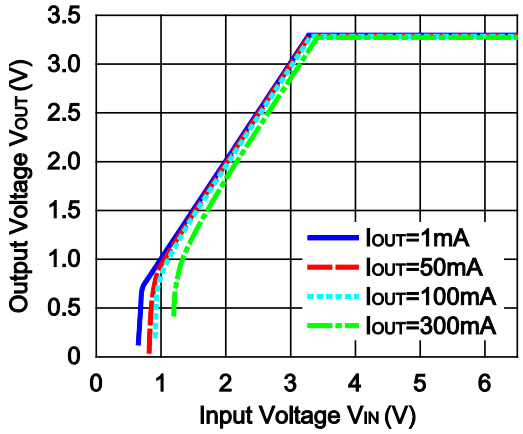
### RP131x081x



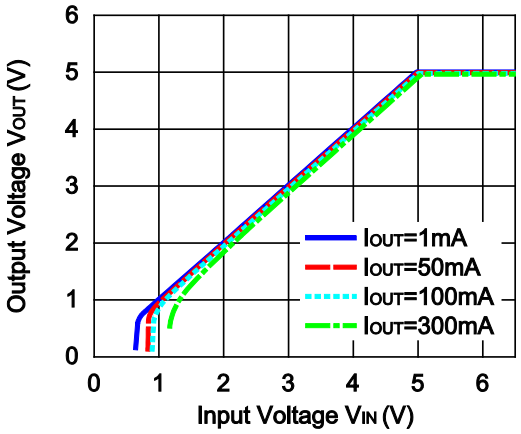

### RP131x151x



RP131x331x

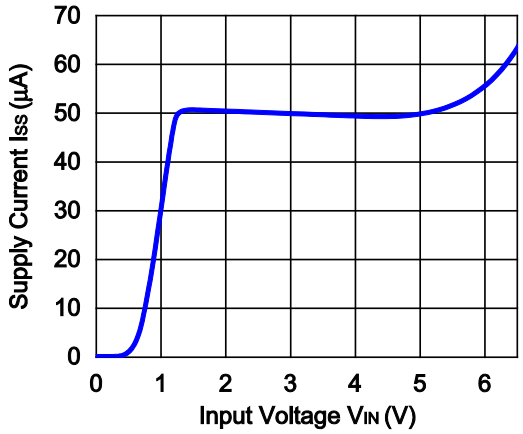



RP131x501x

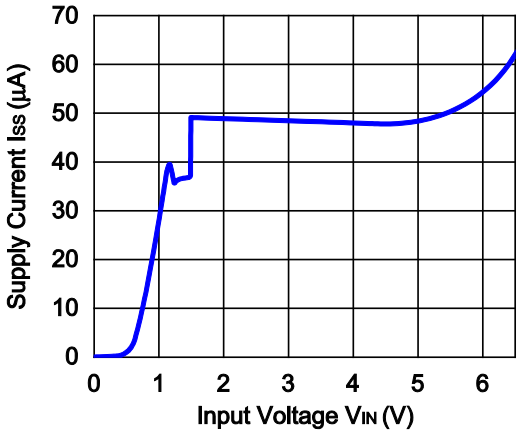



### 3) Supply Current vs. Input Voltage (Ta=25°C)

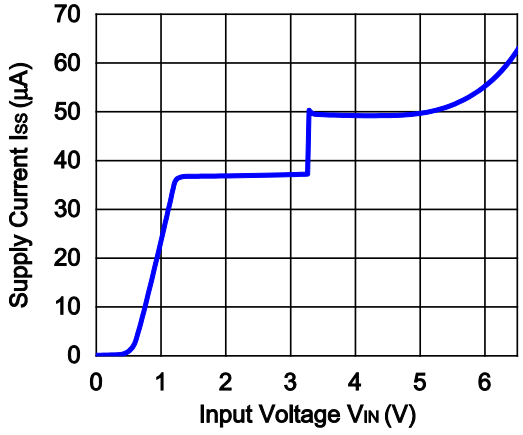
RP131x081x



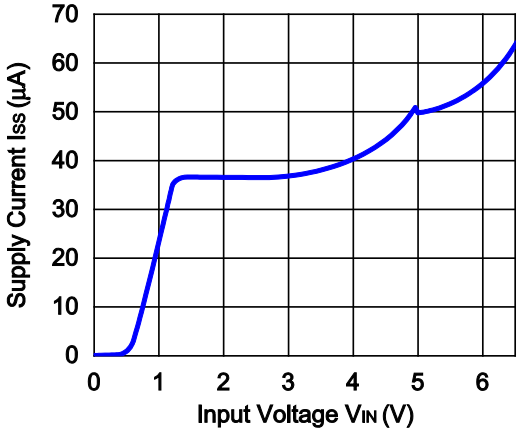

RP131x151x




RP131x331x

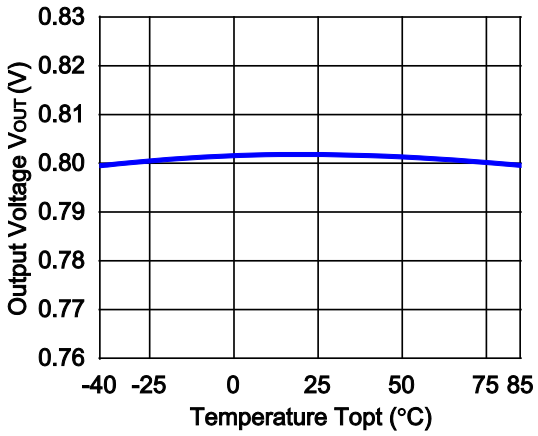



RP131x501x

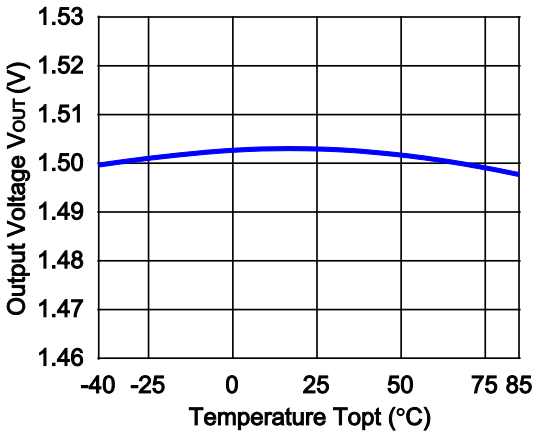


### 4) Output Voltage vs. Temperature

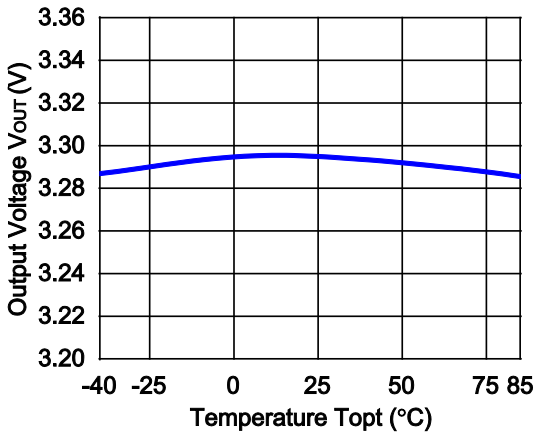
RP131x081x



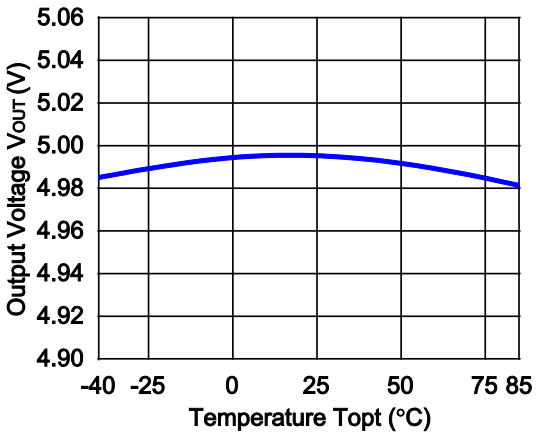

RP131x281x




RP131x331x

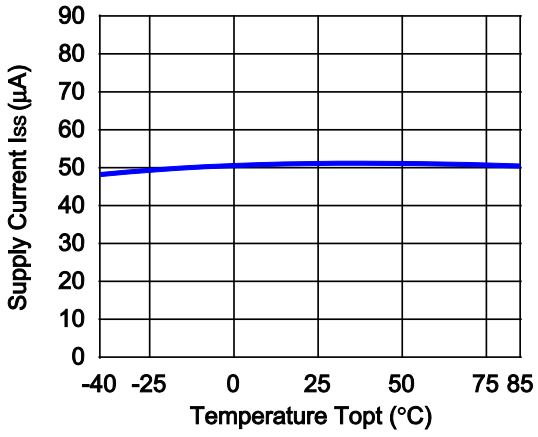



RP131x501x

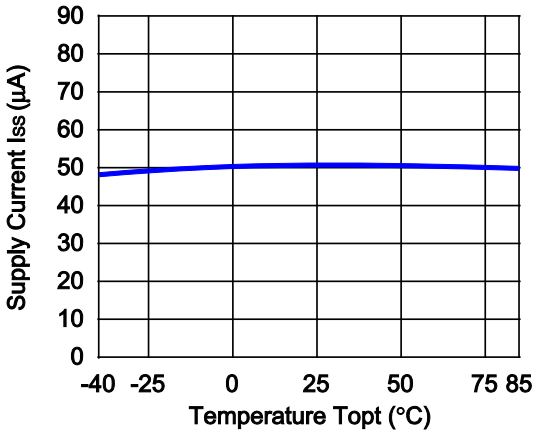



### 5) Supply Current vs. Temperature

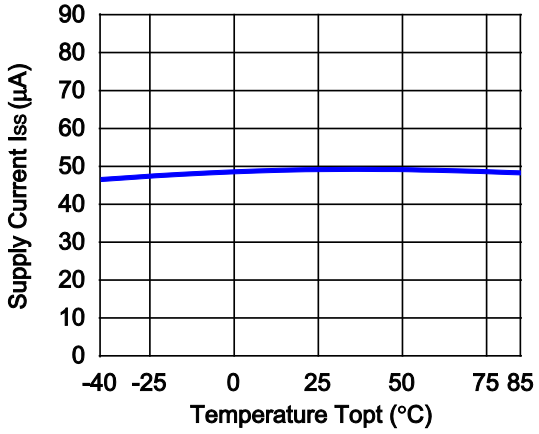
RP131x081x



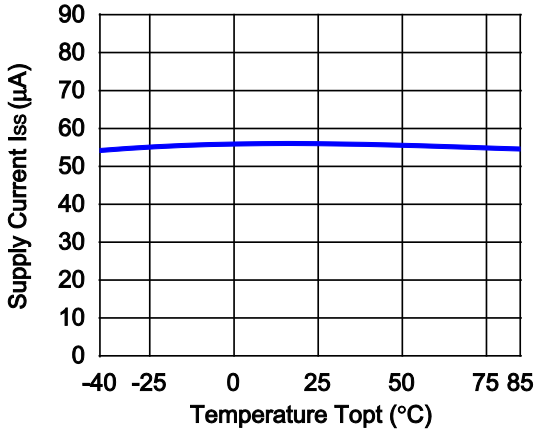

RP131x151x



RP131x331x

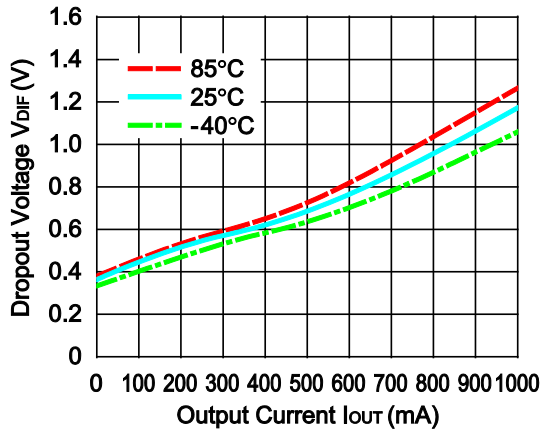



RP131x501x

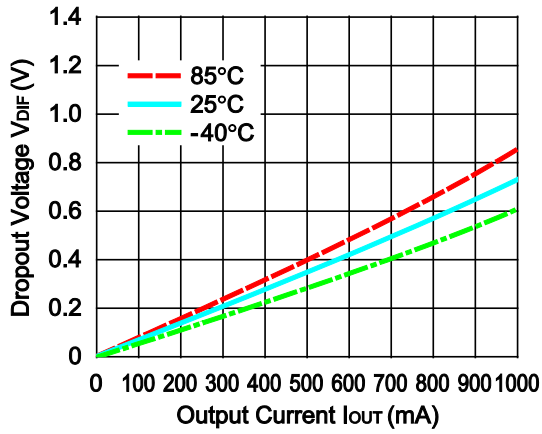



## 6) Dropout Voltage vs. Output Current

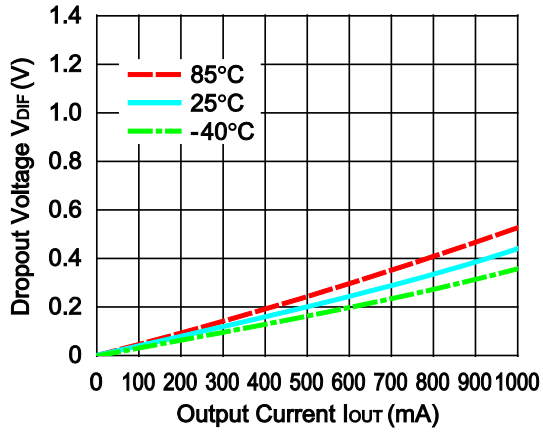
RP131x081x



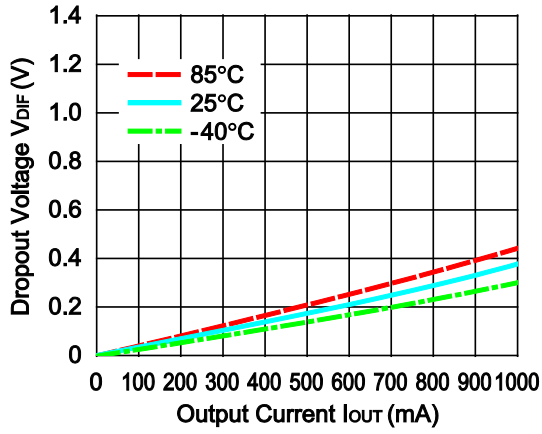

RP131x151x



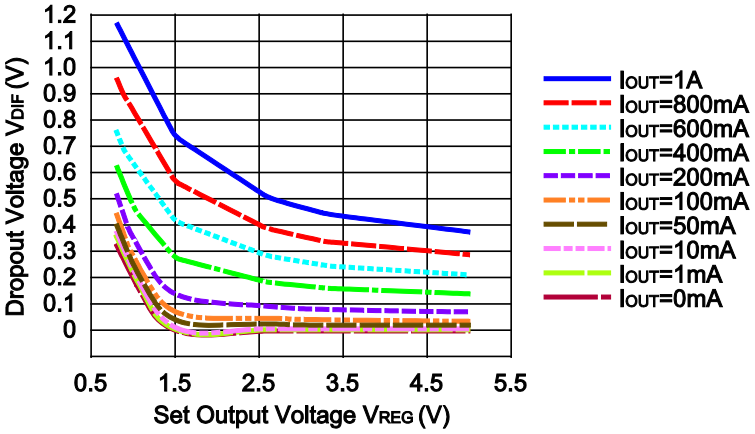

RP131x331x



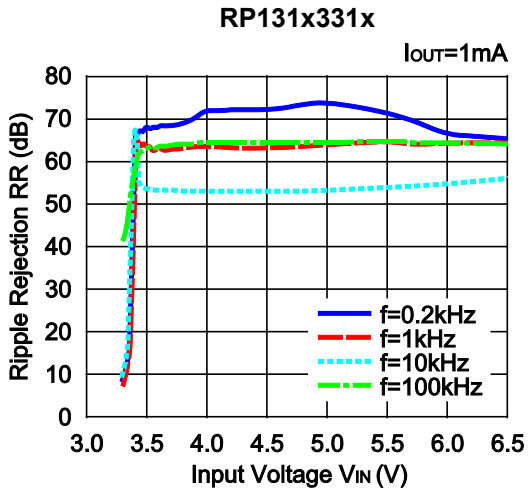

RP131x501x

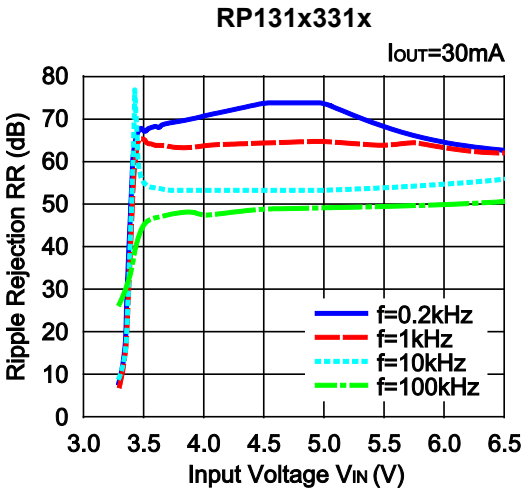


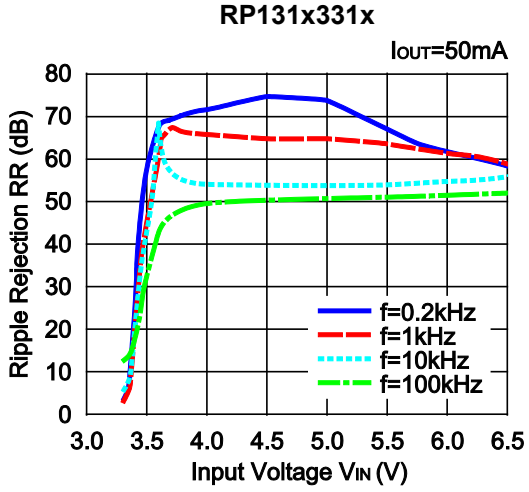
### 7) Dropout Voltage vs. Set Output Voltage

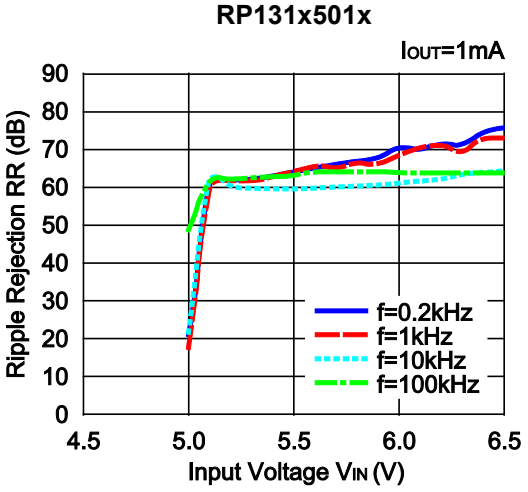



### 8) Ripple Rejection vs. Input Bias Voltage (C1=none, C2=Ceramic 1.0µF, Ripple=0.2Vp-p, Ta=25°C)



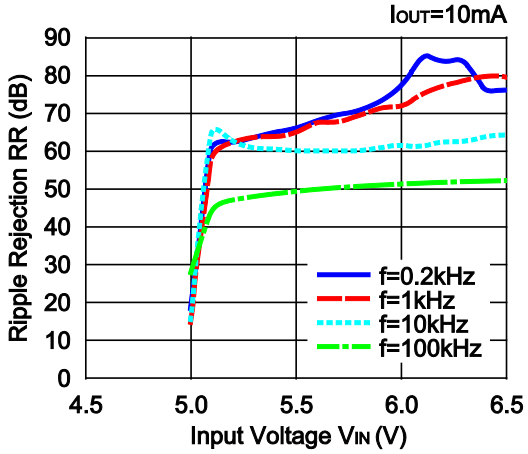



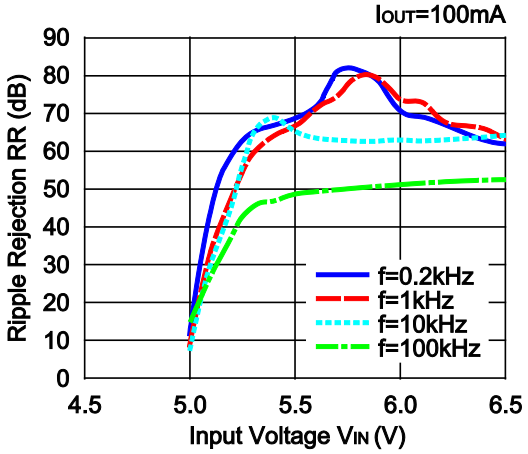
RP131x501x

$I_{OUT}$=10mA




RP131x501x

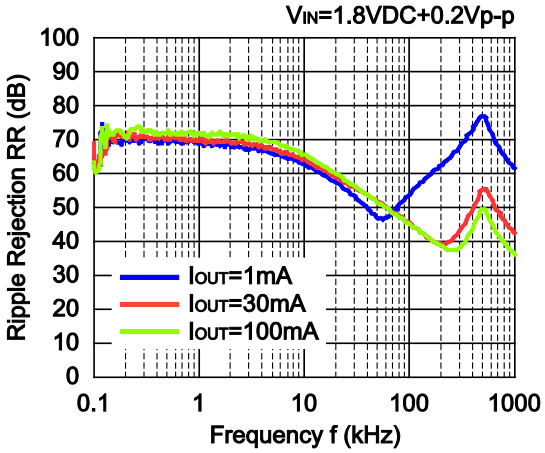
$I_{OUT}$=100mA




## 9) Ripple Rejection vs. Frequency (C1=none, C2=Ceramic 4.7µF, Ta=25°C)

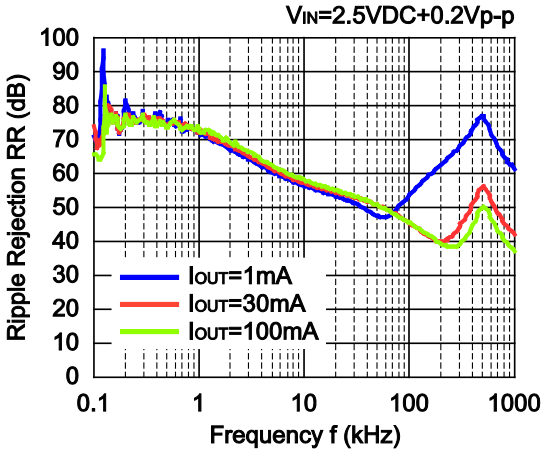
RP131x081x

$V_{IN}$=1.8VDC+0.2Vp-p



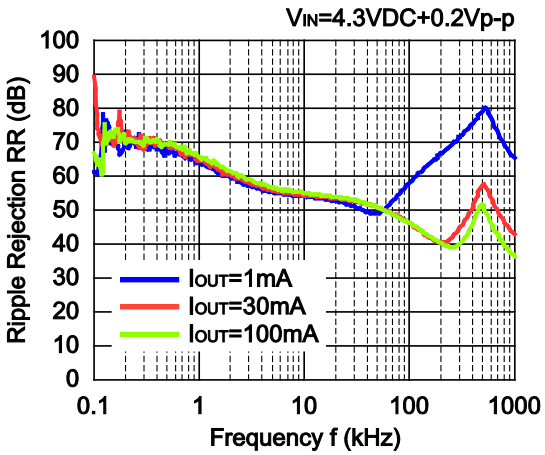

RP131x151x

$V_{IN}$=2.5VDC+0.2Vp-p



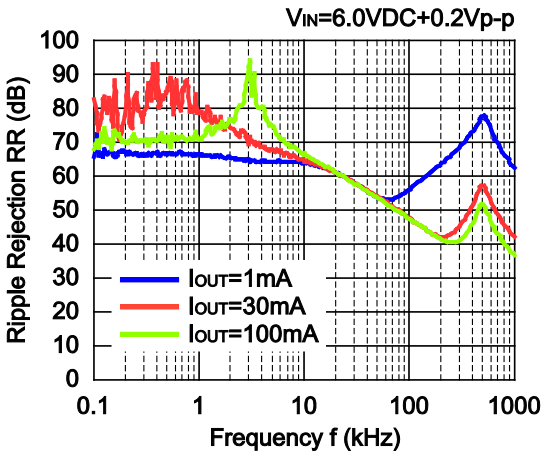

RP131x331x

$V_{IN}$=4.3VDC+0.2Vp-p



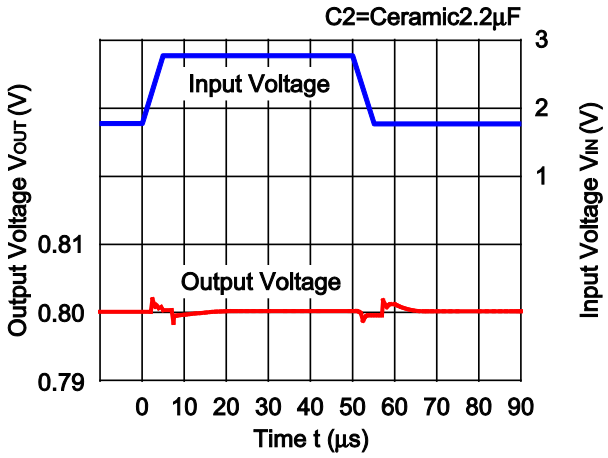

RP131x501x

$V_{IN}$=6.0VDC+0.2Vp-p

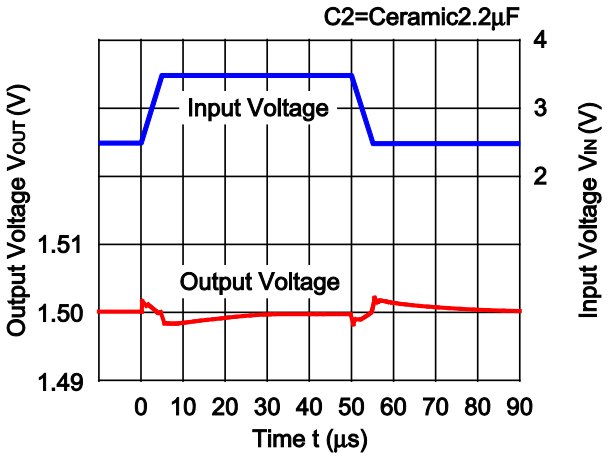


### 10) Input Transient Response ($I_{OUT}$=100mA, tr=tf=5µs, C1=none, Ta=25°C)

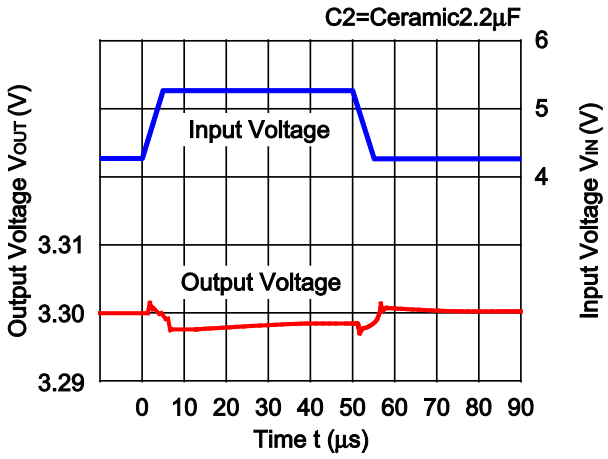
RP131x081x



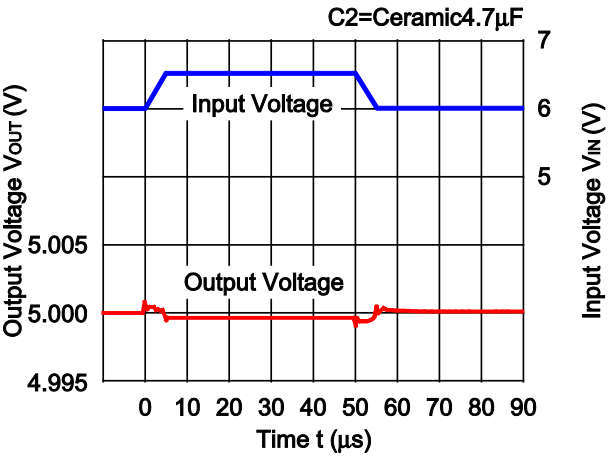

RP131x151x




RP131x331x

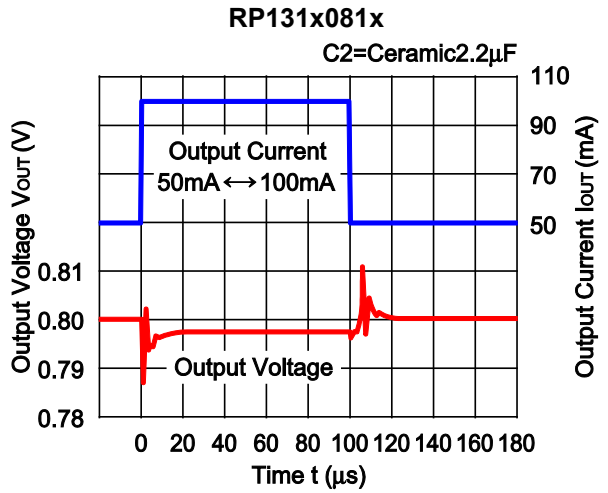



RP131x501x

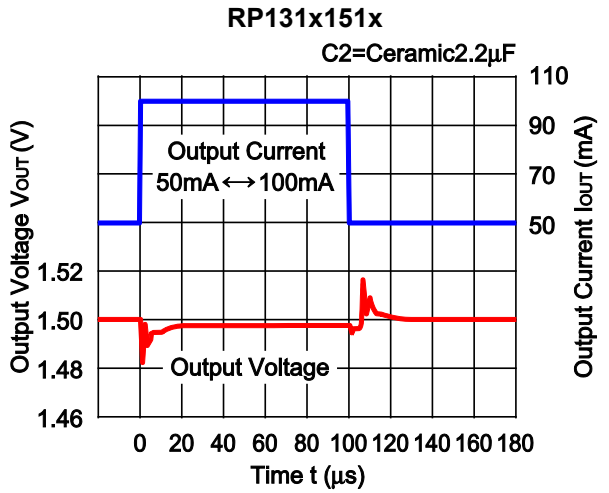



### 11) Load Transient Response (tr=tf=0.5µs, C1=Ceramic 2.2µF, $V_{IN}$=$V_{OUT}$+1.0V, Topt=25°C)

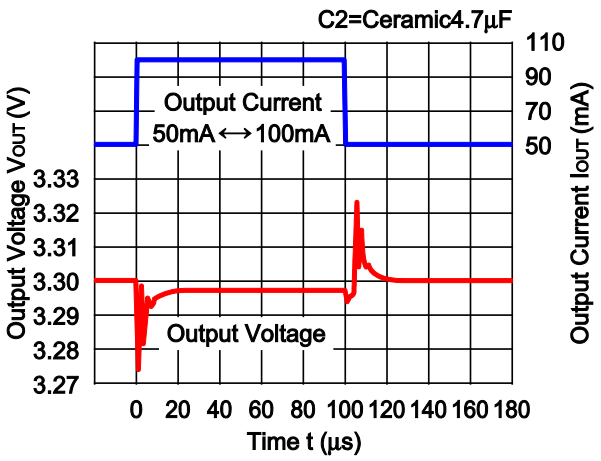
RP131x081x



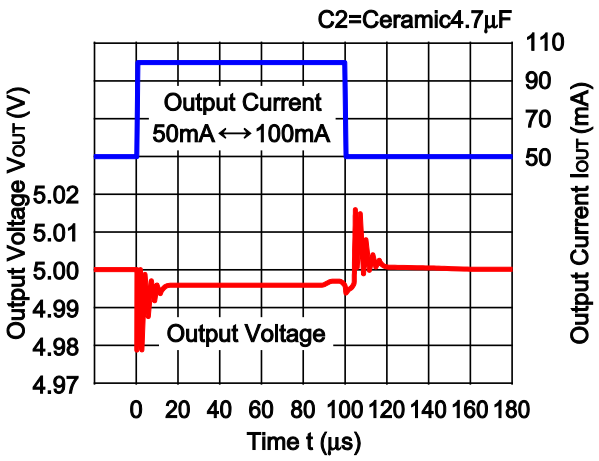

RP131x151x



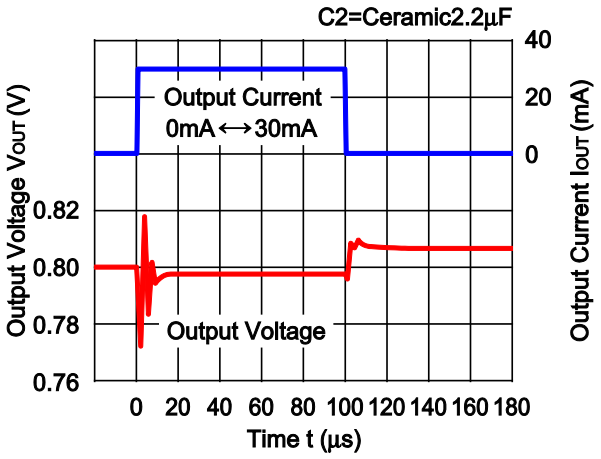
RP131x331x



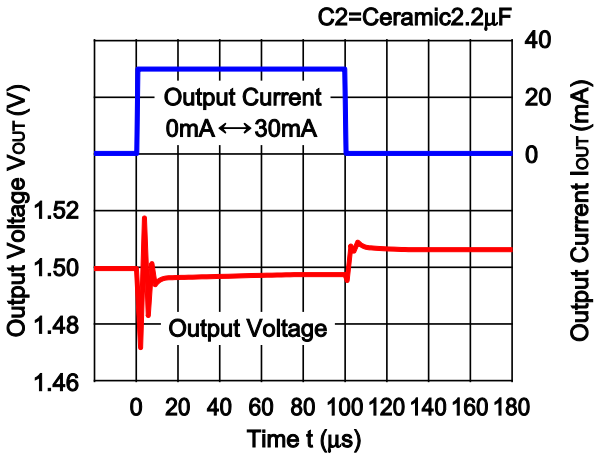

RP131x501x



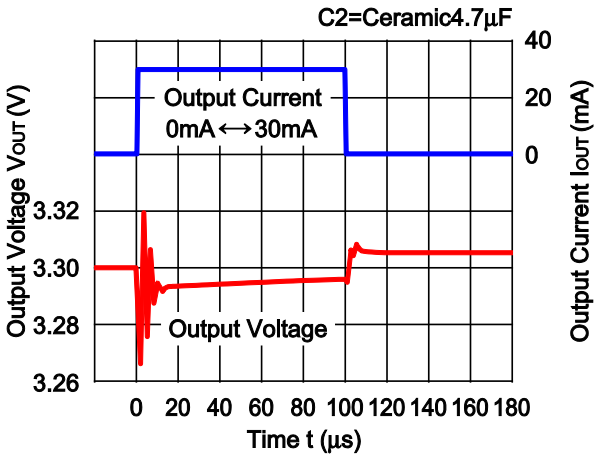

RP131x081x



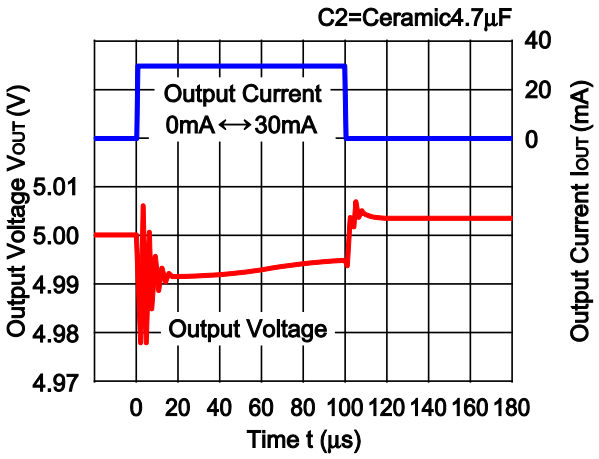

RP131x151x



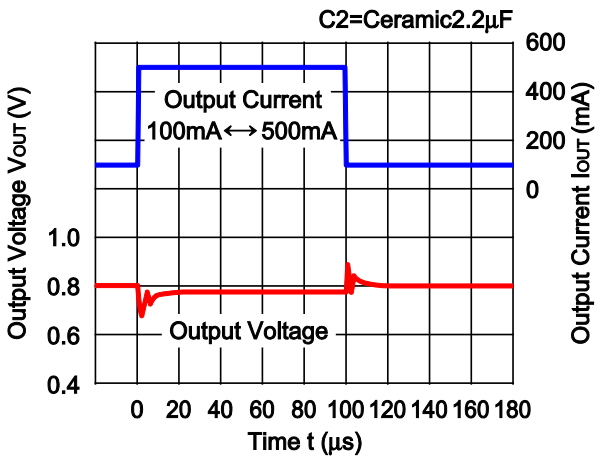

RP131x331x



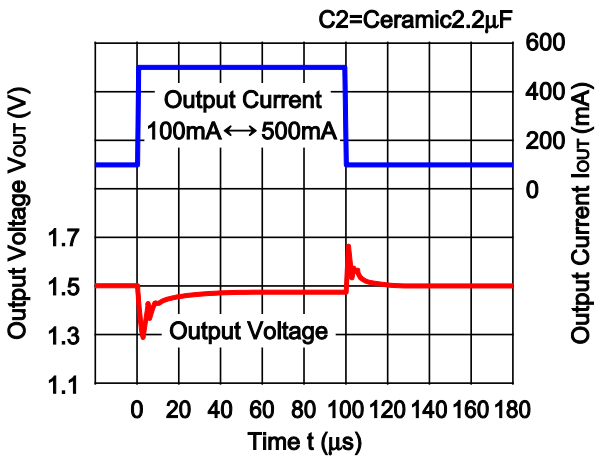

RP131x501x



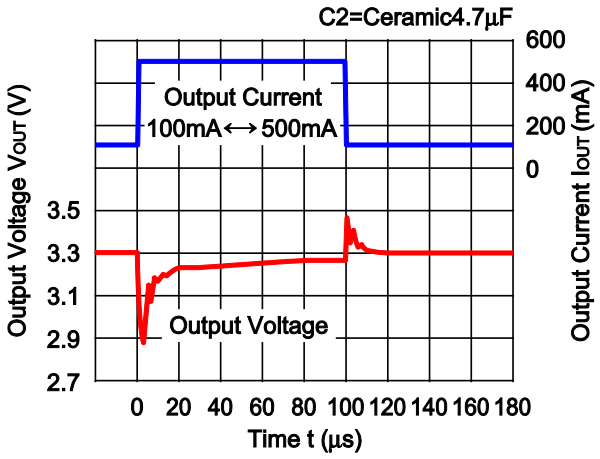
RP131x081x



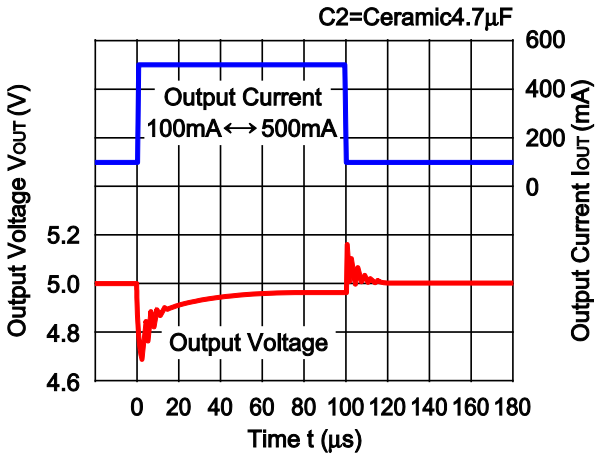

RP131x151x




RP131x331x

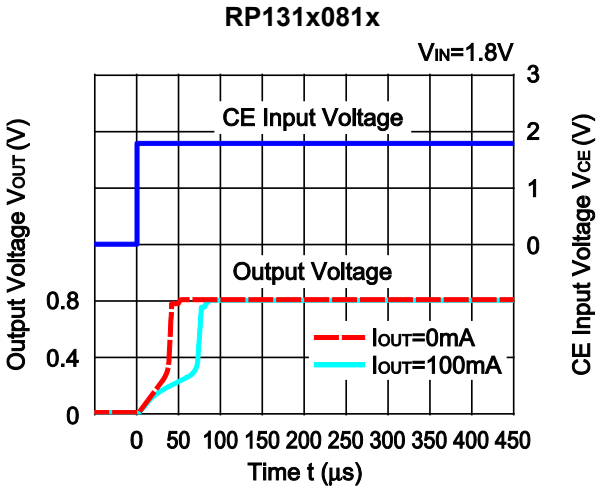



RP131x501x

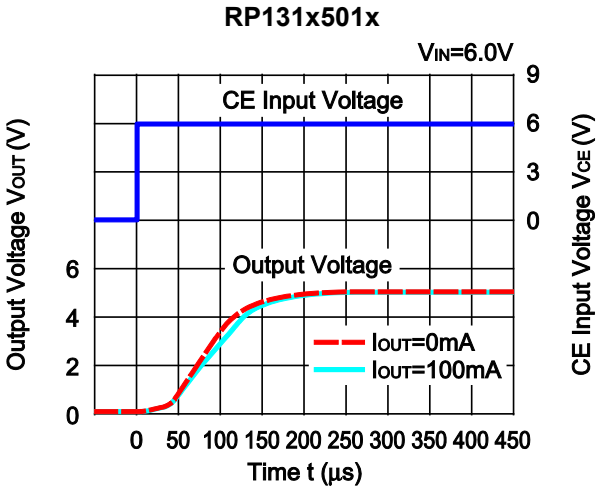



## 12) Turn On Speed with CE pin (C1=Ceramic 2.2µF, C2=Ceramic 4.7µF, Topt=25°C)

RP131x081x

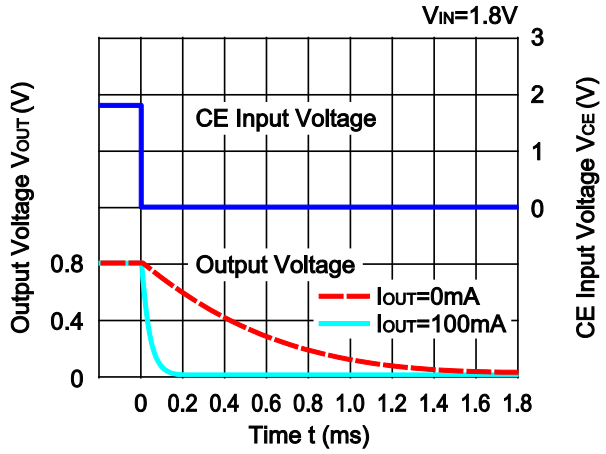



RP131x501x

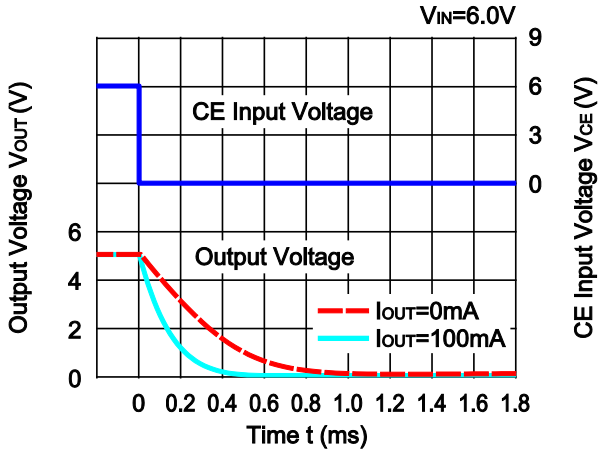


### 13) Turn Off Speed with CE pin (D Version) (C1=Ceramic 2.2µF, C2=Ceramic 4.7µF, Ta=25°C)

RP131x081D

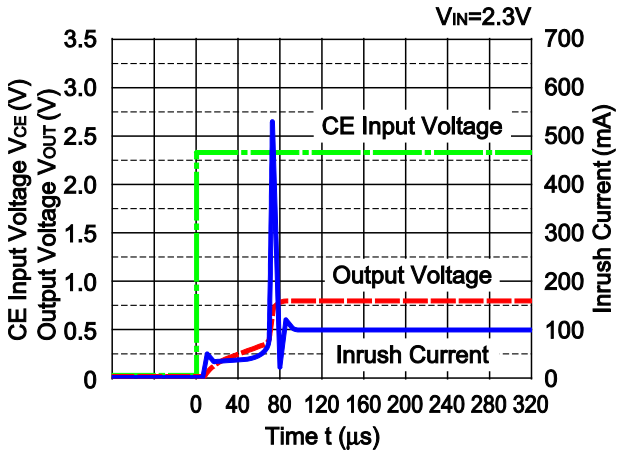



RP131x501D

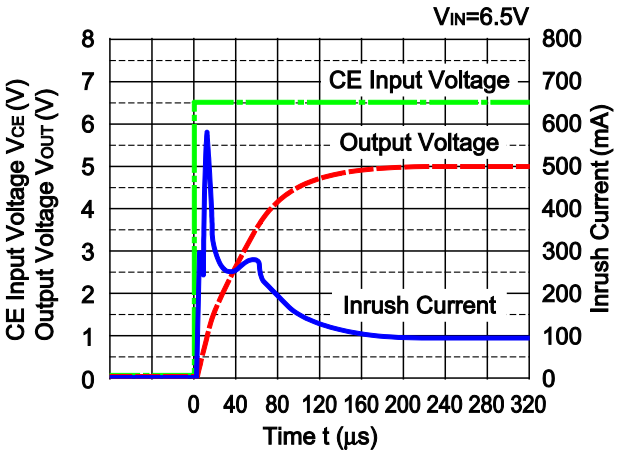



### 14) Inrush Current at turning on (C1=Ceramic 2.2µF, C2=Ceramic 4.7µF, Topt=25°C)

RP131x081x

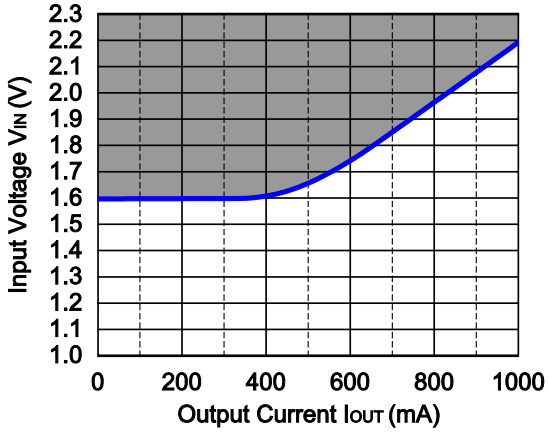



RP131x501x




### 15) Minimum Operating Voltage

RP131x081x




Hatched area is available for 0.8V output.

# ESR vs. Output Current

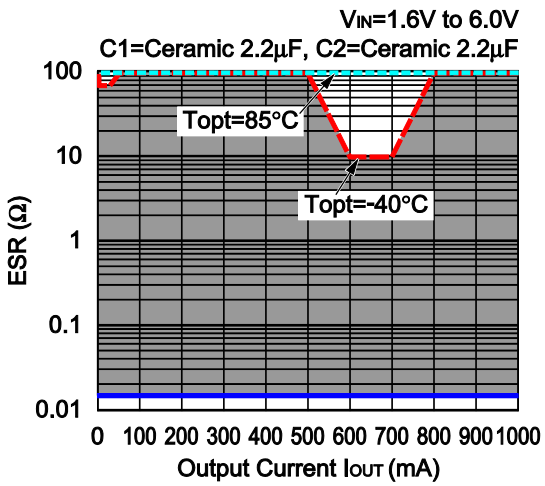
When using these ICs, consider the following points:

The relations between $I_{OUT}$ (Output Current) and ESR of an output capacitor are shown below.
The conditions when the white noise level is under 40μV (Avg.) are marked as the hatched area in the graph.

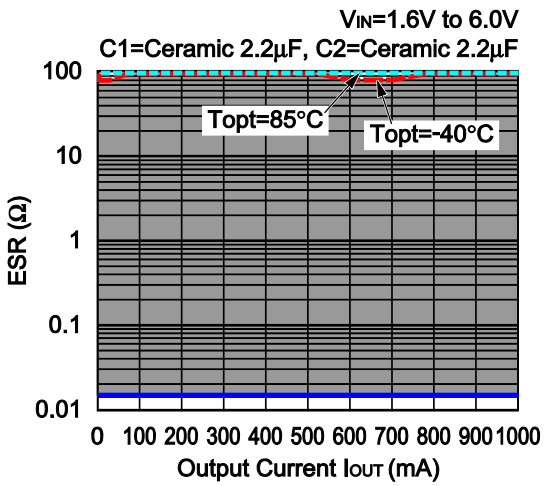
**Measurement conditions**

Frequency Band : 10Hz to 3MHz
Temperature : –40°C to 85°C
C1 : 2.2μF (Kyocera, CM05X5R225M04AD)
C2 : 2.2μF (Kyocera, CM105X5R225K06AE)
4.7μF (Kyocera, CM105X5R475M06AB)

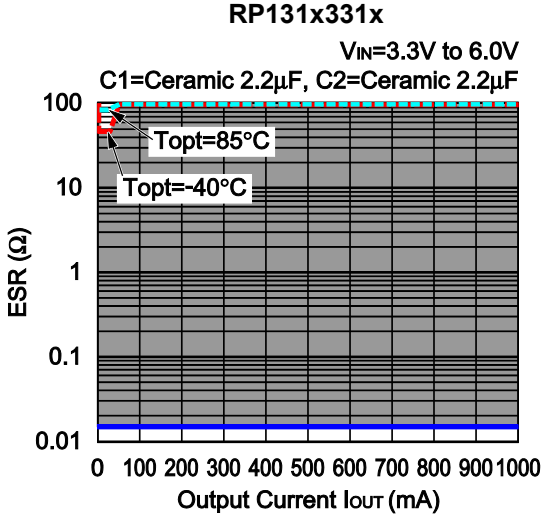
**RP131x081x**



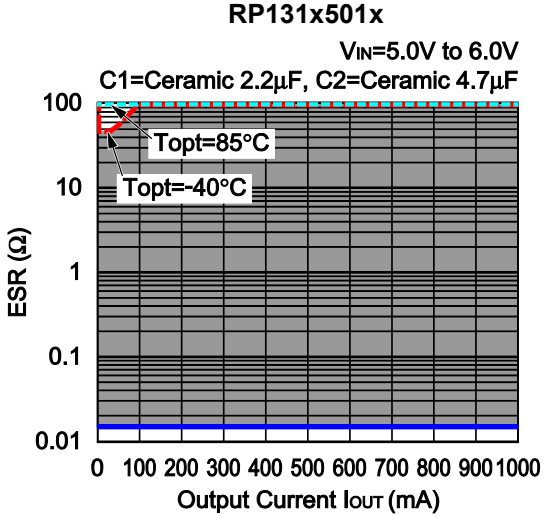

**RP131x151x**




**RP131x331x**




**RP131x501x**



# POWER DISSIPATION DFN1616-6B

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

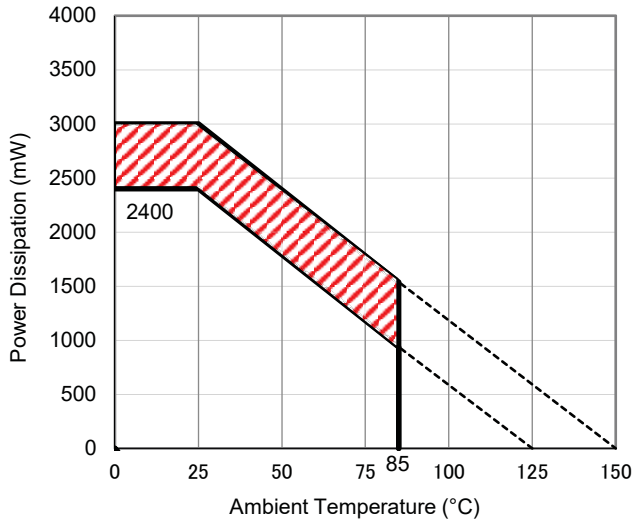
**Measurement Conditions**

| Item | Measurement Conditions |
|---|---|
| Environment | Mounting on Board (Wind Velocity = 0 m/s) |
| Board Material | Glass Cloth Epoxy Plastic (Four-Layer Board) |
| Board Dimensions | 76.2 mm × 114.3 mm × 0.8 mm |
| Copper Ratio | Outer Layer (First Layer): Less than 95% of 50 mm Square<br>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square<br>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square |
| Through-holes | ϕ 0.2 mm × 15 pcs |

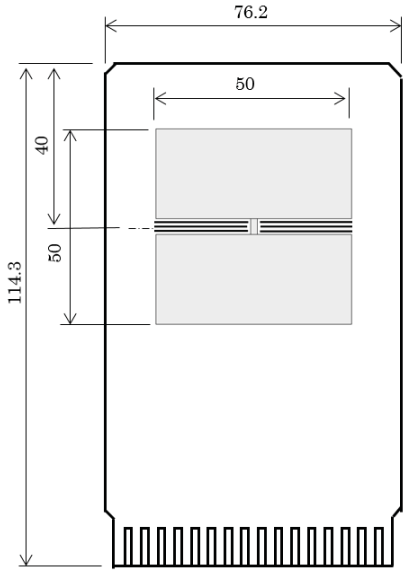
**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

| Item | Measurement Result |
|---|---|
| Power Dissipation | 2400 mW |
| Thermal Resistance (θja) | θja = 41°C/W |
| Thermal Characterization Parameter (ψjt) | ψjt = 11°C/W |

θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter




**Power Dissipation vs. Ambient Temperature**



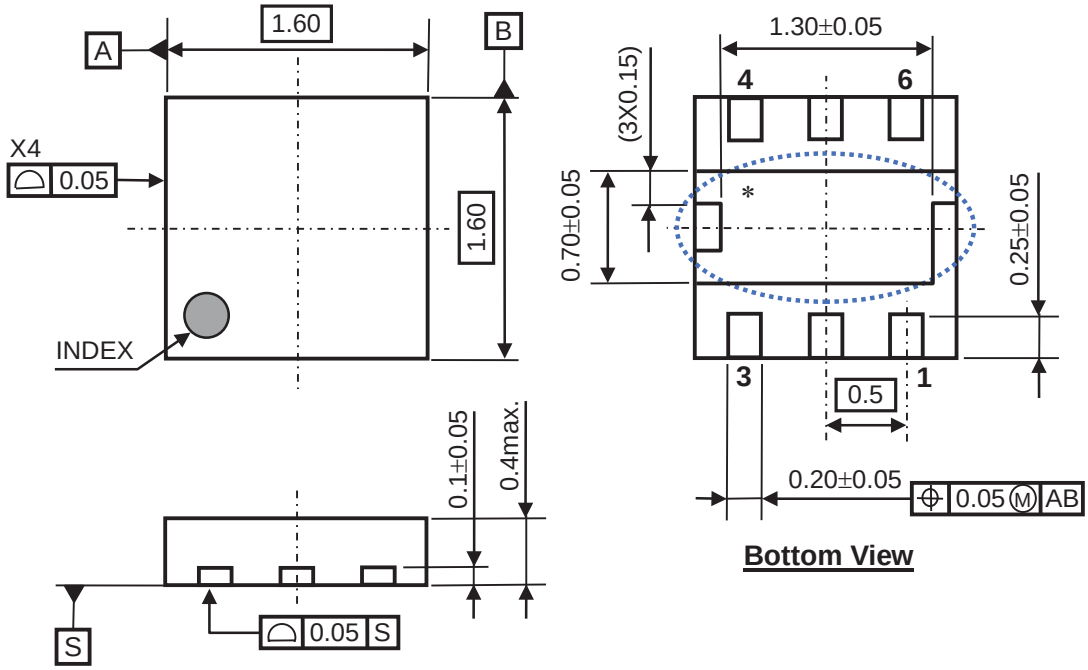

**Measurement Board Pattern**

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

| Total Hours of Use | Total Years of Use (4 hours/day) |
|---|---|
| 13,000 hours | 9 years |

# PACKAGE DIMENSIONS DFN1616-6B

Ver. A




**DFN1616-6B Package Dimensions (Unit: mm)**

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

# POWER DISSIPATION DFN(PL)1820-6

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

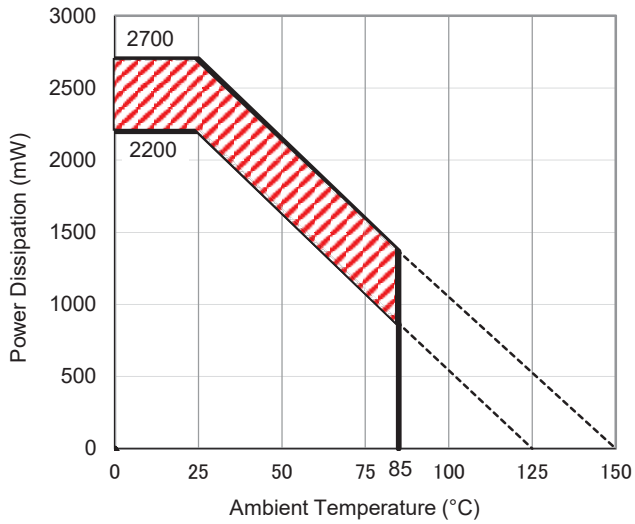
| Item | Measurement Conditions |
|---|---|
| Environment | Mounting on Board (Wind Velocity = 0 m/s) |
| Board Material | Glass Cloth Epoxy Plastic (Four-Layer Board) |
| Board Dimensions | 76.2 mm × 114.3 mm × 0.8 mm |
| Copper Ratio | Outer Layer (First Layer): Less than 95% of 50 mm Square<br>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square<br>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square |
| Through-holes | ϕ 0.2 mm × 34 pcs |

**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

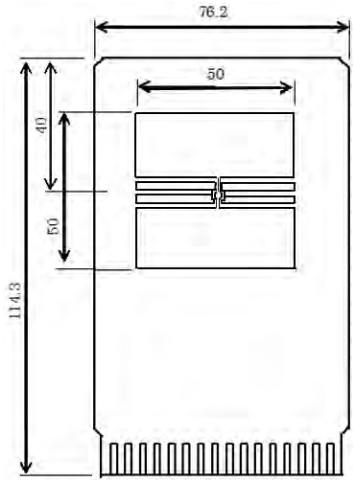
| Item | Measurement Result |
|---|---|
| Power Dissipation | 2200 mW |
| Thermal Resistance (θja) | θja = 45°C/W |
| Thermal Characterization Parameter (ψjt) | ψjt = 18°C/W |

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter




**Power Dissipation vs. Ambient Temperature**



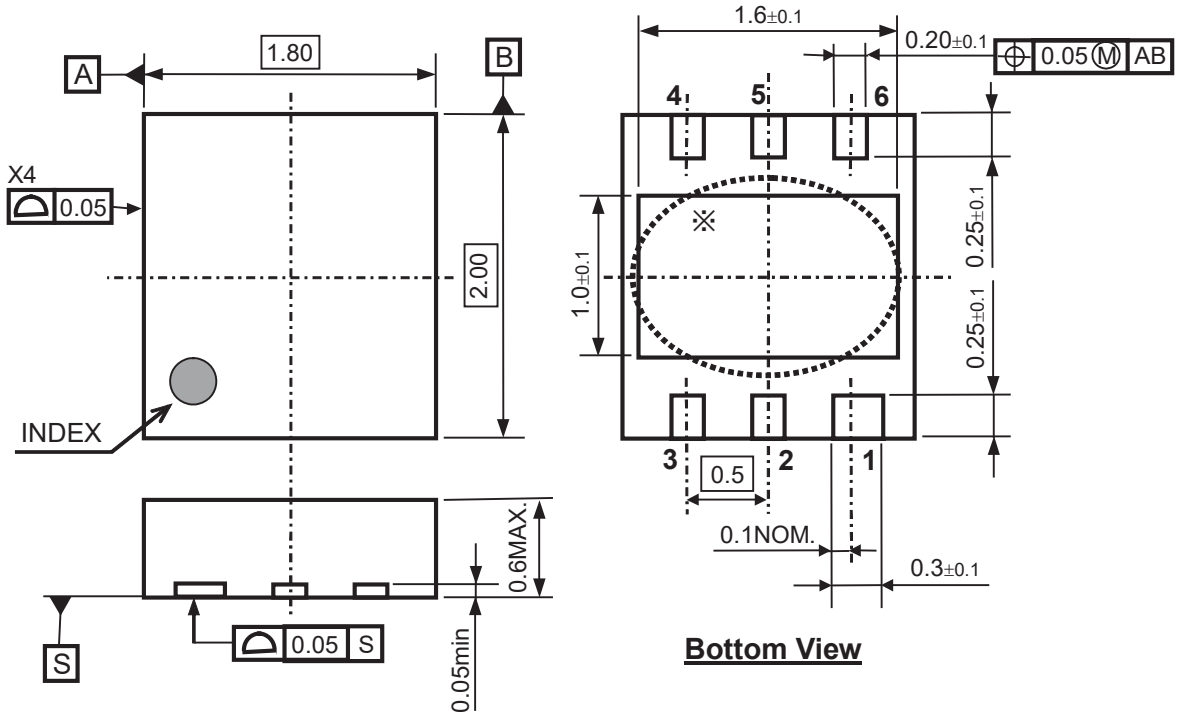

**Measurement Board Pattern**

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

| Total Hours of Use | Total Years of Use (4 hours/day) |
|---|---|
| 13,000 hours | 9 years |

# PACKAGE DIMENSIONS DFN(PL)1820-6

Ver. A




**DFN(PL)1820-6 Package Dimensions (Unit: mm)**

∗ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

# POWER DISSIPATION SOT-89-5

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

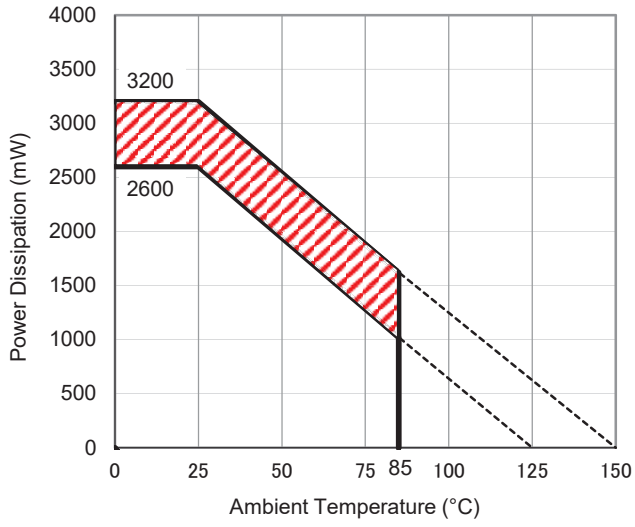
| Item | Measurement Conditions |
|---|---|
| Environment | Mounting on Board (Wind Velocity = 0 m/s) |
| Board Material | Glass Cloth Epoxy Plastic (Four-Layer Board) |
| Board Dimensions | 76.2 mm × 114.3 mm × 0.8 mm |
| Copper Ratio | Outer Layer (First Layer): Less than 95% of 50 mm Square<br>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square<br>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square |
| Through-holes | ϕ 0.3 mm × 13 pcs |

**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

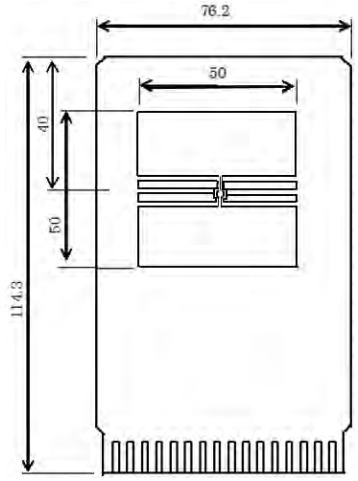
| Item | Measurement Result |
|---|---|
| Power Dissipation | 2600 mW |
| Thermal Resistance (θja) | θja = 38°C/W |
| Thermal Characterization Parameter (ψjt) | ψjt = 13°C/W |

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter




**Power Dissipation vs. Ambient Temperature**



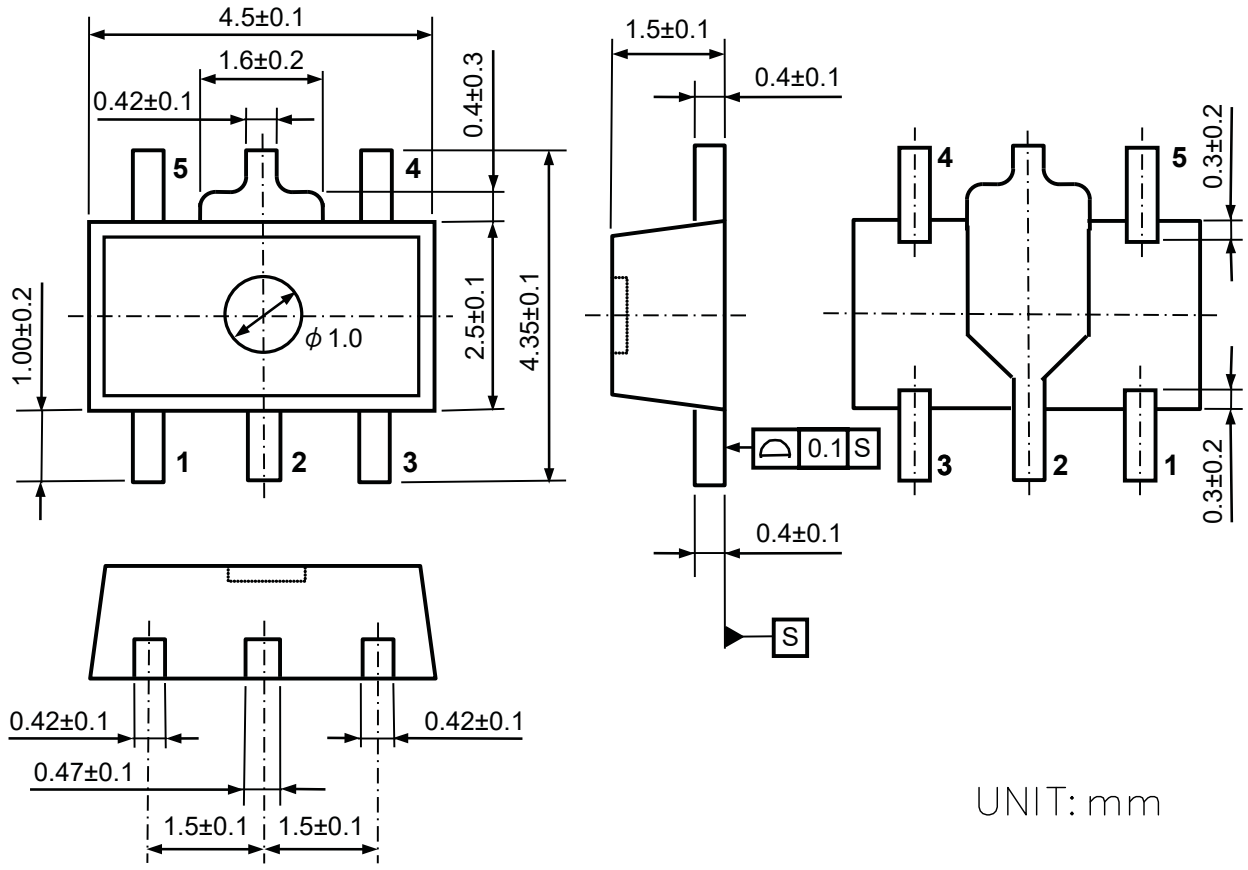

**Measurement Board Pattern**

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

| Total Hours of Use | Total Years of Use (4 hours/day) |
|---|---|
| 13,000 hours | 9 years |

# PACKAGE DIMENSIONS SOT-89-5

Ver. A




**SOT-89-5 Package Dimensions**

# POWER DISSIPATION HSOP-6J

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

**Measurement Conditions**

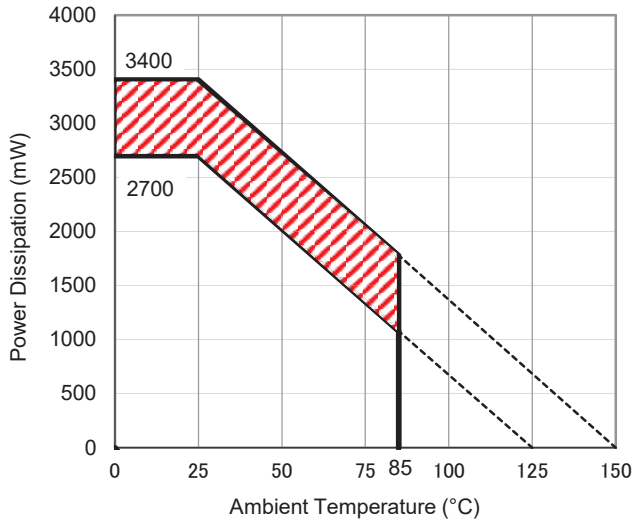
| Item | Measurement Conditions |
|---|---|
| Environment | Mounting on Board (Wind Velocity = 0 m/s) |
| Board Material | Glass Cloth Epoxy Plastic (Four-Layer Board) |
| Board Dimensions | 76.2 mm × 114.3 mm × 0.8 mm |
| Copper Ratio | Outer Layer (First Layer): Less than 95% of 50 mm Square<br>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square<br>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square |
| Through-holes | ϕ 0.3 mm × 28 pcs |

**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

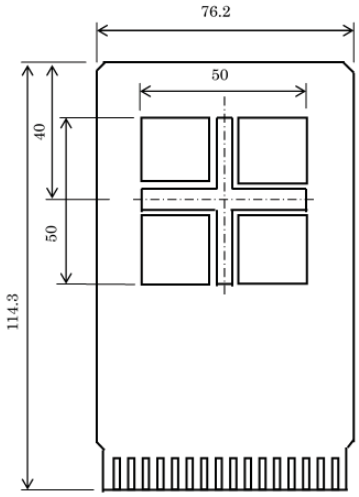
| Item | Measurement Result |
|---|---|
| Power Dissipation | 2700 mW |
| Thermal Resistance (θja) | θja = 37°C/W |
| Thermal Characterization Parameter (ψjt) | ψjt = 7°C/W |

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter




**Power Dissipation vs. Ambient Temperature**



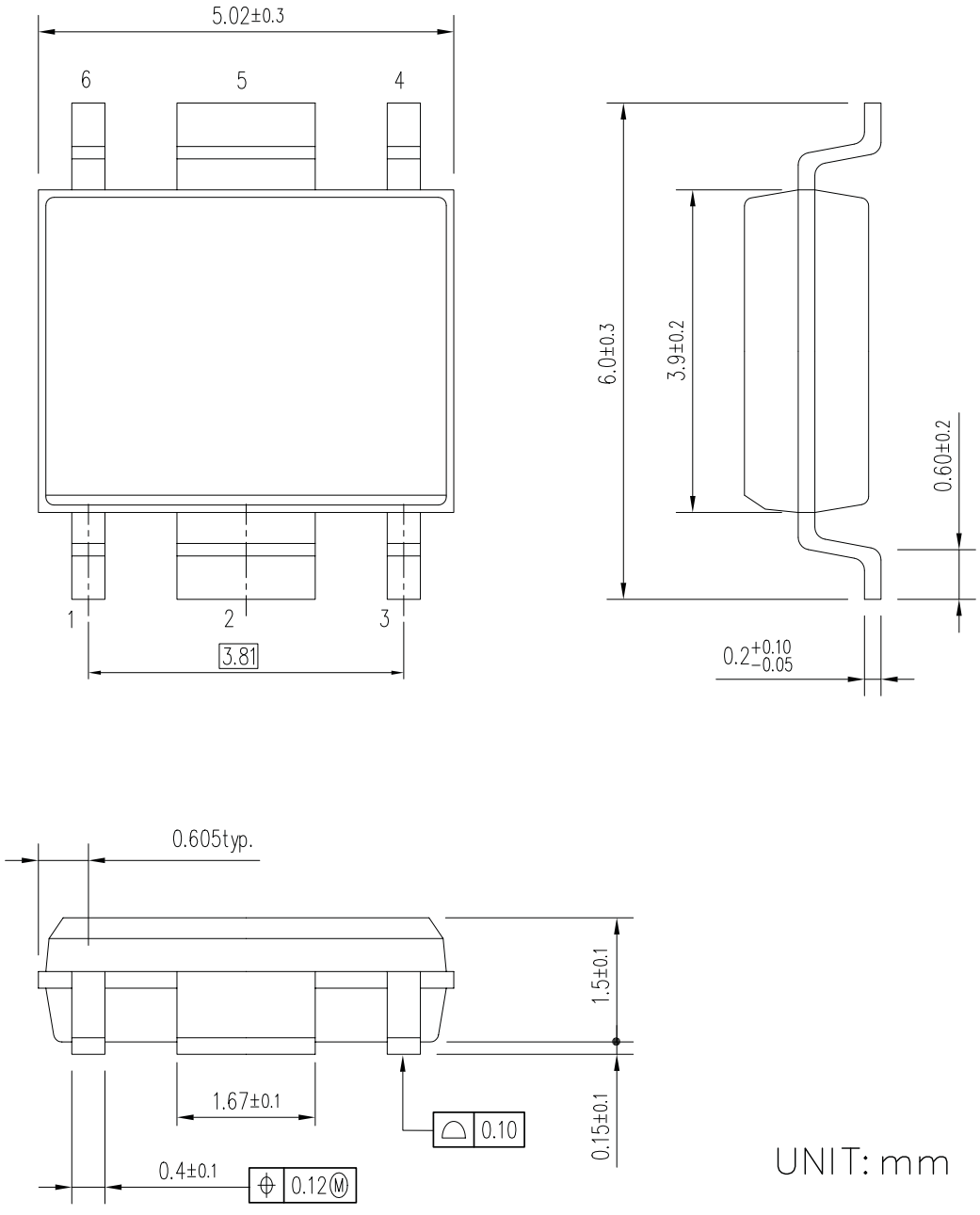

**Measurement Board Pattern**

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

| Total Hours of Use | Total Years of Use (4 hours/day) |
|---|---|
| 13,000 hours | 9 years |

# PACKAGE DIMENSIONS HSOP-6J

Ver. A




**HSOP-6J Package Dimensions**

# POWER DISSIPATION TO-252-5

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

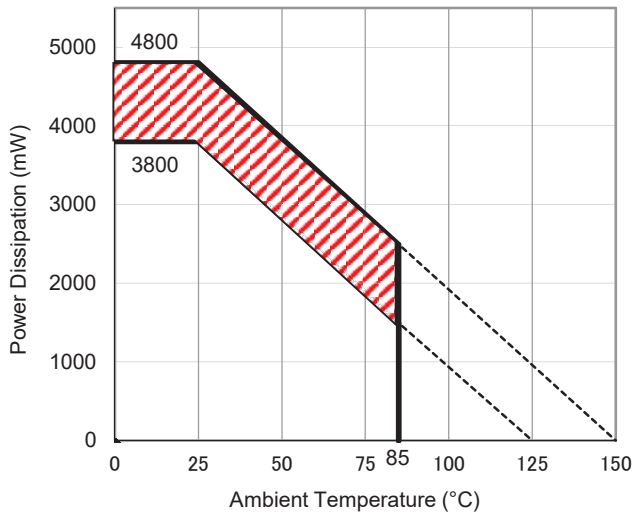
**Measurement Conditions**

| Item | Measurement Conditions |
|---|---|
| Environment | Mounting on Board (Wind Velocity = 0 m/s) |
| Board Material | Glass Cloth Epoxy Plastic (Four-Layer Board) |
| Board Dimensions | 76.2 mm × 114.3 mm × 0.8 mm |
| Copper Ratio | Outer Layer (First Layer): Less than 95% of 50 mm Square<br>Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square<br>Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square |
| Through-holes | ϕ 0.3 mm × 21 pcs |

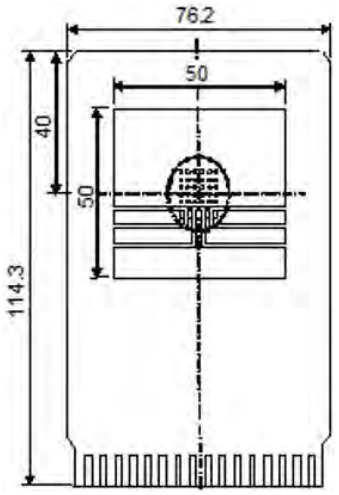
**Measurement Result** (Ta = 25°C, Tjmax = 125°C)

| Item | Measurement Result |
|---|---|
| Power Dissipation | 3800 mW |
| Thermal Resistance (θja) | θja = 26°C/W |
| Thermal Characterization Parameter (ψjt) | ψjt = 7°C/W |

θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter




**Power Dissipation vs. Ambient Temperature**



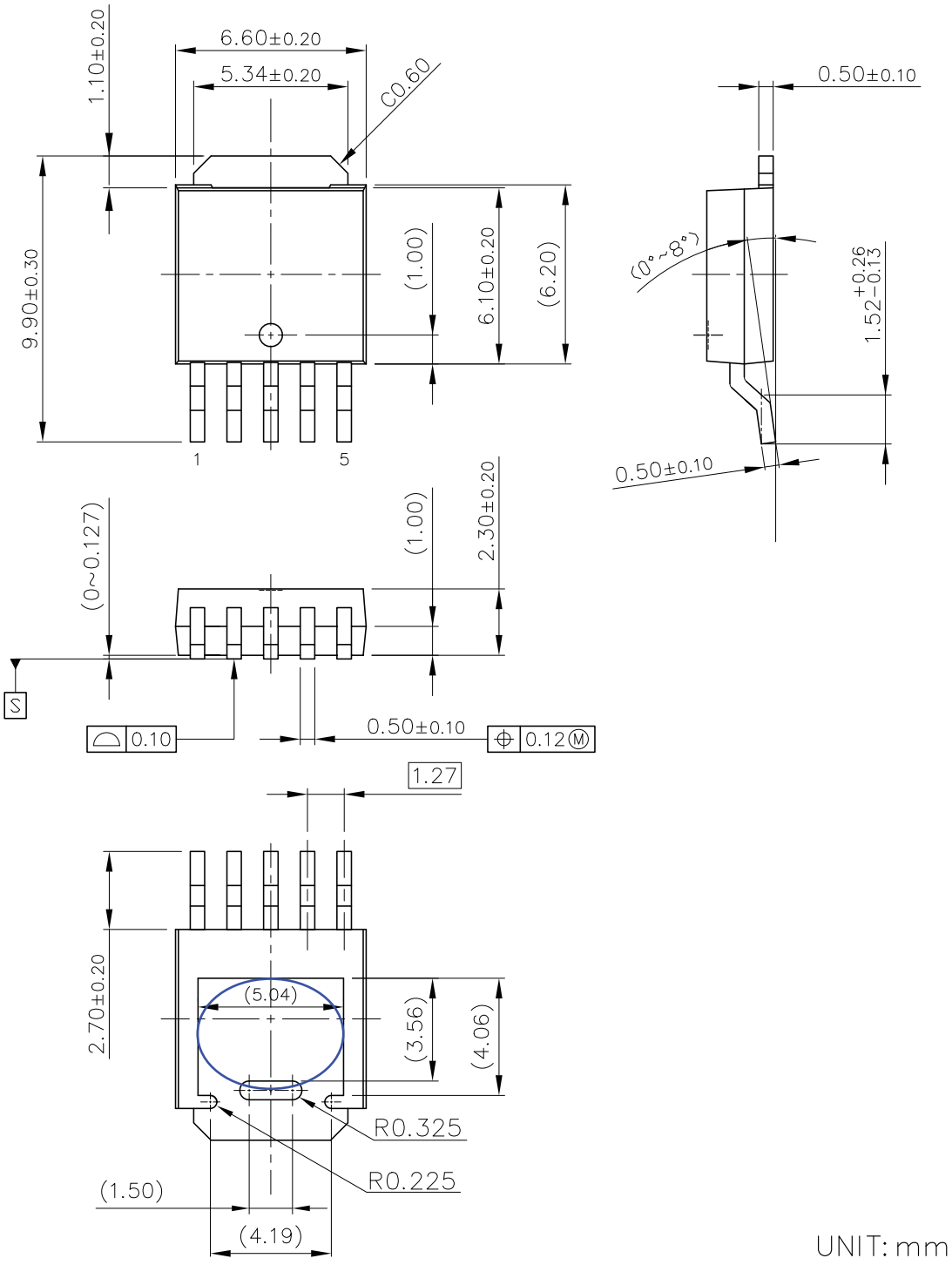

**Measurement Board Pattern**

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

| Total Hours of Use | Total Years of Use (4 hours/day) |
|---|---|
| 13,000 hours | 9 years |

# PACKAGE DIMENSIONS TO-252-5-P2

Ver. A




**TO-252-5-P2 Package Dimensions**

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
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    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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